

Reconceptualizing to Unshackle Programmers from the Burden of Exascale Hardware Issues

Abstract: This talk will start with a description of the anticipated hardware constraints for year 2018 silicon and computer architectures, drawing on public materials from Reservoir Labs' experiences as part of the Intel UHPC Runnemedede team. We will itemize the specific challenges arising, such as the concurrency, variances, and resilience issues arising from the near-subthreshold voltage supply levels needed to achieve exascale with reasonable power, and constraints arising from the memory system. We will argue that these hardware aspects should not surface to the level of the programming interface, but rather that it is plausible that they could be addressed with automatic mapping tools: static and dynamic. We will describe the language interfaces that are helpful – particularly semantic annotations that increase the available concurrency and scheduling flexibility, and a split between application expressing and tuning expression orthogonally, and different kinds of tuning expressions. We will also describe issues in runtimes, particularly with respect to the need for new research in regulating and automatic scheduling fine grained computations, and the dynamics of message-driven computations.