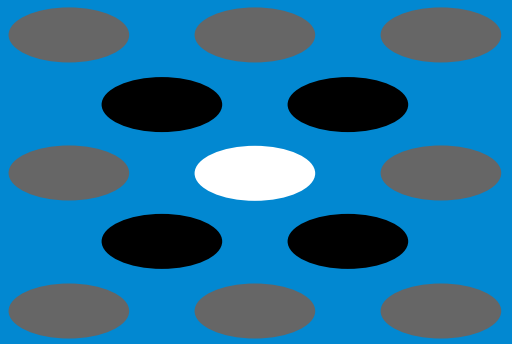


CAPORUS
TECHNOLOGIES

Material and Design Advances in Silicon-on-Insulator Substrates to Improve Nuclear Physics Sensors and Circuits

August 13, 2024

Redacted Copy for Distribution

Intro to Caporus & NLP™

Silicon on Insulator for NP

Phase II Demonstration

Intro to Caporus & NLP™

Silicon on Insulator for NP

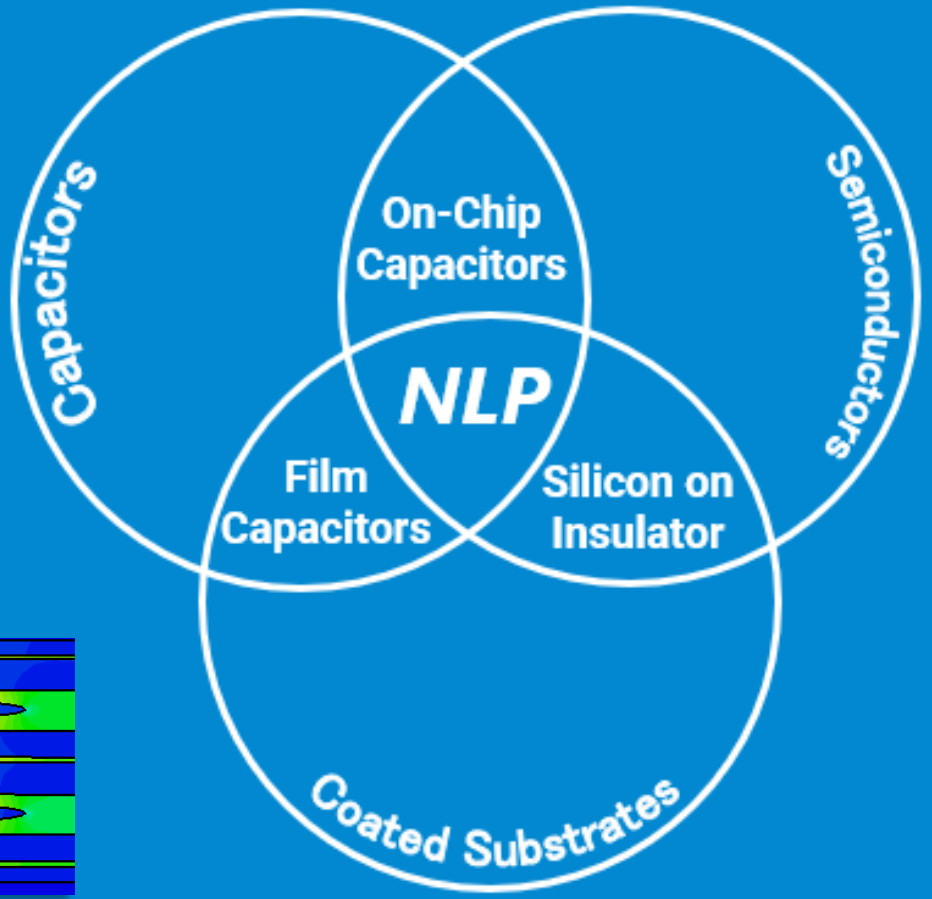
Phase II Demonstration

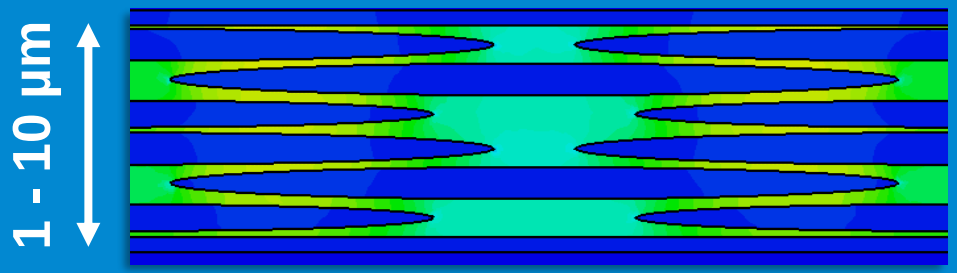
Caporus NLP™

CAPORUS TECHNOLOGIES

Nanoscale Lamellar Porosity™ (NLP™)

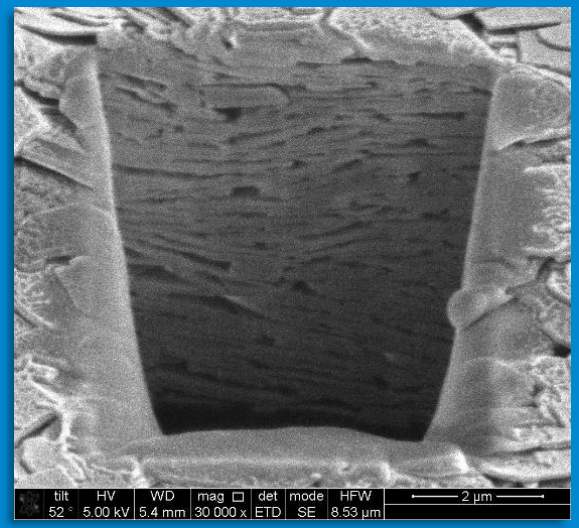
Controls the electric field distribution within a porous ceramic structure





illustration

Ceramic matrix (blue)
Porous regions (green)

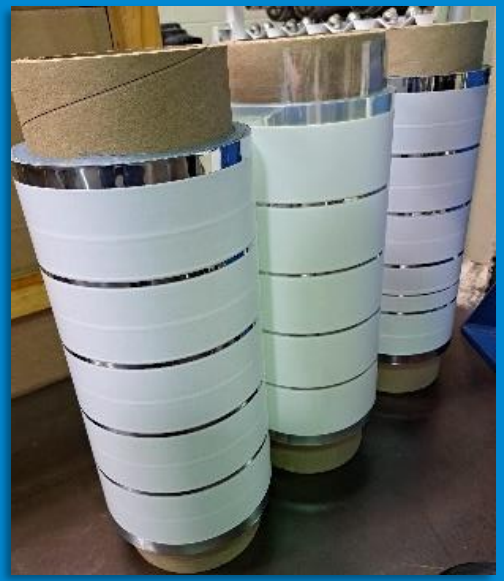


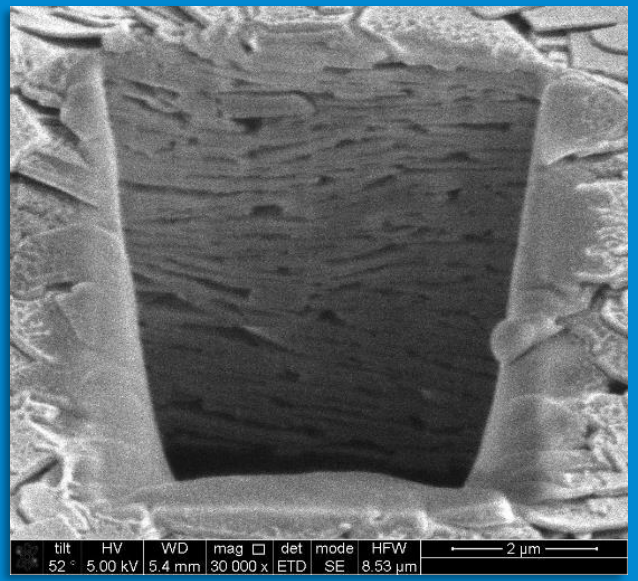
FIB image of material

NLP™ Technology | Production at Scale

>10 L Slurry Production

Compatible with High-Volume Roll-to-Roll Manufacturing

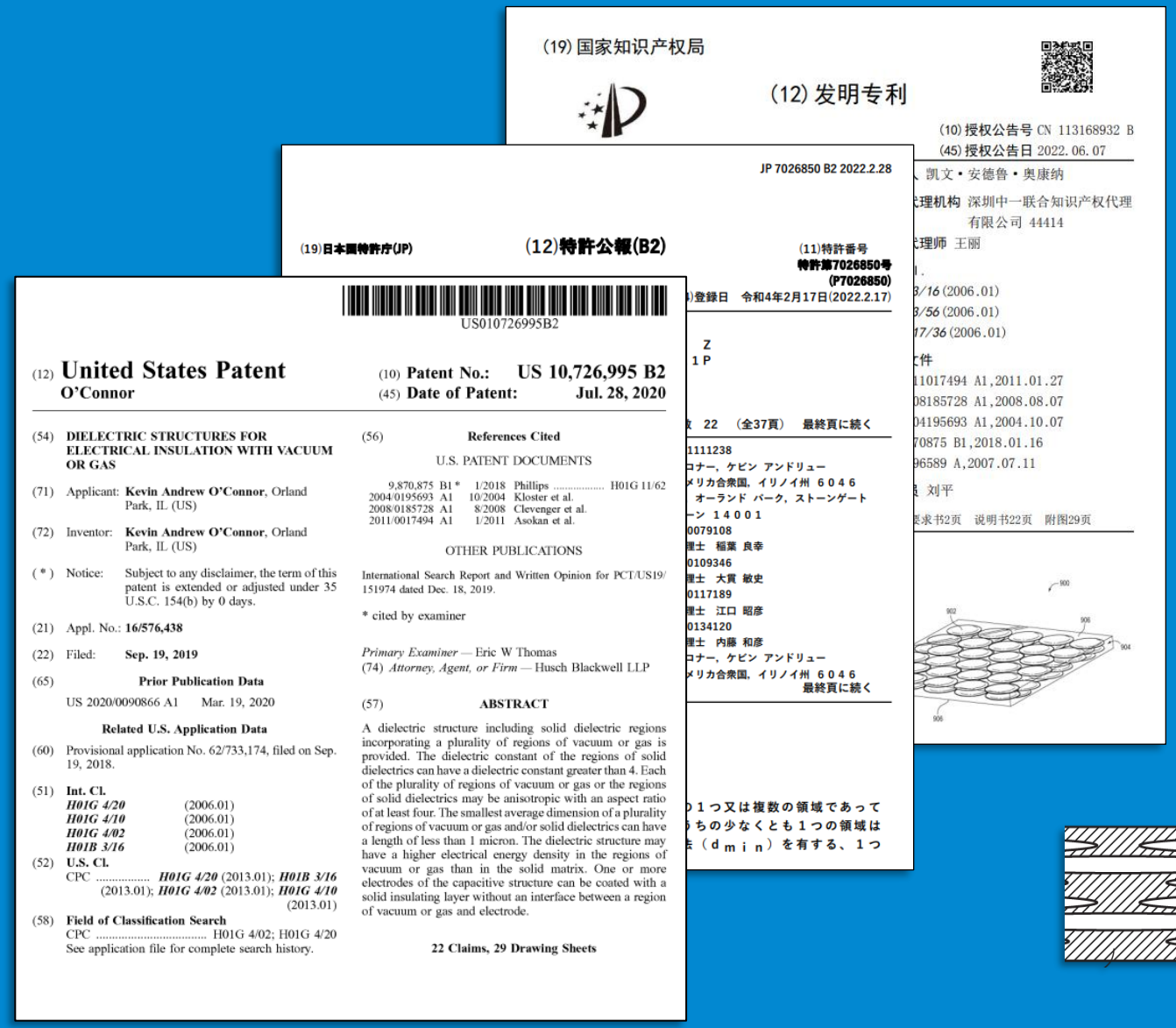




Demonstrated Nanoscale Lamellar Porosity over Large Areas

Slurry-based coating for R2R deposition of ceramic coating - No sintering required

NLP | Issued IP



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(12)特許公報(B2)

(11)特許番号
特許第7026850号
(P7026850)

US010726995B2

(12) **United States Patent**
O'Connor

(10) **Patent No.: US 10,726,995 B2**
(45) **Date of Patent: Jul. 28, 2020**

(54) **DIELECTRIC STRUCTURES FOR ELECTRICAL INSULATION WITH VACUUM OR GAS**

(71) Applicant: **Kevin Andrew O'Connor**, Orland Park, IL (US)

(72) Inventor: **Kevin Andrew O'Connor**, Orland Park, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/576,438**

(22) Filed: **Sep. 19, 2019**

(65) **Prior Publication Data**

US 2020/0090866 A1 Mar. 19, 2020

Related U.S. Application Data

(60) Provisional application No. 62/733,174, filed on Sep. 19, 2018.

(51) **Int. Cl.**
H01G 4/20 (2006.01)
H01G 4/10 (2006.01)
H01G 4/02 (2006.01)
H01B 3/16 (2006.01)

(52) **U.S. Cl.**
CPC ***H01G 4/20*** (2013.01); ***H01B 3/16*** (2013.01); ***H01G 4/02*** (2013.01); ***H01G 4/10*** (2013.01)

(58) **Field of Classification Search**
CPC H01G 4/02; H01G 4/20
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

9,870,875 B1 * 1/2018 Phillips H01G 11/62
2004/0195693 A1 10/2004 Kloster et al.
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OTHER PUBLICATIONS

International Search Report and Written Opinion for PCT/US19/151974 dated Dec. 18, 2019.

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Primary Examiner — Eric W Thomas
(74) *Attorney, Agent, or Firm* — Husch Blackwell LLP

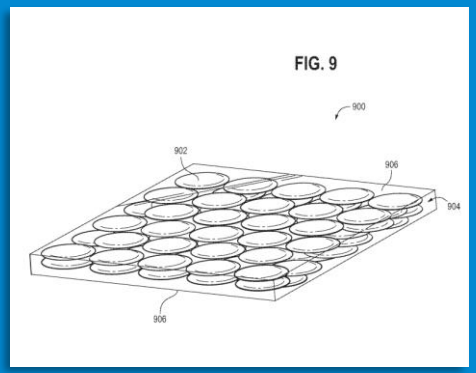
(57) **ABSTRACT**

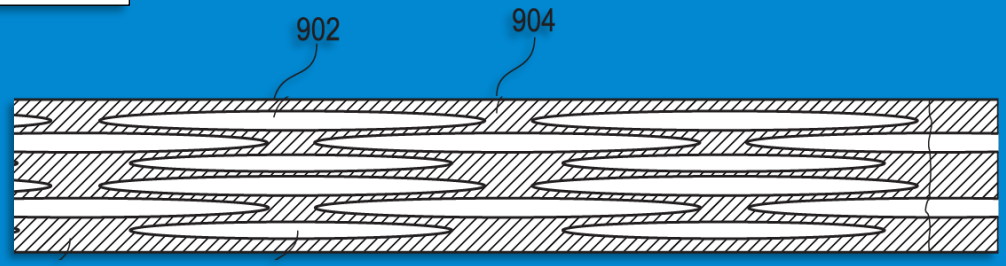
A dielectric structure including solid dielectric regions incorporating a plurality of regions of vacuum or gas is provided. The dielectric constant of the regions of solid dielectrics can have a dielectric constant greater than 4. Each of the plurality of regions of vacuum or gas or the regions of solid dielectrics may be anisotropic with an aspect ratio of at least four. The smallest average dimension of a plurality of regions of vacuum or gas and/or solid dielectrics can have a length of less than 1 micron. The dielectric structure may have a higher electrical energy density in the regions of vacuum or gas than in the solid matrix. One or more electrodes of the capacitive structure can be coated with a solid insulating layer without an interface between a region of vacuum or gas and electrode.

22 Claims, 29 Drawing Sheets

USPTO *issued July 2020*
JPO *issued March 2022*
CNIPA *issued June 2022*
EPO *pending*

additional filings in process

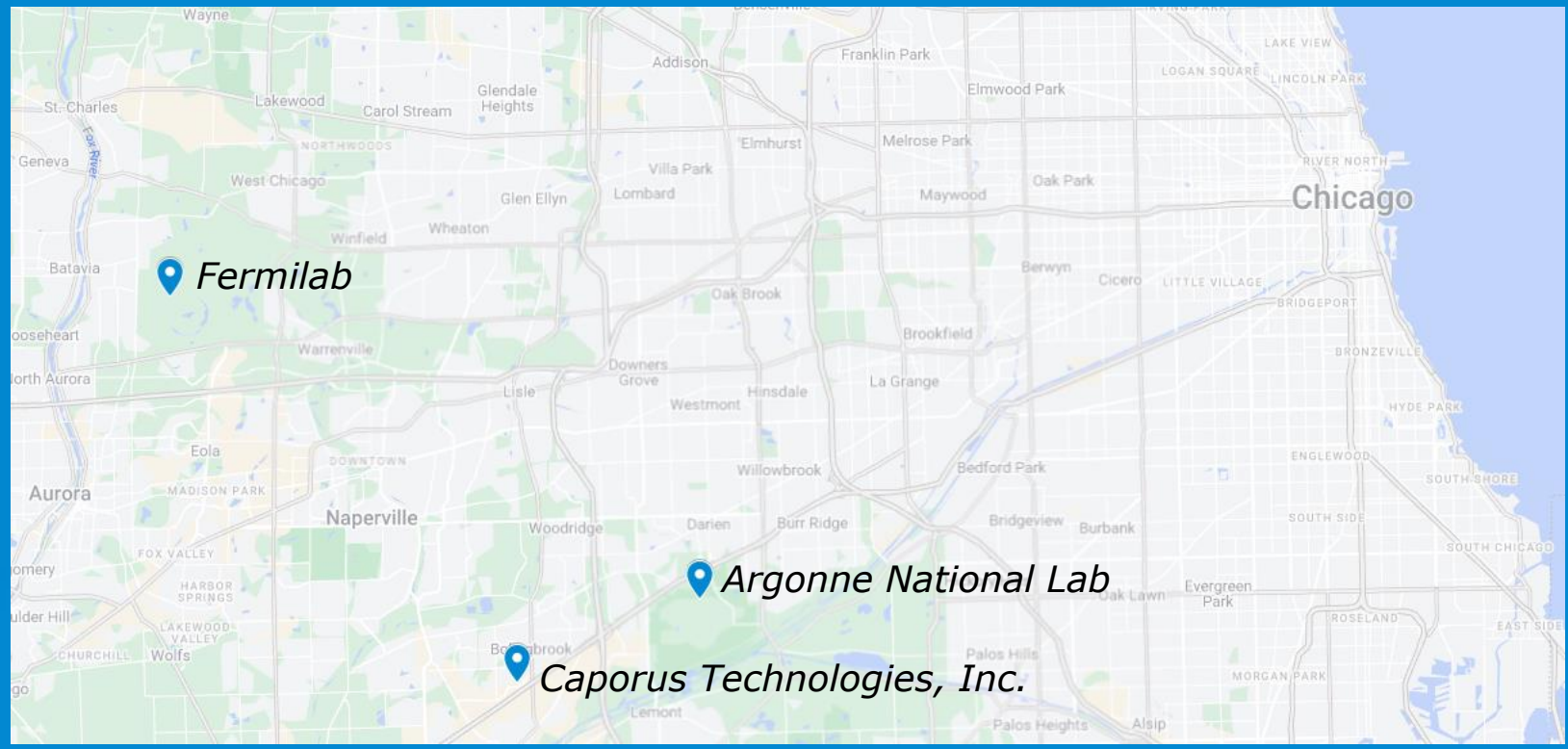




CAPORUS TECHNOLOGIES

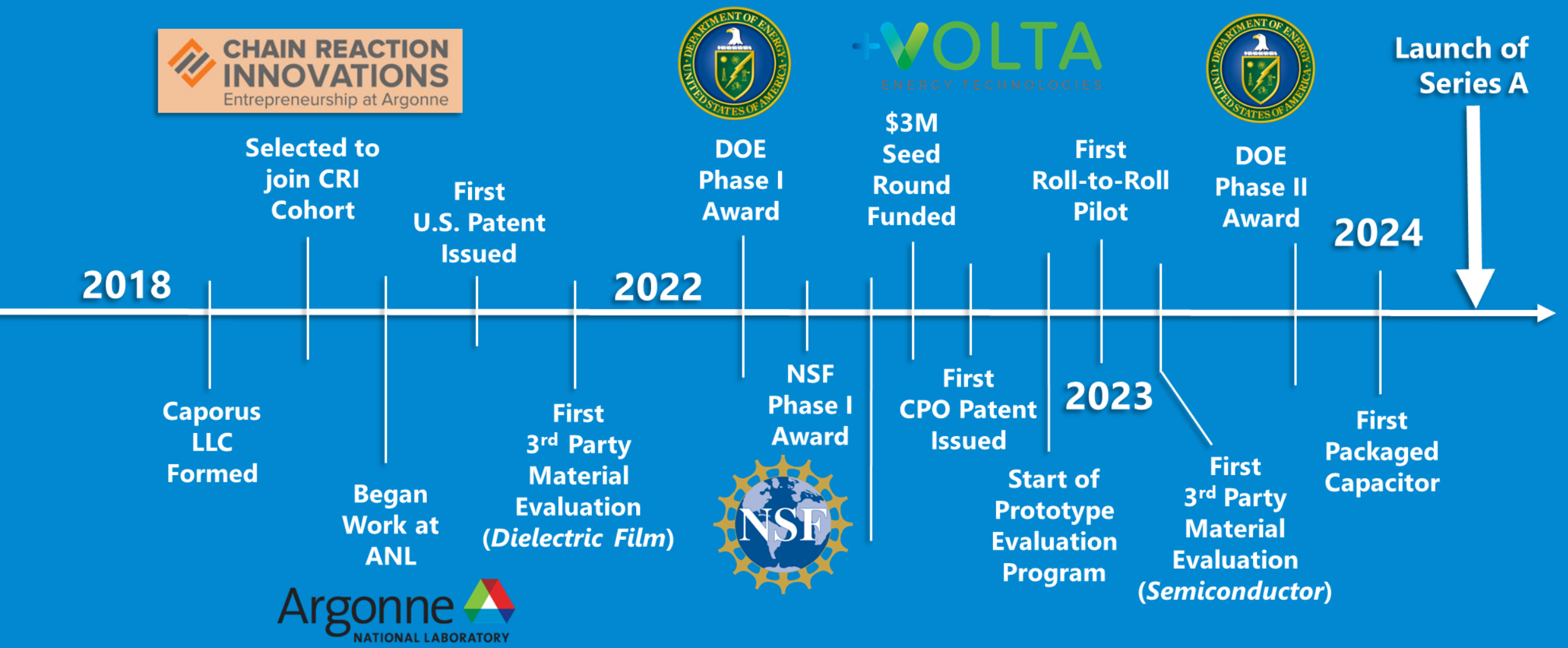
CHAIN REACTION INNOVATIONS
Entrepreneurship at Argonne

Caporus is located near Fermilab and Argonne in Southwest Chicagoland



Caporus was previously embedded at Argonne through the Chain Reaction Innovations program

Timeline and Milestones



Caporus | Team

BOARD OF DIRECTORS

Kevin O'Connor, PhD
Founder and CEO

David Schroeder
Chief Technology Officer
Volta Energy Technologies

Jim Cable
Former CEO
Peregrine Semiconductor

CAPORUS TECHNOLOGIES

Intro to Caporus & NLP™

Silicon on Insulator for NP

Phase II Demonstration

Silicon on Insulator (SOI)

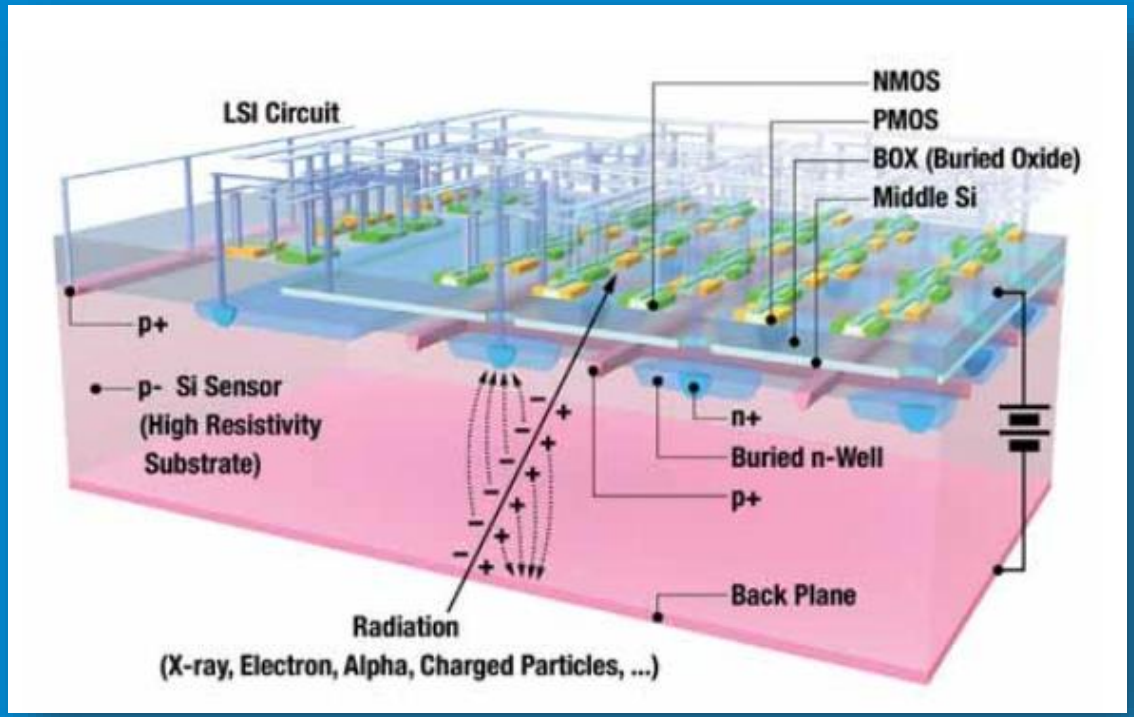
Commercial RF-SOI Substrate Structure

Image from SOITEC

SOI Advantages	SOI Disadvantages
Superior Single Event Upset Tolerance	Total Ionizing Dose Issues (Charge Effects)
Better Noise Isolation	Radiation Damage to BOX
Speed	Back-gate Effect due to Field Applied in Sensor
Density	Coupling of Charges in BOX and sensor

Improved SOI for MAPS

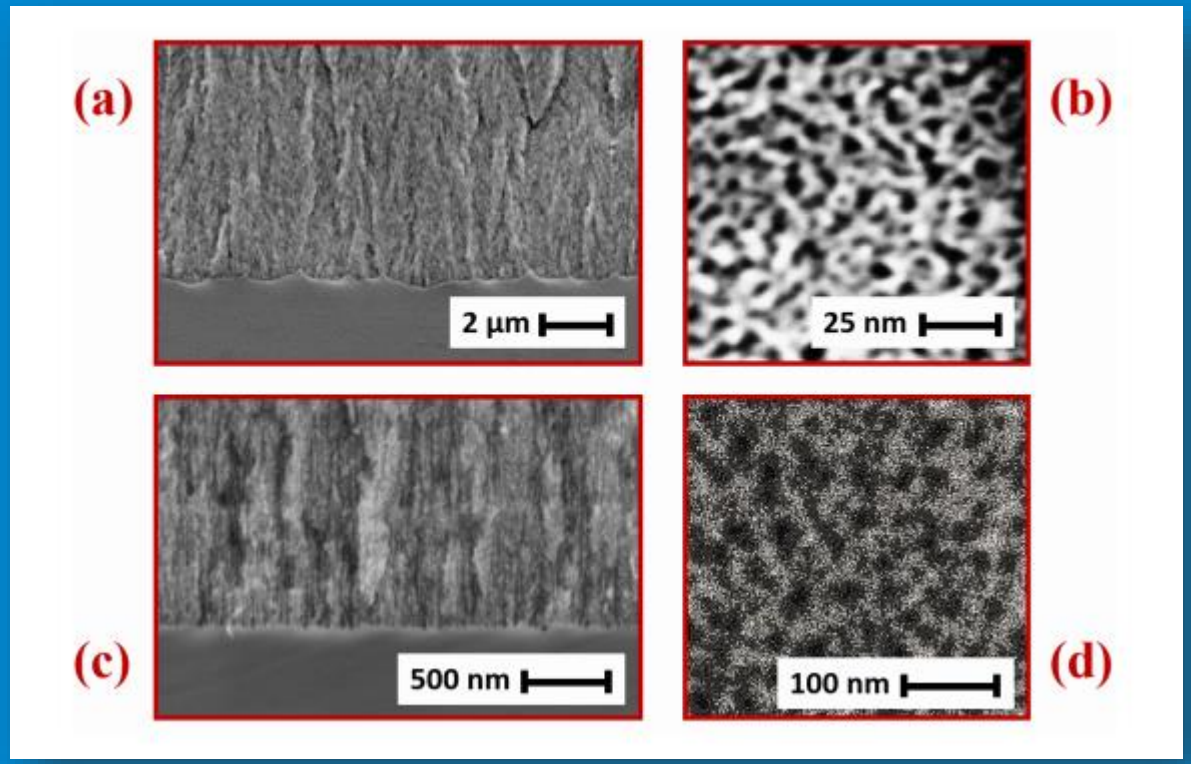
- Reduce unwanted coupling between substrate and front-end electronics
  - Reduced back-gate effect
  - Improve sensitivity
  - Reduce noise
- Improved radiation hardness
  - Lower radiation cross-section
  - Reduced coupling decreases effects of trapped charges
- Elimination of inversion layer effects
  - Enable depletion with applied electric field
  - Improve sensitivity



SOIPIX – 2016 KEK Annual Report

NLP | Porous Si SOI

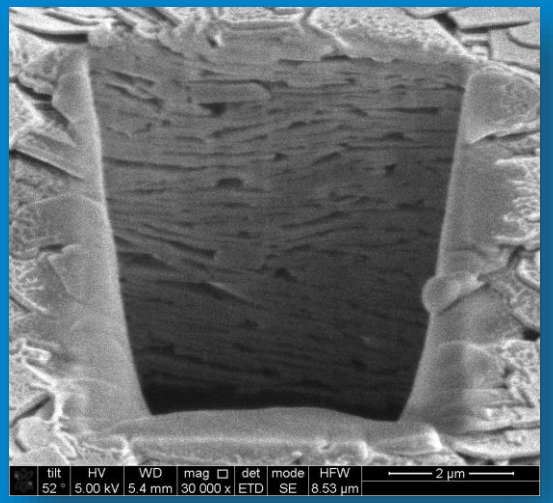
- Porous Si SOI
  - State-of-the-art in research
  - Porous Si layer between silica and silicon
  - Electrochemical etching of Si
    - Columnar porosity
- Advantages
  - Trap-rich and low dielectric constant
  - Record-high linearity (RF)
  - Reduced substrate noise, coupling and parasitics
- Disadvantages
  - Poor mechanical stability (>50% porosity)
  - Sometimes requires doped substrates to increase conductivity for electrochemical etching ($)

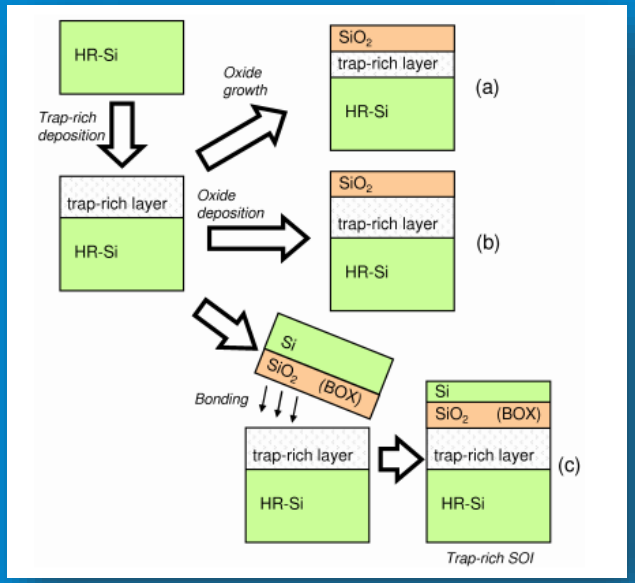


M. Rack, UCL Dissertation, 2021

NLP Porous Si SOI

- Advantages over Standard Si
  - High effective resistivity due to trap layers at pore interfaces
- Advantages over Trap-Rich SOI
  - Potential for record-high linearity
  - Reduced substrate noise coupling levels and associated parasitics
- Advantages over Porous Si
  - Equal or potentially lower effective permittivity
  - Lower porosity required for given effective permittivity – higher mechanical strength due to higher solid content
  - Higher mechanical strength due to pore structure – highly resistant to crushing/breaking from compaction
  - Compatible with any substrate resistivity (e.g. compatible with HR or std Si) – no need for low resistivity for electrochemical porosification
  - No need for post-processing to implement porosity (e.g. no etch-stop layers, patterning, etc.)





Intro to Caporus & NLP™

Silicon on Insulator for NP

Phase II Demonstration

Phase II Project Summary

- Priorities from Solicitation
  - Next generation of monolithic active pixel sensors (MAPS)
  - Radiation hardness (EIC luminosity of 10^{33} – 10^{34} $cm^{-2}s^{-1}$)
  - Apply E-field to substrate to fully deplete detection volume

- Proposed Technology
  - Implement MAPS on SOI
  - Improved single-event upset, better noise isolation, speed, and density compared to bulk process
  - Modified SOI with porous Si below BOX
    - Reduce capacitive coupling between Si layers (Lower ε_{eff} and greater non-BOX thickness of porous Si)
    - Reduce radiation cross-section of BOX and total ionizing dose effects
    - Eliminate parasitic conduction layer at interface of BOX and bulk Si (Trap-rich)

- Phase II Demonstration
  1. Scale processes for radiation testing
  2. Etching processes for porous layer
  3. Design CMOS and test structures
  4. Fabricate test devices
  5. Test for radiation hardness
     - With and without porous layer
     - As-received and after irradiation

Phase II Resources

Phase II Team

- Caporus Technologies
  - Kevin O'Connor (PI)
  - Nikki Chang
  - Karabi Mondal
  - Eric Acosta
  - Bill Fortino
  - Michael Boehme
  - Jim Cable (Consultant - SOI Development and Commercialization)
  - Francis Chapman (Consultant - Materials Development)
- Subaward
  - Fermi National Accelerator Laboratory
    - Farah Fahim, Davide Braga, and Xiaoran Wang (SOI – MAPS Design, Irradiation, Device Testing)

Additional Resources

- SkyWater (Vendor)
  - Device fabrication
- Foley and Lardner (TABA)
  - IP: USPTO and PCT applications
  - Contracts: Commercial engagement – pilot and license
- External Facilities
  - Center for Nanoscale Materials (CNM)
    - Liliana Stan and Ralu Divan (SciCon)
  - UChicago Pritzker Nanofabrication Facility
  - Northwestern NUFAB
- Carl Traynor (Consultant - Commercialization)

Asks from NP Community

- Addressing Vendor Schedule Risk
  - Availability of SkyWater RH90 process is delayed
  - Investigating alternatives for fabrication of test structures
    - CMOS processing on SOI substrates preferred

- Connections within DOE Community
  - End users of MAPS detectors
  - Detector development community

Contact

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oconnorka@caporus.com