Pacific MicroCHIP Corp.

A Multichannel DSP ASIC for Streaming Readout

DoE award number: DE-SC0022495
PI: Anton Karnitski
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OUTLINE

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- The company, its specialization/expertise
- Multichannel DSP ASIC description and improvements vs. previously designed ASICs
- Multichannel DSP ASIC operational capabilities
- ASIC core architecture for analog and digital part of the ASIC
- Output data frame structure
- ASIC layout integration
- Time-interleaving challenges
- Chip fabrication
- Characterization PCB design
- Power consumption and preliminary ADC performance testing results
- Phase II project schedule and future plans

COMPANY

Pacific MicroCHIP Corp. is incorporated in 2006. It is headquartered in Culver City, California. Main focus – providing IC/ASIC design services and turnkey solutions. The office includes the working space and a laboratory for ASIC testing.

Core expertise:

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (CMOS/SiGe) down to 7nm

MULTICHANNEL DSP ASIC

The designed ASIC include a digitizer block which is preceded by a 32-channel 12-bit 1GS/s ADC array.

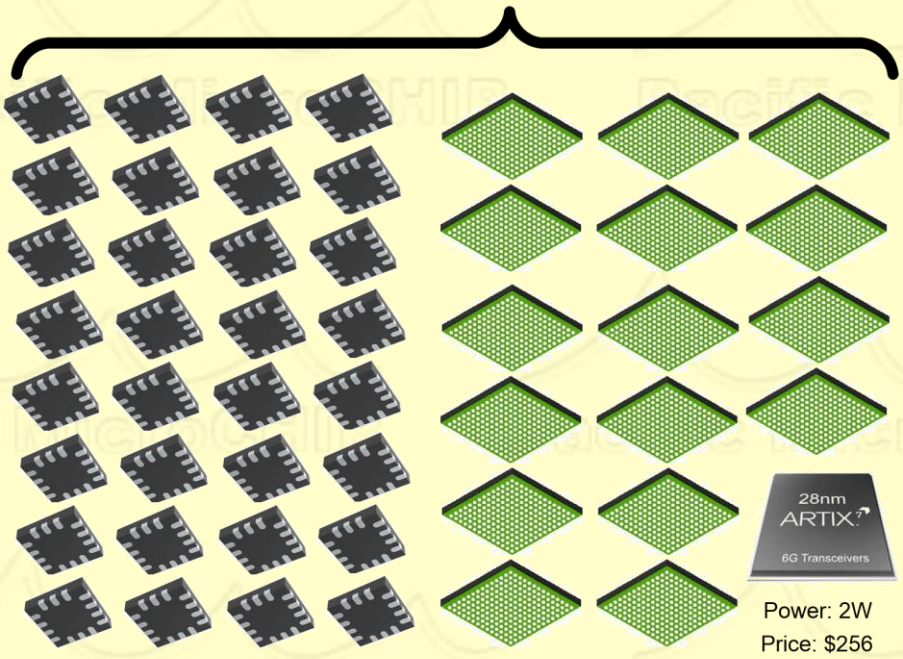
The digitized data is further processed in the DSP block which performs pulse shaping and event building, data serializing and shipping it out through a single lane high-speed interface.

Our ASIC will include a functionality equivalent to 32 ADC parts, 32 pulse shapers based on amplifiers and passive components, an FPGA and a great amount of wiring between these components

Applications:

- Readout of SiPMs used in calorimeters at the EIC
- Detector streaming readout
- Multichannel gamma-ray spectroscopy systems (DoE)
- X-ray detectors (DoE)
- CT systems, luggage, and cargo scanners
- Test and measurement instrumentation
- Multichannel data acquisition devices
- Synthetic aperture radars and lidars

Power reduction: 47.7W→3.5W
Price reduction: $4.5k→$1k
Size reduction: 33 times



Power: 2W
Price: $256

Part: TILMH3401

Per Part:
Price: $17.11
Power: 5V x 55mA=275mW
Total:
Price: $17.11 x 32= $547
Power: 275mW x 32 = 8.8W

Part: ADS54T04IZAYR

Per part:
Price $231 (1000parts)
Power =2.25W,
Total:
Price $231x16 = $3,696
Total power32x1.15W=36.8W

MULTICHANNEL DSP ASIC IMPROVEMENTS

A 32-channel 12-bit 0.5GS/s ADC was already developed within the DoE SBIR project DE-SC0017213. A 32-channel 12-bit 0.2GS/s ADC with event-driven digital backend was developed within the DoE SBIR project DE-SC0018566. For the proposed ASIC, the ADC array will be modified to increase the sampling rate to 1GS/s, while many blocks will be reused from already designed ASICs. This approach will reduce risk and effort which will turn into cost reduction

Major improvements vs. previously designed ASICs:

- Increased ADC sampling rate up to 1GS/s
- The DSP block will use proven algorithms to provide a rate capability exceeding 3 Mega-events per second per channel.
- Waveform capture (pre- and post-event);
- Increased JESD output data throughput up to 16Gbit/s
- DSP power down mode
- Improved 28nm TSMC HPC+ CMOS process

A FLOW CHART FOR THE PHASE II PROJECT

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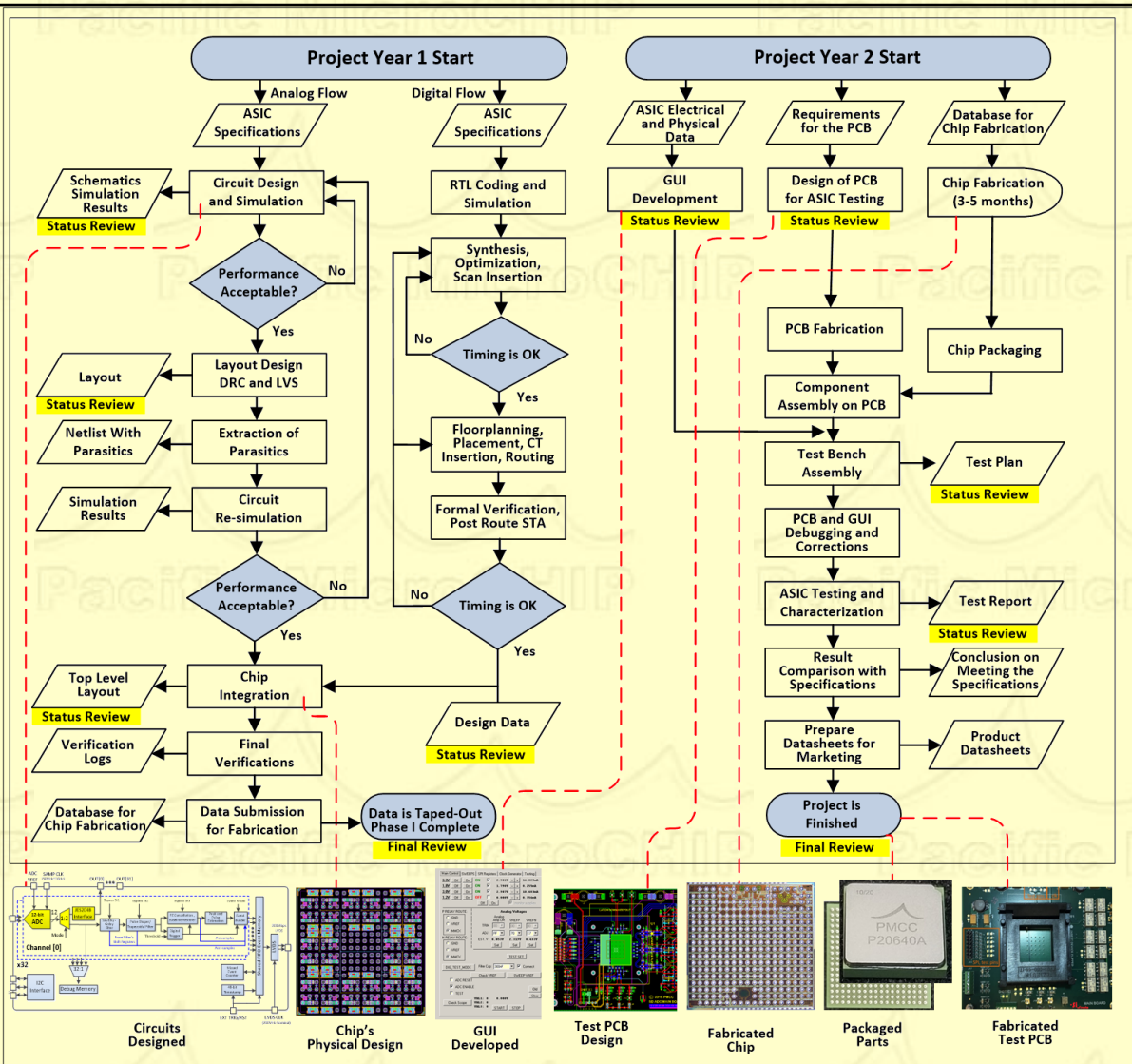
During the project year 1:

- Completed the ASIC's circuit level (analog and digital) design
- Design the layout, optimize the circuit performance
- Integrate the circuits and the layouts to assemble the complete ASIC
- Perform comprehensive simulations and verifications
- Submitted to the foundry for fabrication.

During project year 2:

- The ASIC prototypes are fabricated and packaged.
- The test board will be designed, fabricated and assembled.
- The test bench will be set up, a GUI for automating of the ASIC's testing will be developed
- Characterization and testing of the ASIC will be performed.
- The documentation for the ASIC's commercialization will be prepared.



A MULTICHANNEL DSP ASIC OPERATIONAL CAPABILITIES

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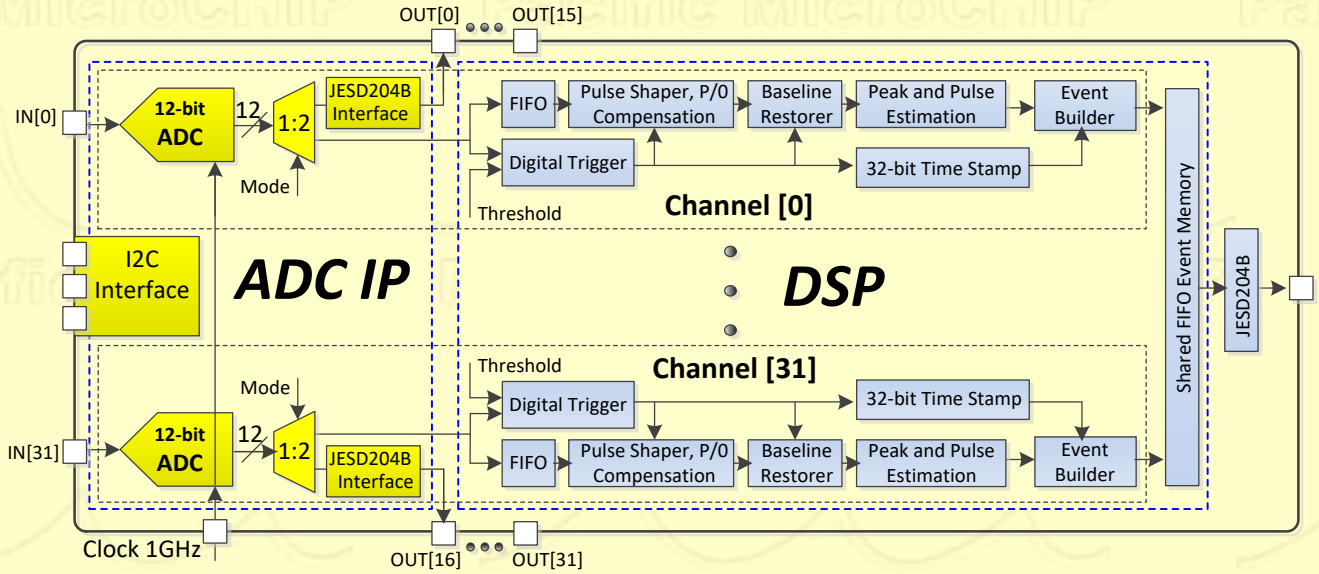


ADC IP:

- 32 independent channels, 12-bit 1GS/s
- Programmable sampling rate of 1 / 0.5 / 0.25 GS/s;
- 0.9Vppd input voltage swing with Input signal BW > 0.5GHz;
- JESD204B+ standard compliant output data interface;
- I2C interface for ASIC control.
- Extended temperature range -40…125C (junction).
- Built-in temperature sensor
- Power consumption of 110mW per channel.
- TID tolerance >10Mrad.
- 15mm x 15mm 324 ball BGA package.

A DSP block for:

- Digital filters for pulse shaping;
- Baseline restoration.

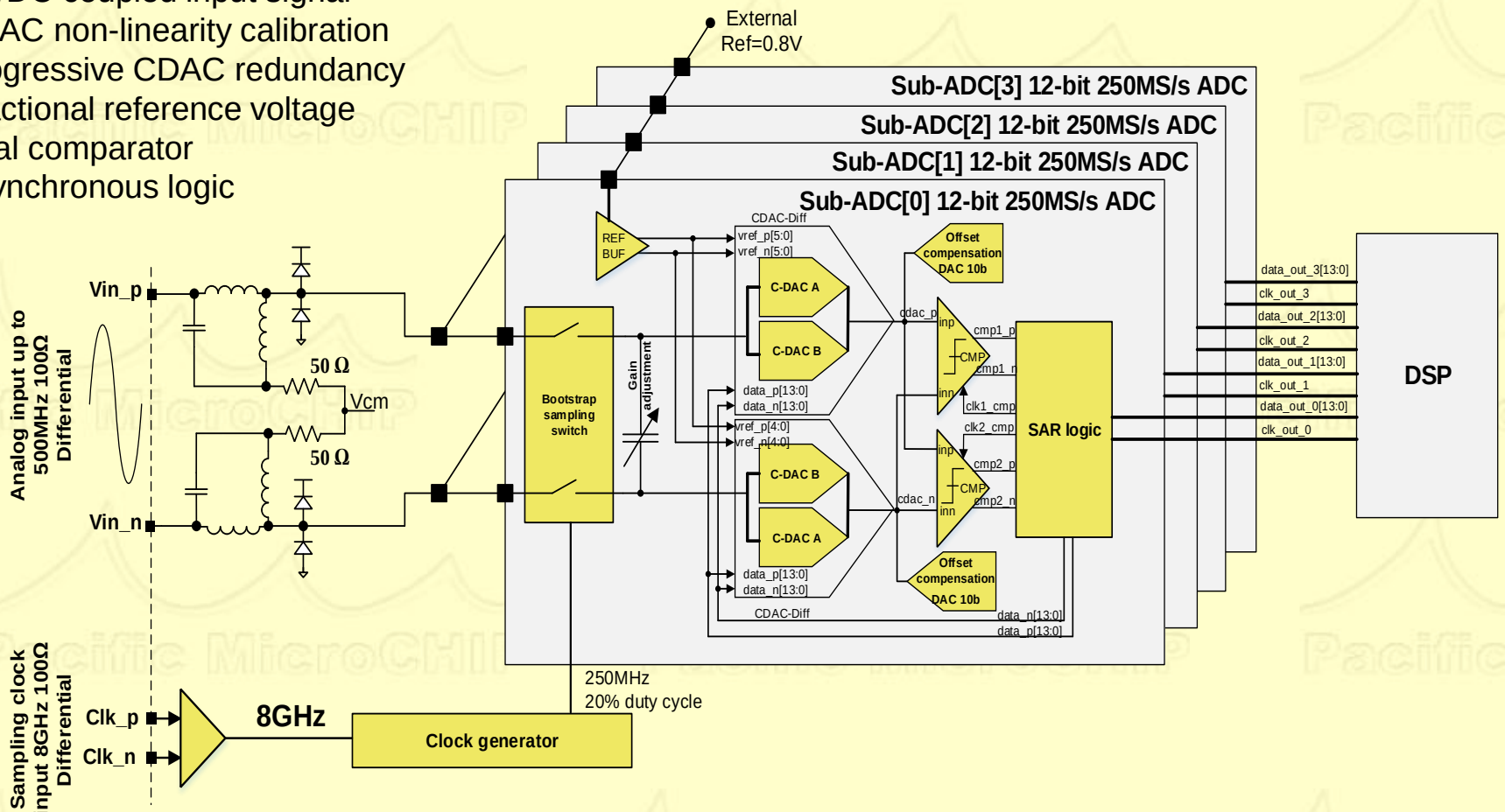
Event builder function:

- Automatic triggering, timestamping;
- Digital detection of pulse time-to-peak, duration and amplitude;
- Event building, >3M events per channel per second;
- Waveform capture (pre- and post-event);
- JESD204B+ interface for data output.

ADC CORE ARCHITECTURE

Features:

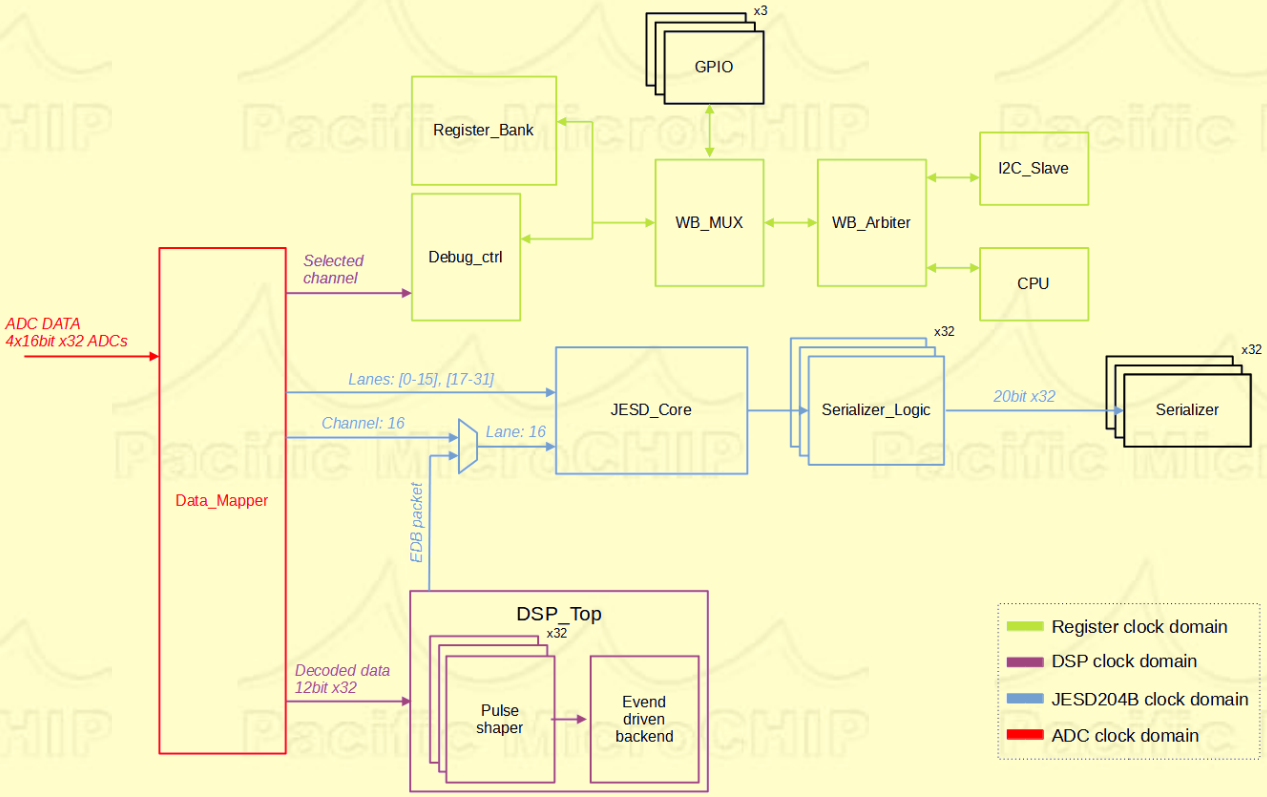
- 12b 4 x time-interleaved SAR ADC architecture
- AC/DC coupled input signal
- CDAC non-linearity calibration
- Progressive CDAC redundancy
- Fractional reference voltage
- Dual comparator
- Asynchronous logic



BLOCK DIAGRAM OF DIGITAL BLOCKS

There are 4 main clock domains:

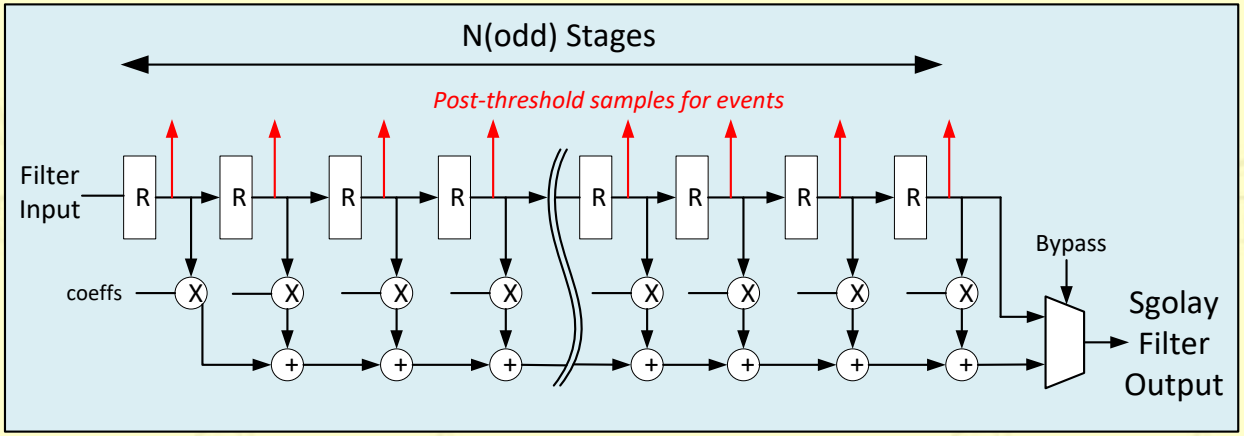
- DSP clock domain (1GHz) – Main clock domain for the DSP function
- JESD204B clock domain (800MHz frame clock) – Clock for data transfer using JESD204b interface. This frame clock frequency allows to achieve 16Gbps line rate.
- ADC clock domain (4 phases shifted clocks @ 250MHz) – Used to capture data coming from ADC and synchronize them to DSP/JESD204b clock domains.
- Registers clock domain (125MHz) – low frequency clock for control and debug functions.



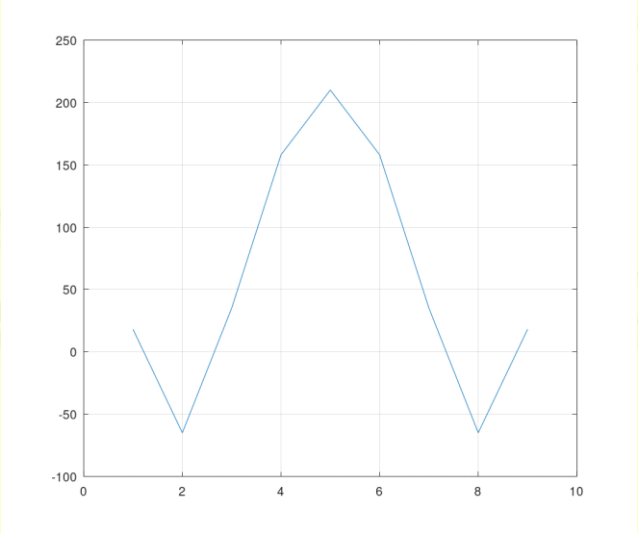
SAVITZKY-GOLAY FILTER

- The Savitzky-Golay filter is used to smoothen the input data without distorting the signal.
- It is implemented as a FIR Filter with length 9.
- Since the coefficients are symmetrical, only 5 are stored in registers.
- A bypass option has been added in the case when the filtering is not required, or when raw ADC sample events are desired.
- The samples for the post-threshold section of the sample events will be recorded based on the shift register within the filter.

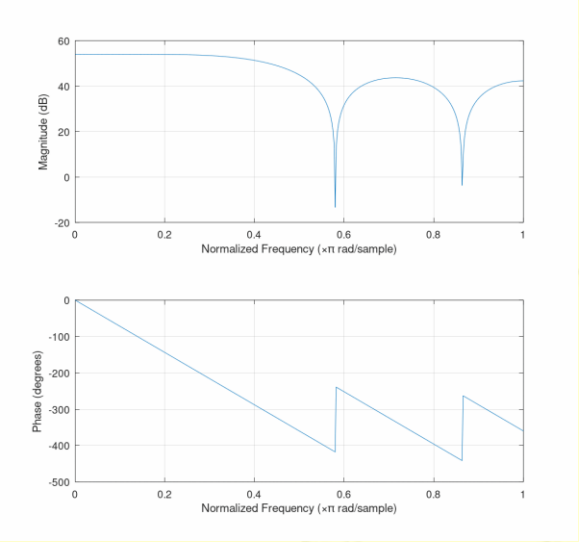
Block diagram of an FIR filter implemented as a Savitzky-Golay filter



Filter coefficients



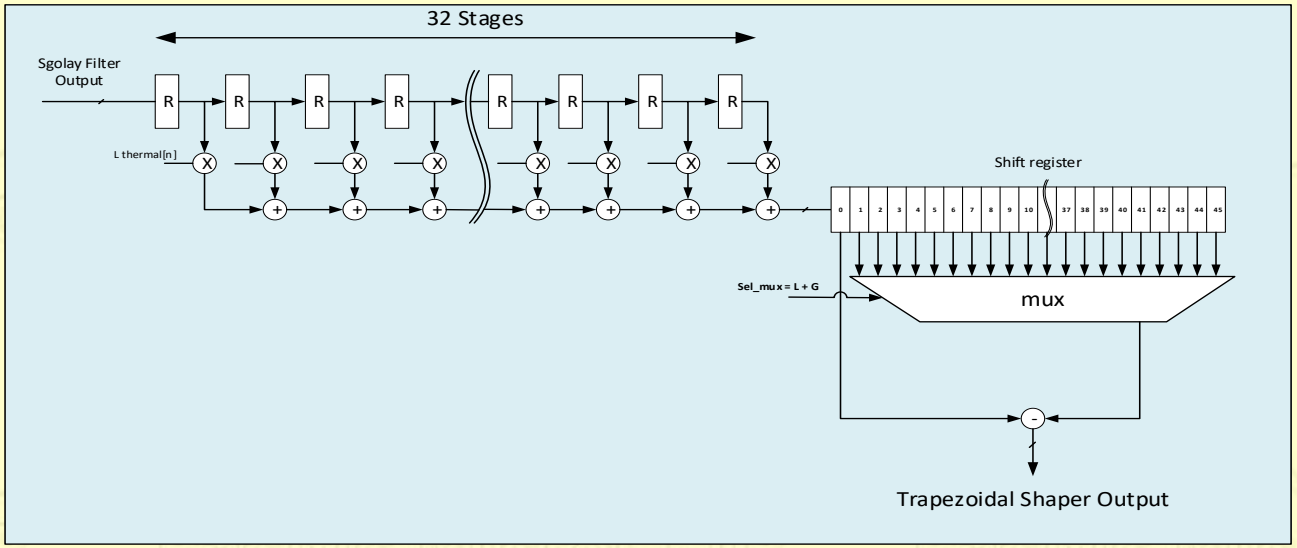
AC response



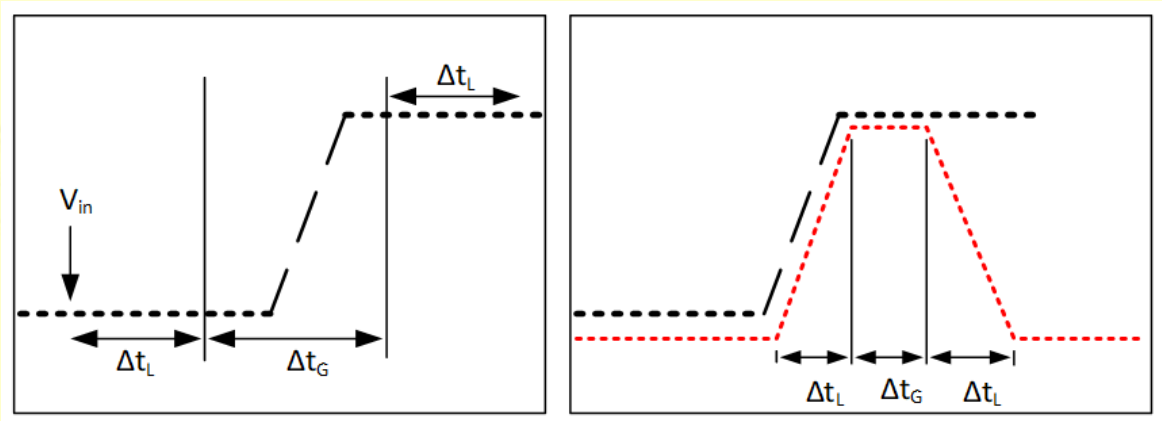
TRAPEZOIDAL FILTER

- The trapezoidal filter shapes the preamplifier output into a trapezoidal shaped output hence the name.
- Shaping the input signal pulses into trapezoidal pulses improve the accuracy of pulse width and height measurements.
- The trapezoidal filter has two configurable parameters, Length (L) and Gap (G).The maximum L and G values are limited to 31 and 15 respectively.

Trapezoidal filter architecture



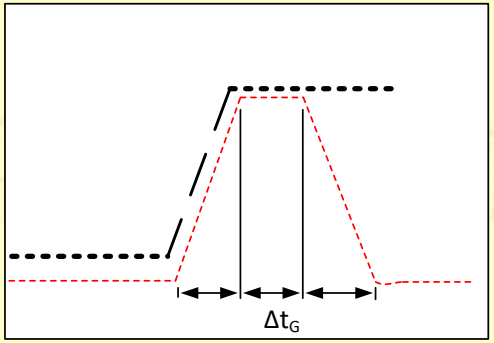
Trapezoidal Filter Parameters (left) and Representative Output (right)



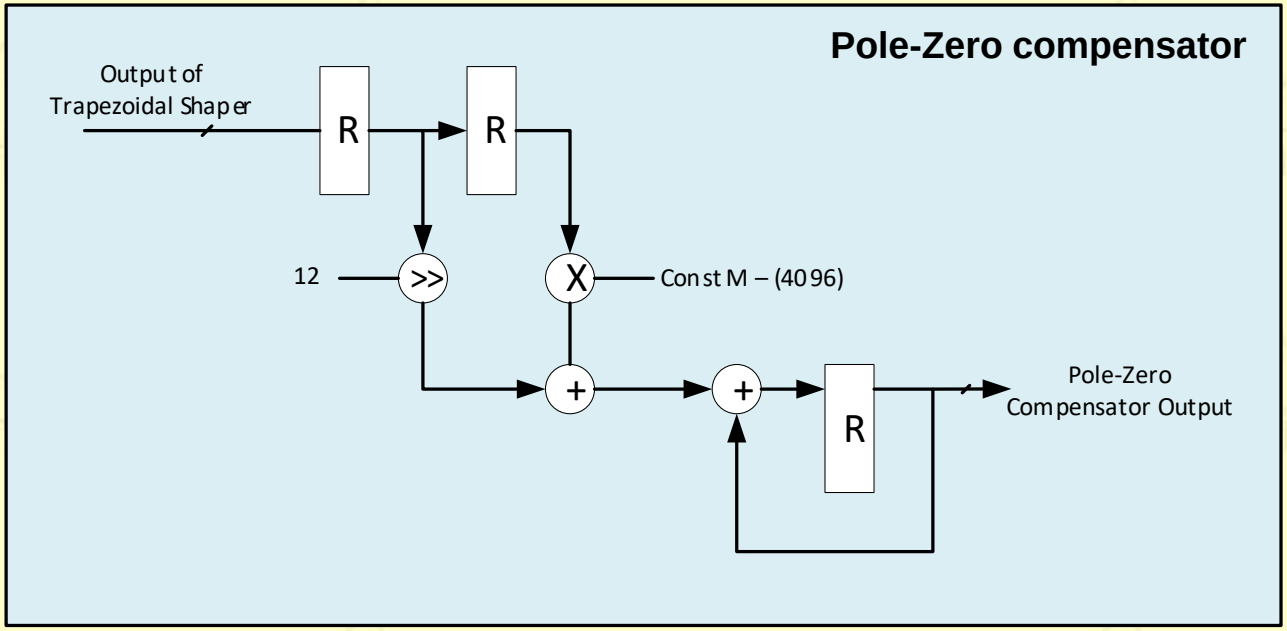
POLE-ZERO COMPENSATION

- The trapezoidal filter can produce an undershoot at its output. This is caused by the differentiator in the trapezoidal filter when the L sum during the pulse is higher compared to the L sum after the current pulse peak.
- A pole-zero cancellation block is implemented in order to correct for this decay.

Trapezoidal Filter output with undershoot



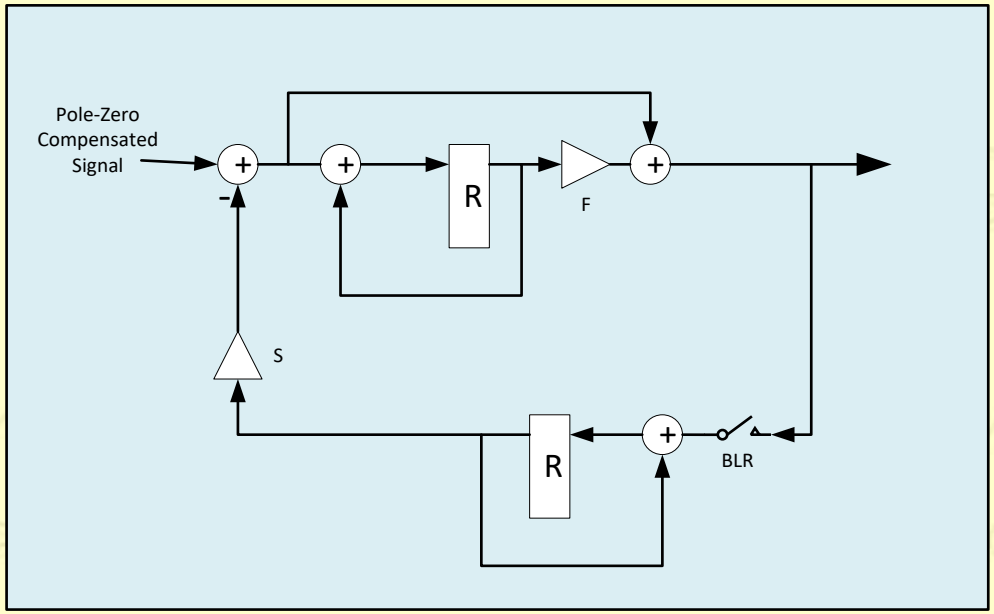
- The pole-zero coefficients can be tuned to support a variety of external CSAs which have variable RC delays (tau), and this is done by adjusting the “Const M" coefficient shown in the block diagram.



BASELINE RESTORATION

- One consequence of canceling the tail (long decay) of the CSA input pulse is the need to restore a constant baseline to the signal.
- The baseline restoration algorithm is implemented as a gated low-pass digital filter at the output of the trapezoidal filter. The baseline filter uses a gated integrator structure to avoid distortion while the system is processing a pulse.
- The digital trigger generates the gate signal which disconnects the feedback accumulator for the Baseline restorer. It is produced by comparing the output of the trapezoidal filter with a user-defined threshold, and once the threshold is exceeded, the trigger is pulsed for the duration of the input pulse width.
- The S and F coefficients are configurable and provide fine tuning for restoring the baseline.

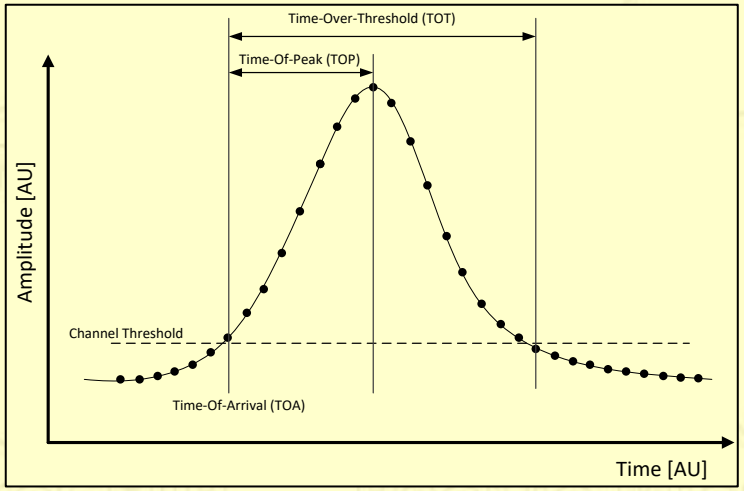
Baseline restorer



PRE- AND POST-PEAK SAMPLING

An event builder back-end (reused from DE-SC0018566) was modified to include signal samples of pre- and post-threshold and pre- and post-peak.

Event-driven backend recorded data



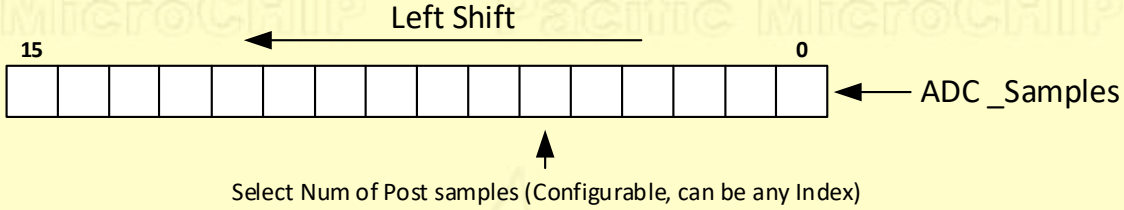
Capture pre- and post-threshold samples. (Mode 2'b11)

- Pre- and post-threshold samples are captured.
- The number of pre-threshold samples is configurable and can be up to 15. The number of post-threshold samples would be 16 minus the number of pre-samples.

Capture pre- and post-peak samples. (Mode 2'b10)

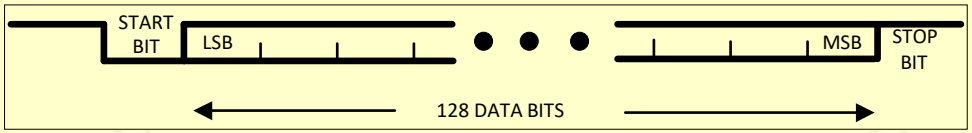
- Pre- and post-peak samples are captured.
- The number of pre-peak samples is configurable up to 15. The number of post-peak samples would be 16 minus the number of pre-samples.

Both modes use a shift register to capture the samples. The ADC data to the DSP block is shifted continuously through the register until the threshold is crossed. Once the threshold is crossed, the shift is limited to the number of post samples requested.



OUTPUT DATA FRAME

Bits	Field Name	Comment
[127:124]	Tail	Tail bits to fill JESD204b frame. Always 0
[123]	Parity	Parity bit used to monitor integrity of data transmission. Bit is high if number of high bits (excluding the parity bit) in event is odd.
[122]	Event Declaration	0 → test event (see text) 1 → normal
[121:120]	Fixed	In normal mode, always 2'b01 (bit 121 = 0, bit 120 = 1)
[119:107]	Window Interval	Setting for **window_interval[11:0]** corresponding to this event.
[106:102]	Channel ID	5-bit unique identifier for each ADC channel on the ASIC.
[101:54]	TOA	Time-of-Arrival. This is the time-stamp of where the ADC value passed the threshold. A 48-bit timestamp covers about 3 days at a 1G clock rate.
[53:42]	TOP	Time-of-Peak. To reduce the event size, the TOP is the 12-bit offset from the TOA. Using 10 bits supports shaper peaking times of up to 1 µs at a 1000 GHz clock rate.
[41:30]	TOT	Time-over-threshold. To reduce the event size, the TOT is a 12-bit offset from the TOP. Using 12 bits supports shaper pulse widths of at least 1 µs at a 1 GHz clock rate.
[29:18]	Peak Value	12-bit Peak Value recorded in the event.
[17:6]	Channel Threshold	12-bit threshold value used during this event.
[5:0]	Shared FIFO usage	The 6-bit FIFO usage when this event was placed in the Shared FIFO. Useful for diagnostics and debugging.



16Gbps / 128bit / 32ch * 0.8 ≈ **3.1M** events per second per channel **vs 12.4k for DE-SC0018566**
(250 times more captured events!)

DIGITAL PART OF THE DESIGNED ASIC

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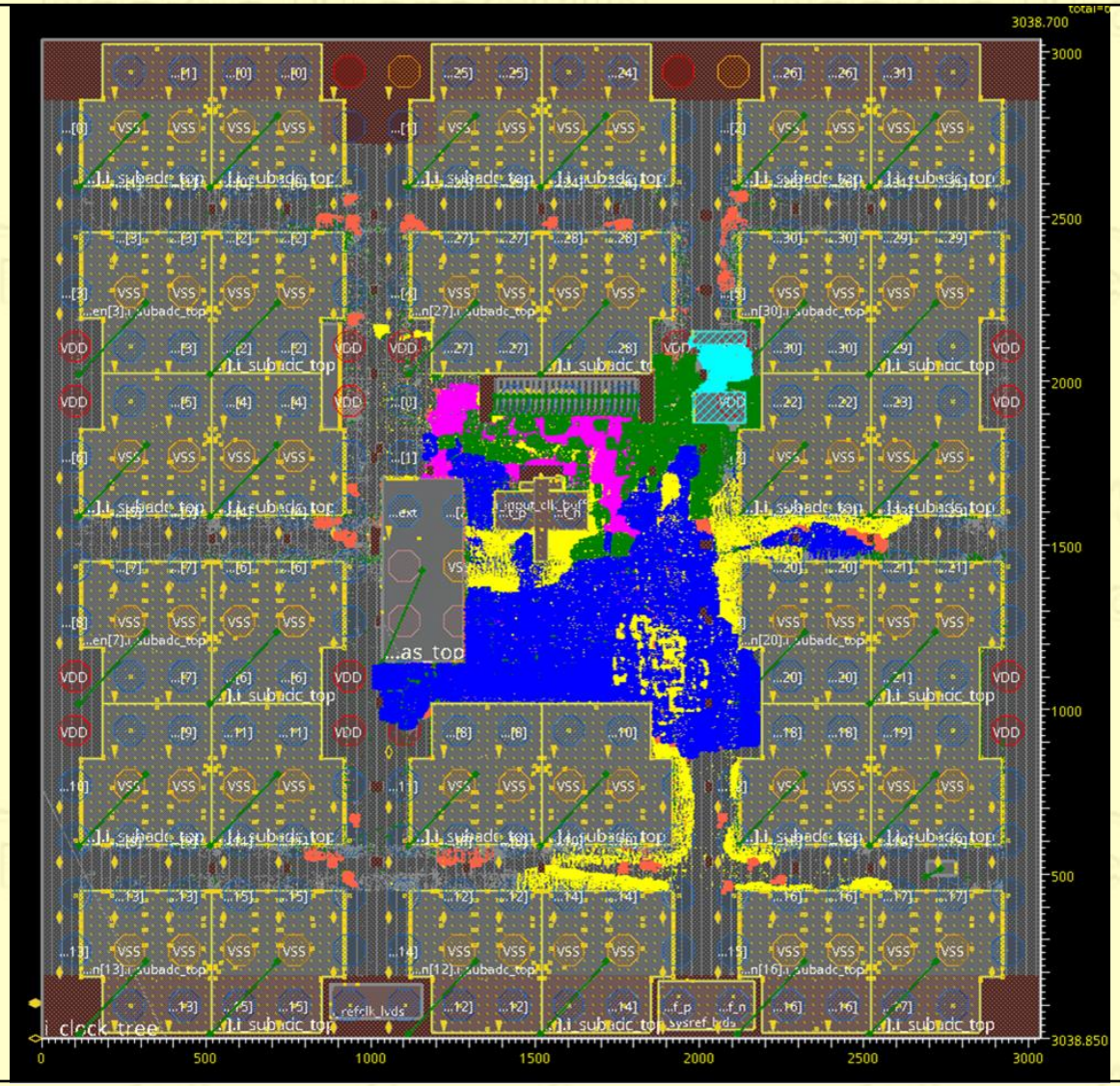
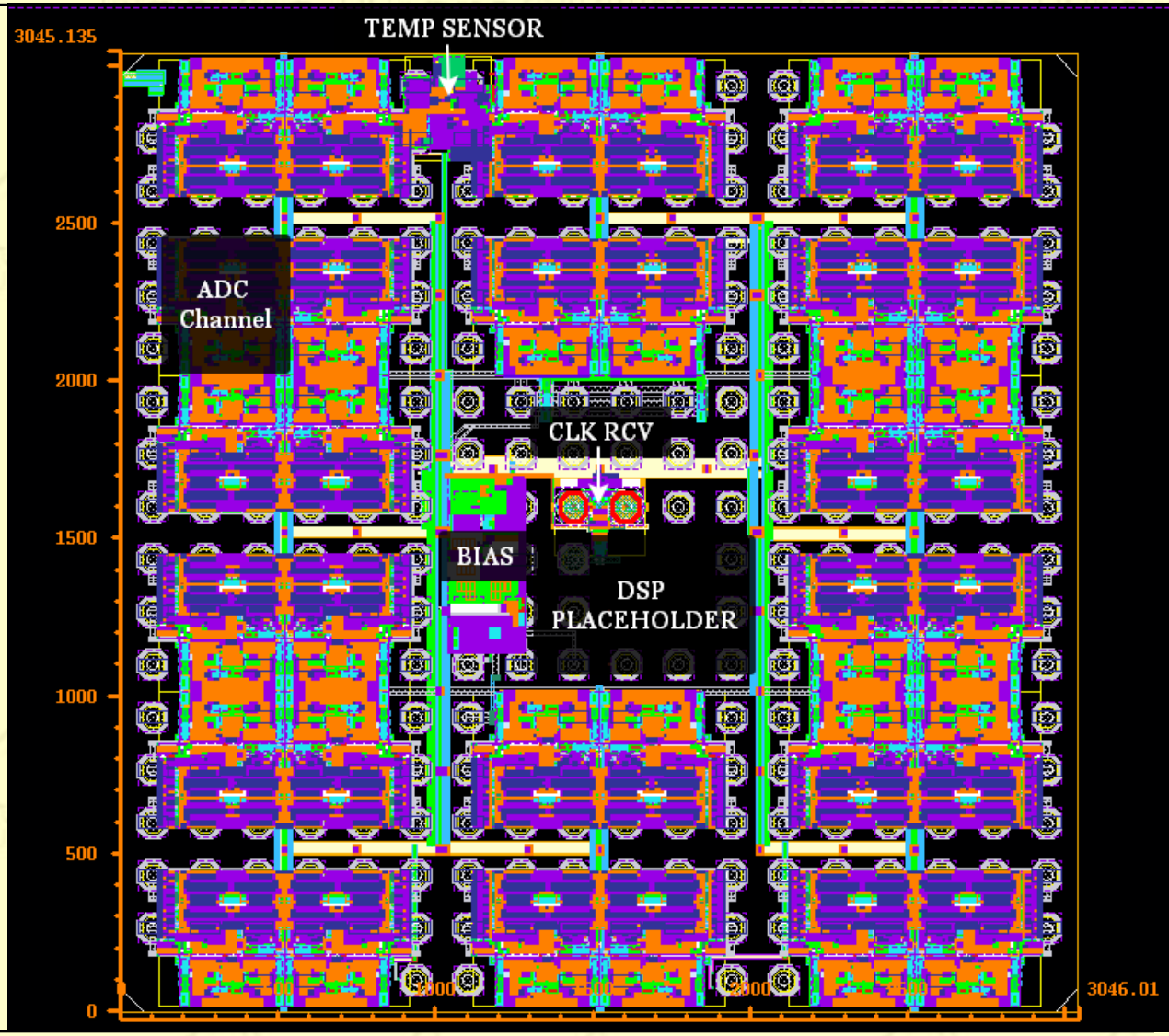
Arrangement of DSP block, an I2C interface, control registers, data mapper, JESD output data interface core and built-in RISC CPU for calibration purposes.



ANALOG PART OF THE DESIGNED ASIC

- The 32 ADC channels are symmetrically positioned around the central area.
- This floorplan of the chip generally follows the floorplan of our previously designed 32-channel ADC ASICs
- Integrated temperature sensor
- External clock source (F=8GHz)
- JESD204B+ interface for DSP data output



ADC LAYOUT COMPARISON

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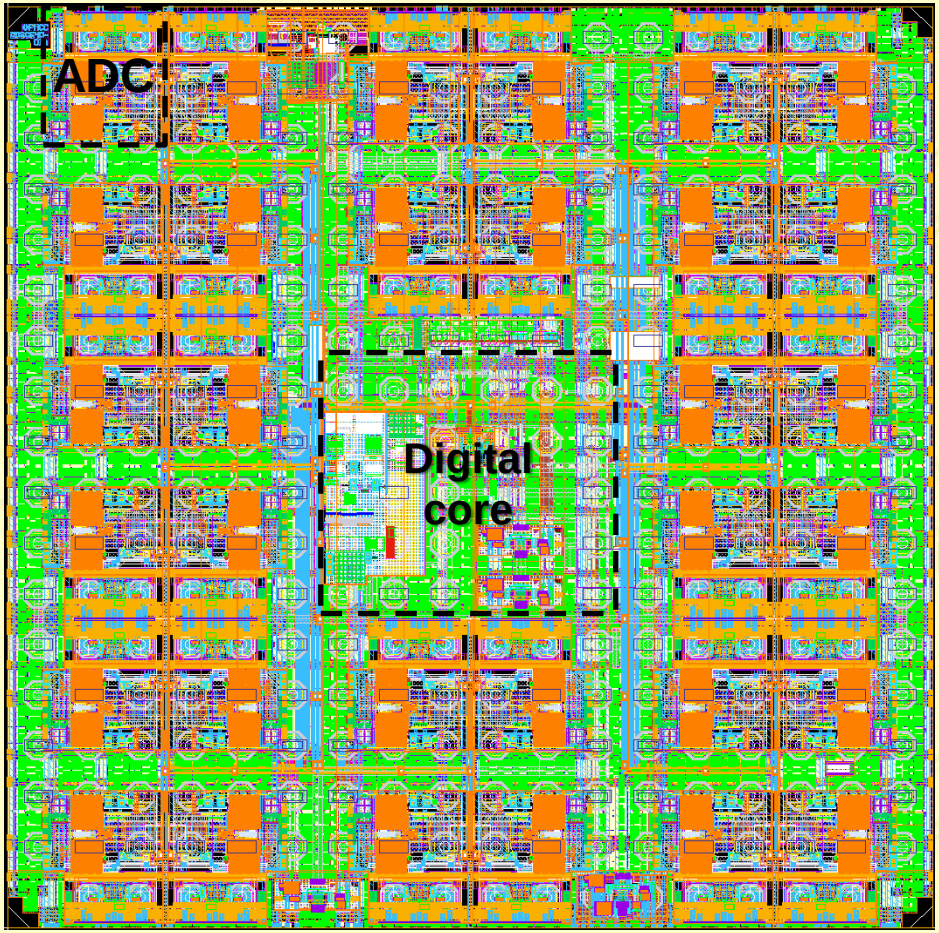
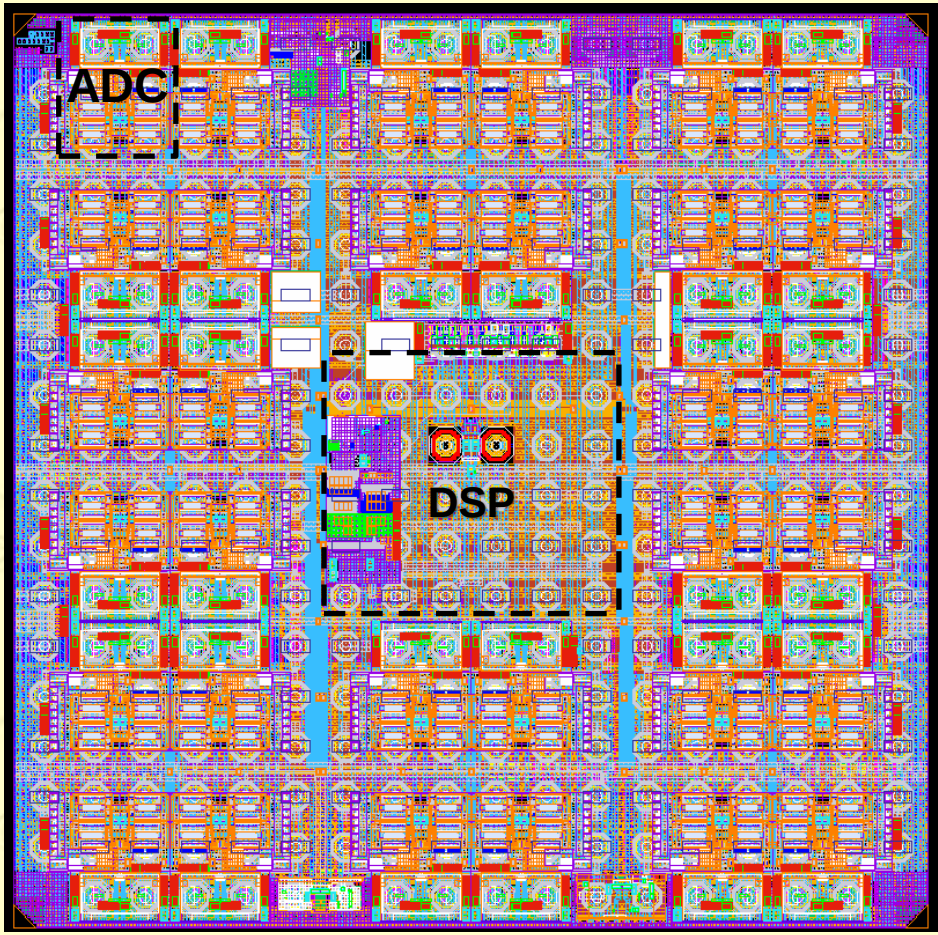
Overall chip floorplan is similar with DE-SC0018566





"The devil is in the details!": 5 times more data should be routed from each ADC to the DSP. Clock distributed to the channels is 2.5 times higher (3.2GHz -> 8GHz)

TIME-INTERLEAVED ADC

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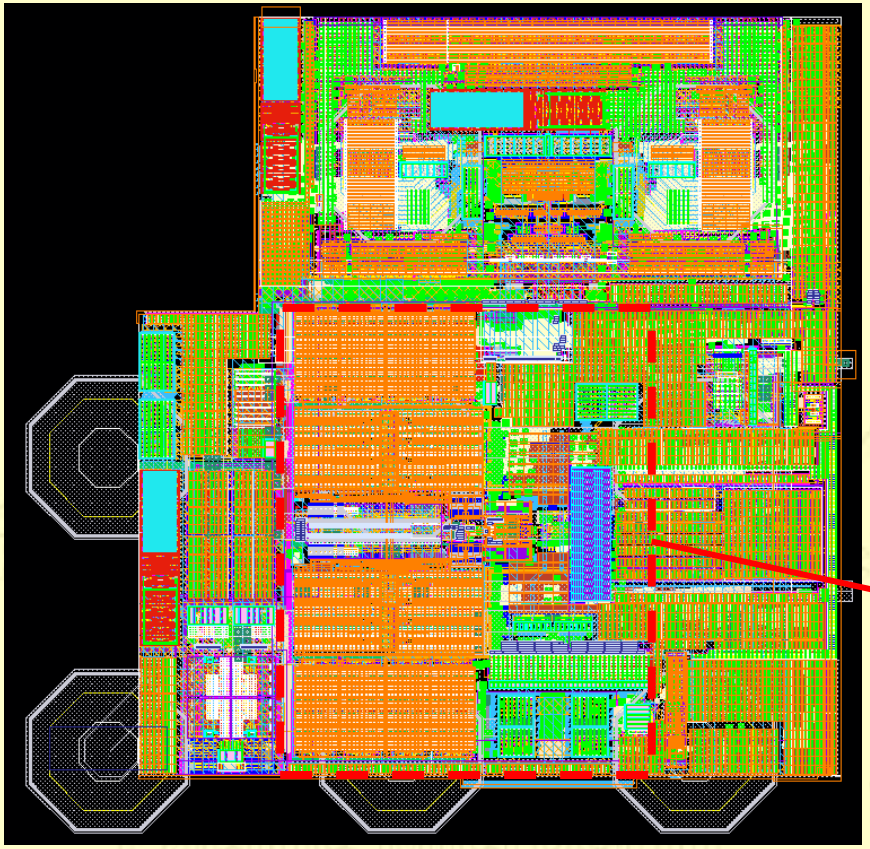
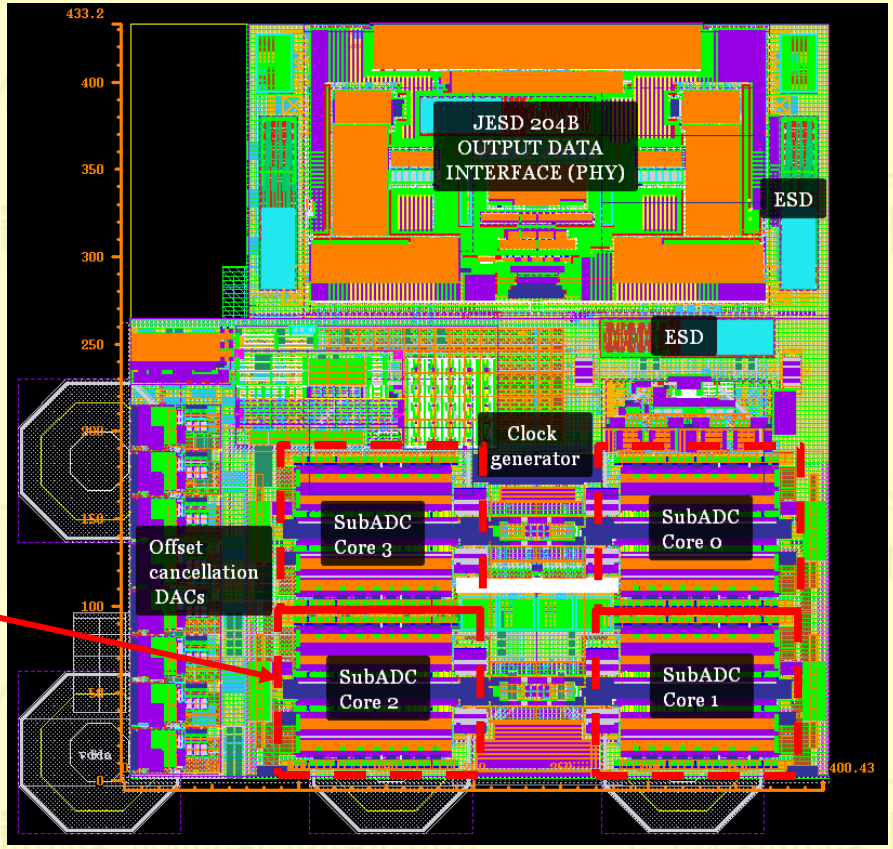
DE-SC0018566:12bit 200MSps ADC



DE-SC0022495:12bit 4 x 250MSps TI-ADC



For the same area: Single ADC core sampling rate increased by 20%. ADC core area significantly decreased allowing us to place 4 ADC cores and fit time-interleaved ADC related calibration circuits (gain and skew calibrations, 4 x offset cancellation DACs). JESD output data interface speed increased from 6.4Gbit/s up to 16Gbit/s.

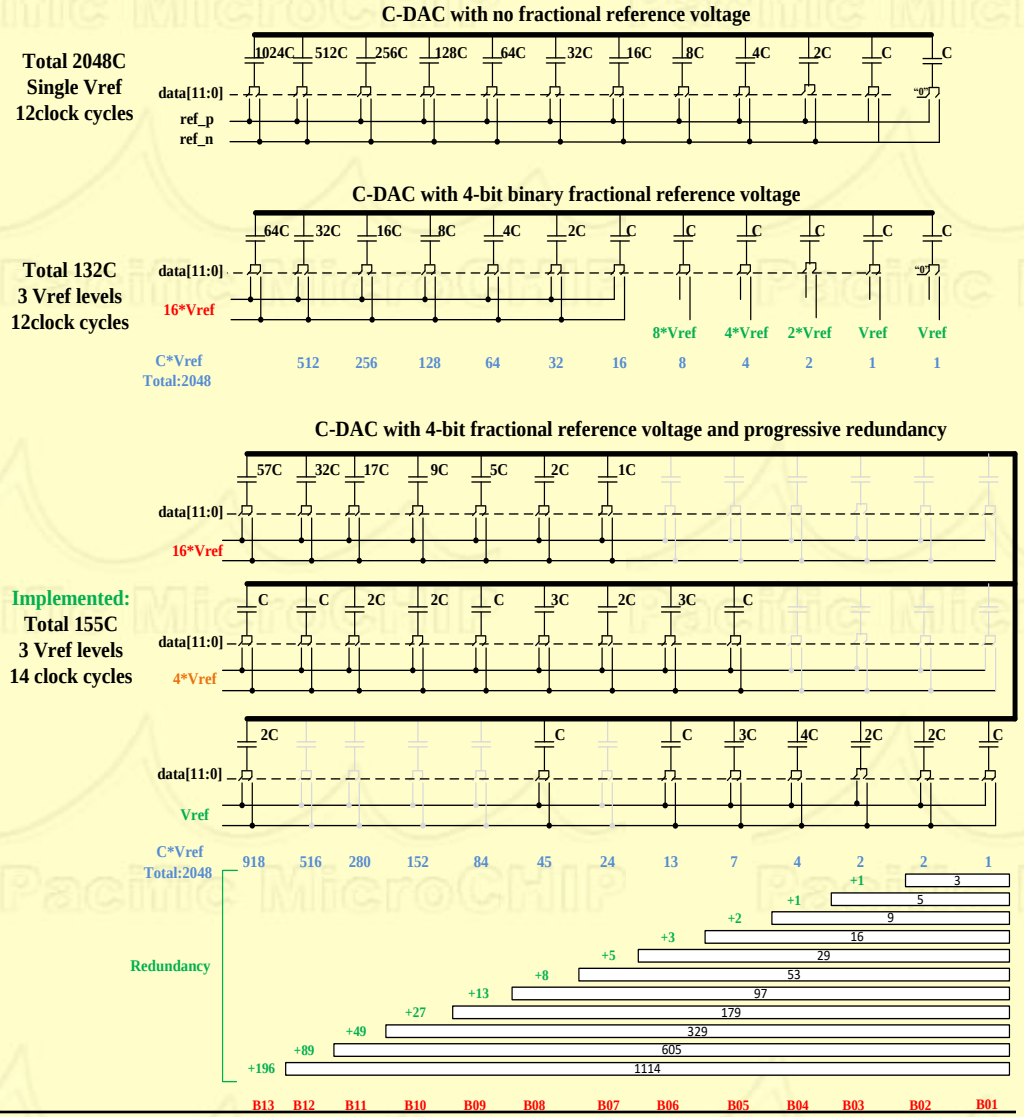
MODIFIED CDAC STRUCTURE

- By incorporating two additional reference voltage levels (Vref/4 and Vref/16), we significantly reduce the number of unit capacitor cells within the CDAC from 2048 in regular binary weighted CDAC to 155 cells in our design.

- This reduction of cell count results in decreased layout area of the total CDAC. At the same time, the matching between capacitors improves (ratio between MSB and LSB caps is reduced from 1024 down to 60).

- Furthermore, instead of using a binary weighted CDAC, we employ custom capacitor ratios, with progressive redundancy that scales proportionally with the capacitor value.

- Redundant CDAC helps to mitigate noise-related errors and relaxes the CDAC voltage settling requirements. This enables us to increase the sub-ADC sampling rate up to 250MSps.



CHIP FABRICATION

The Multichannel DSP ASIC for Streaming Readout of NP detectors was **taped out on March 12, 2024.**

As planned, **100 chips were fabricated** using the TSMC's 28nm HPC+ CMOS technology,

The dies were **received from the foundry** in two waffle packs **on 06 of June, 2024**.

ASSEMBLED PART

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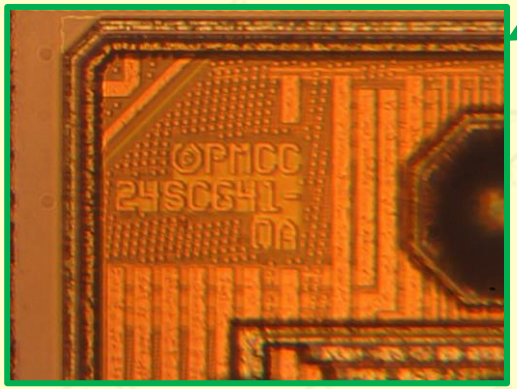
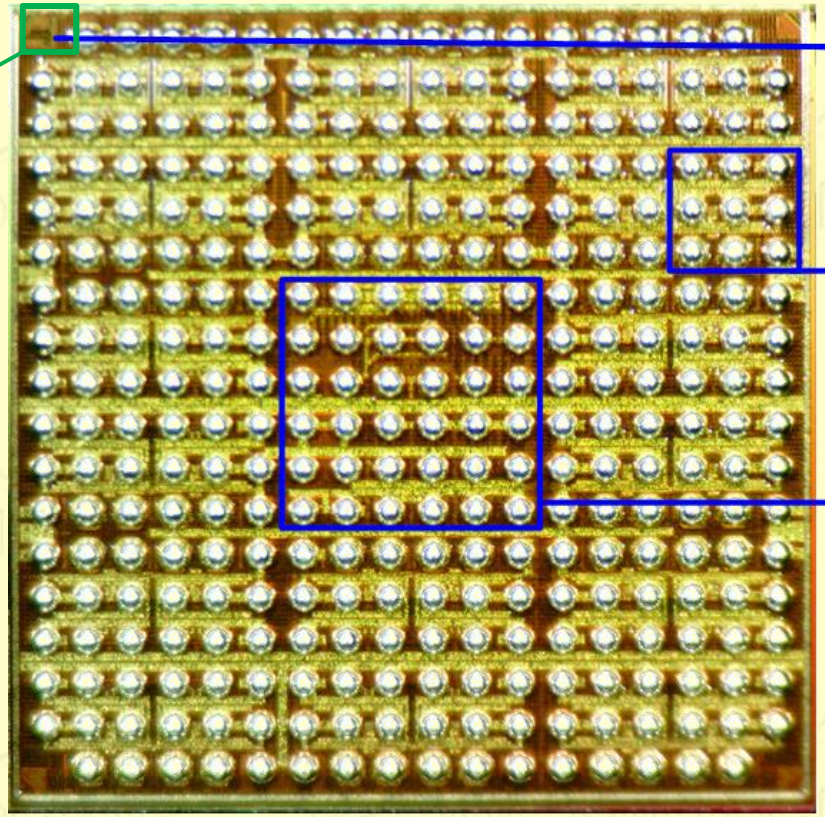
ASIC label
@PMCC24SC641-0A



ASIC die



The chip dimensions: 2.8mm x 2.8mm
Total chip area: 7.84mm²
320 bumps located at a pitch of 150.3um

CHARACTERIZATION PCB DESIGN

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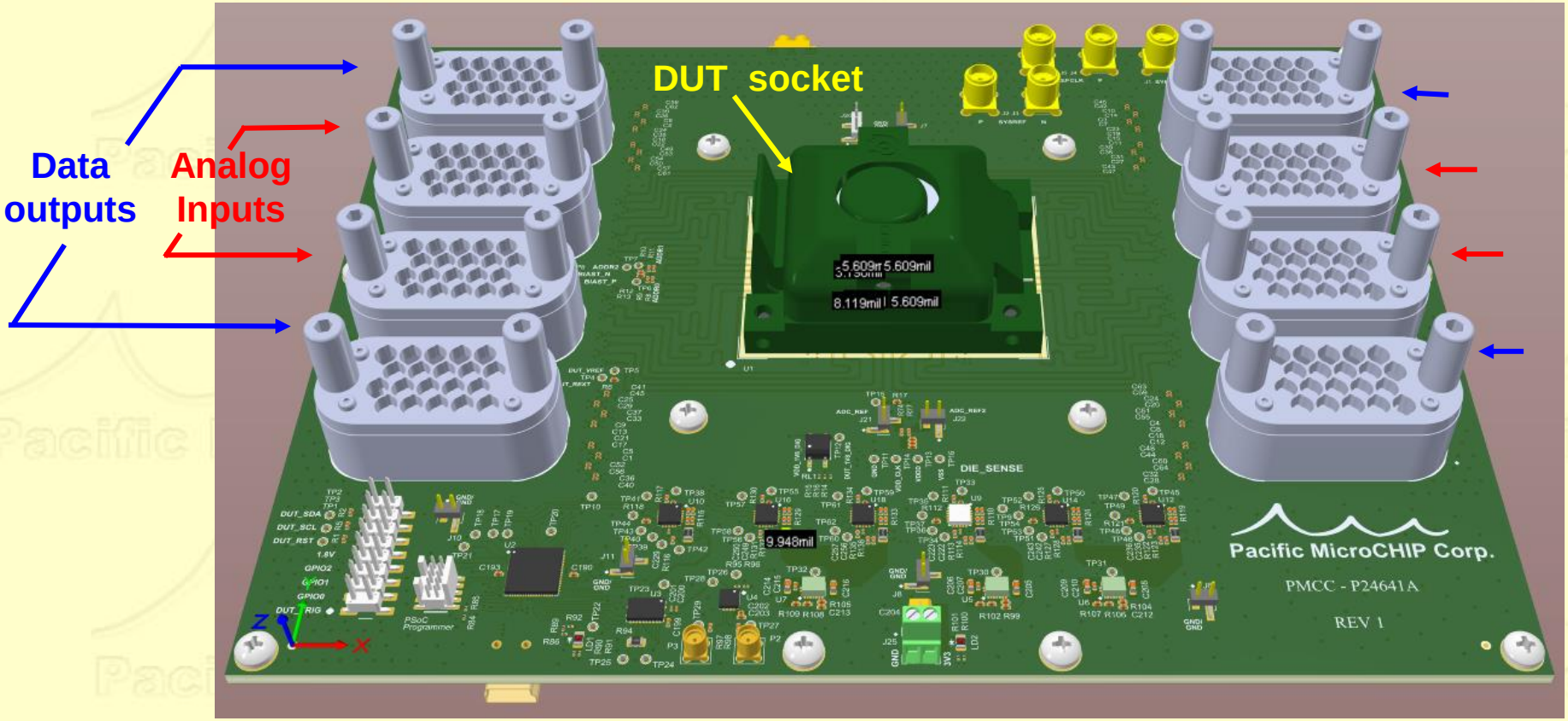
3D rendering of the designed PCB



- Samtec's Bulls Eye connectors used to handle analog input signal / output data
- Dimensions 5.6 x 7.7 inches

ASIC POWER CONSUMPTION

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32 ADC channels enabled
JESD204 output data interface **disabled**

	V [V]	I [mA]	P [mW]
VDDD	0.9	810	729
VDD18	1.8	0	0
VDDA	0.9	1040	936
VDDCLK	0.9	840	756
VDDIO	1.2	0	0
VDDVREF	1.2	560	672
			3093

Average power **96.6mW / ch**

32 ADC channels enabled
JESD204 output data interface **enabled**

	V [V]	I [mA]	P [mW]
VDDD	0.9	880	792
VDD18	1.8	0	0
VDDA	0.9	1040	936
VDDCLK	0.9	840	756
VDDIO	1.2	336	403.2
VDDVREF	1.2	560	672
			3559.2

Average power **111.2mW / ch**

TESTING RESULTS: SINGLE ADC CORE PERFORMANCE

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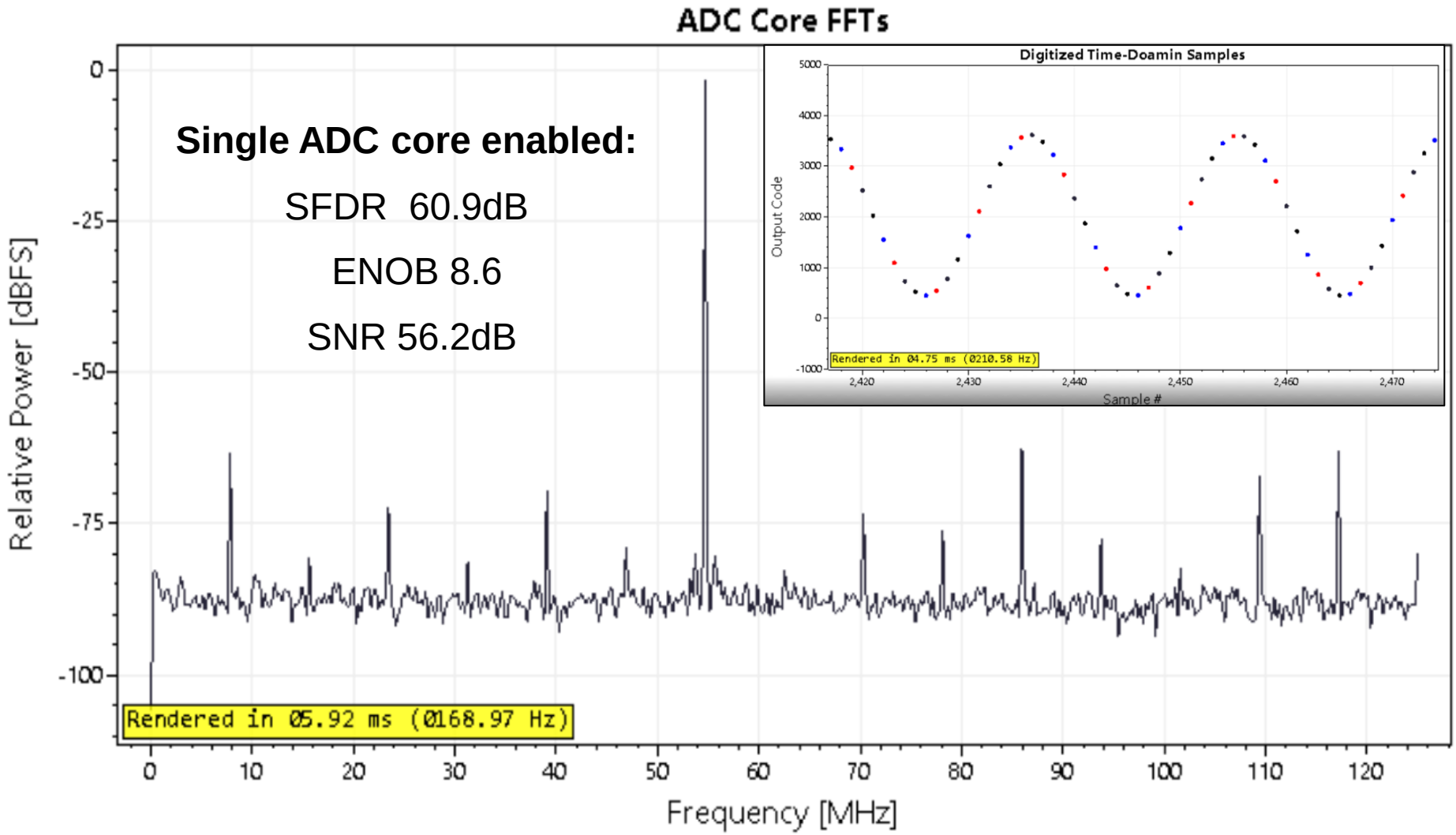
3 SNR=56.2dB THD=-56.9dB SFDR=60.9dB SINAD=53.6dB ENOB=8.6 Avg=2026.7 SW=3306.4 H:303.9/463.2 / CD:394.6



TESTING RESULTS: SINGLE ADC CORE PERFORMANCE

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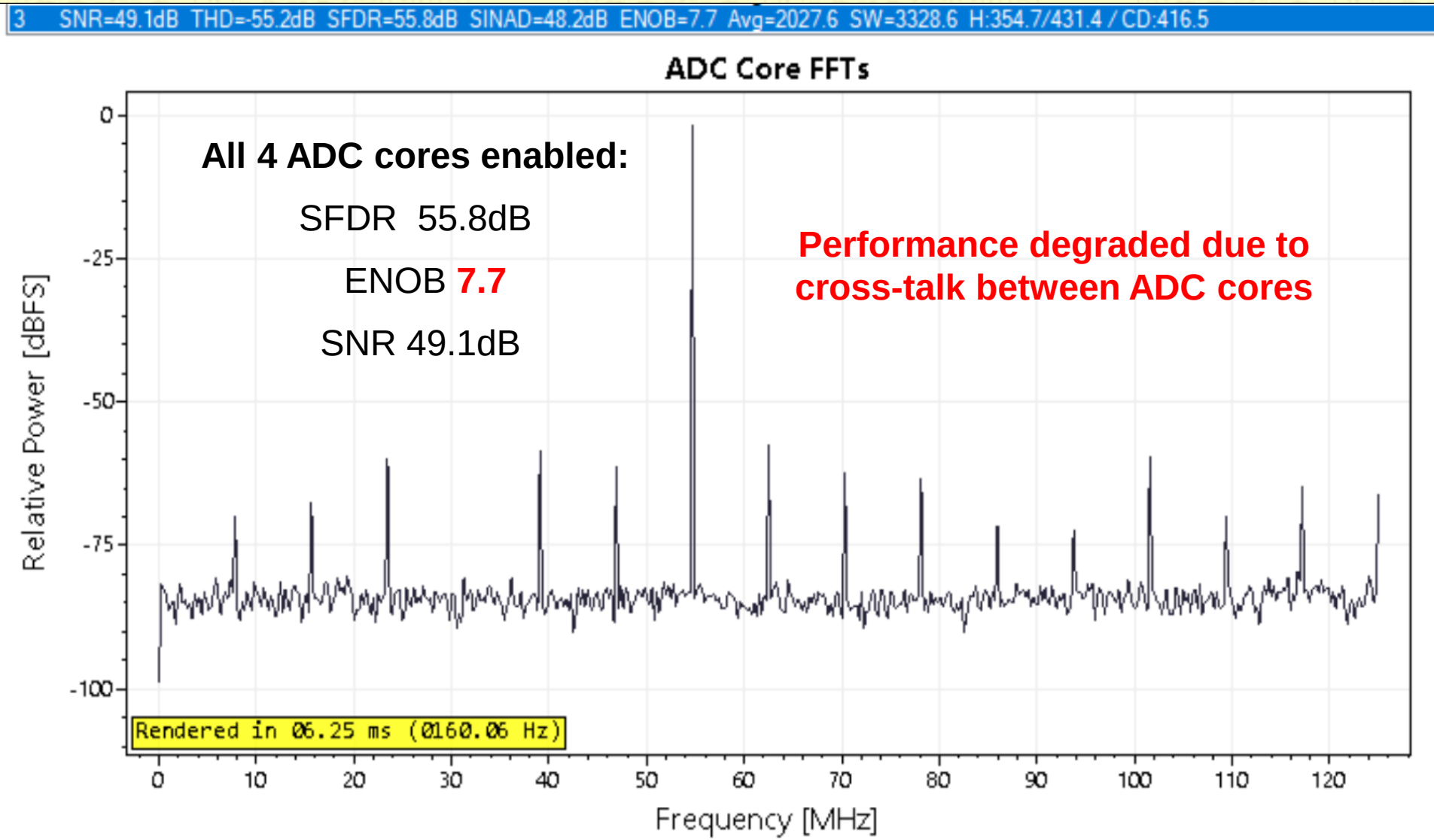

PROJECT SCHEDULE

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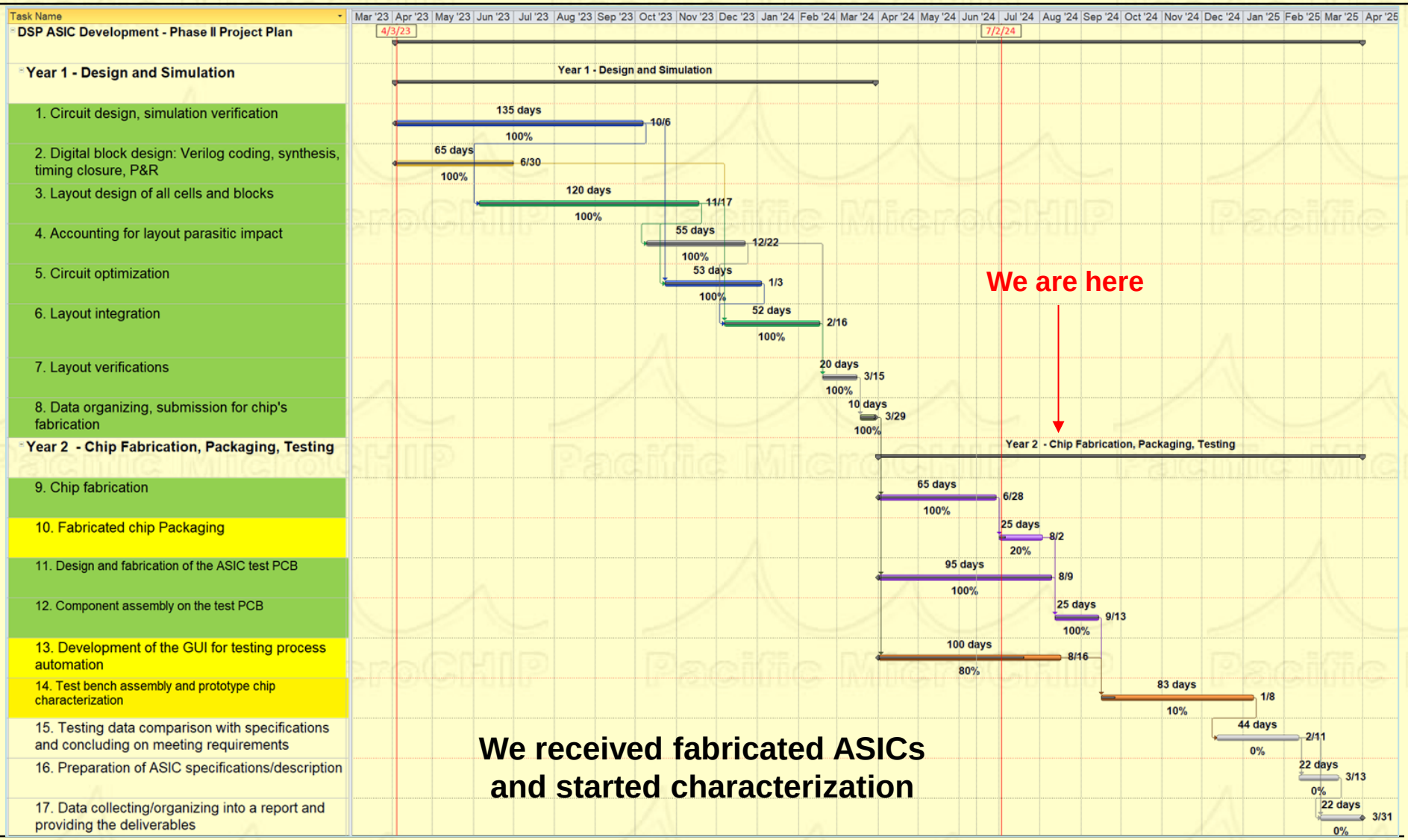

We received fabricated ASICs and started characterization

FUTURE PLANS

- Test/characterize the produced ASIC.
- Create ASIC datasheet
- Start shipping the ASIC/Evaluation boards parts to select customers.

THANK YOU!

Application Ideas for the ADC ASIC are appreciated!