

Project title: High Performance High Current CW polarized photocathodes for Electron Ion Colliders

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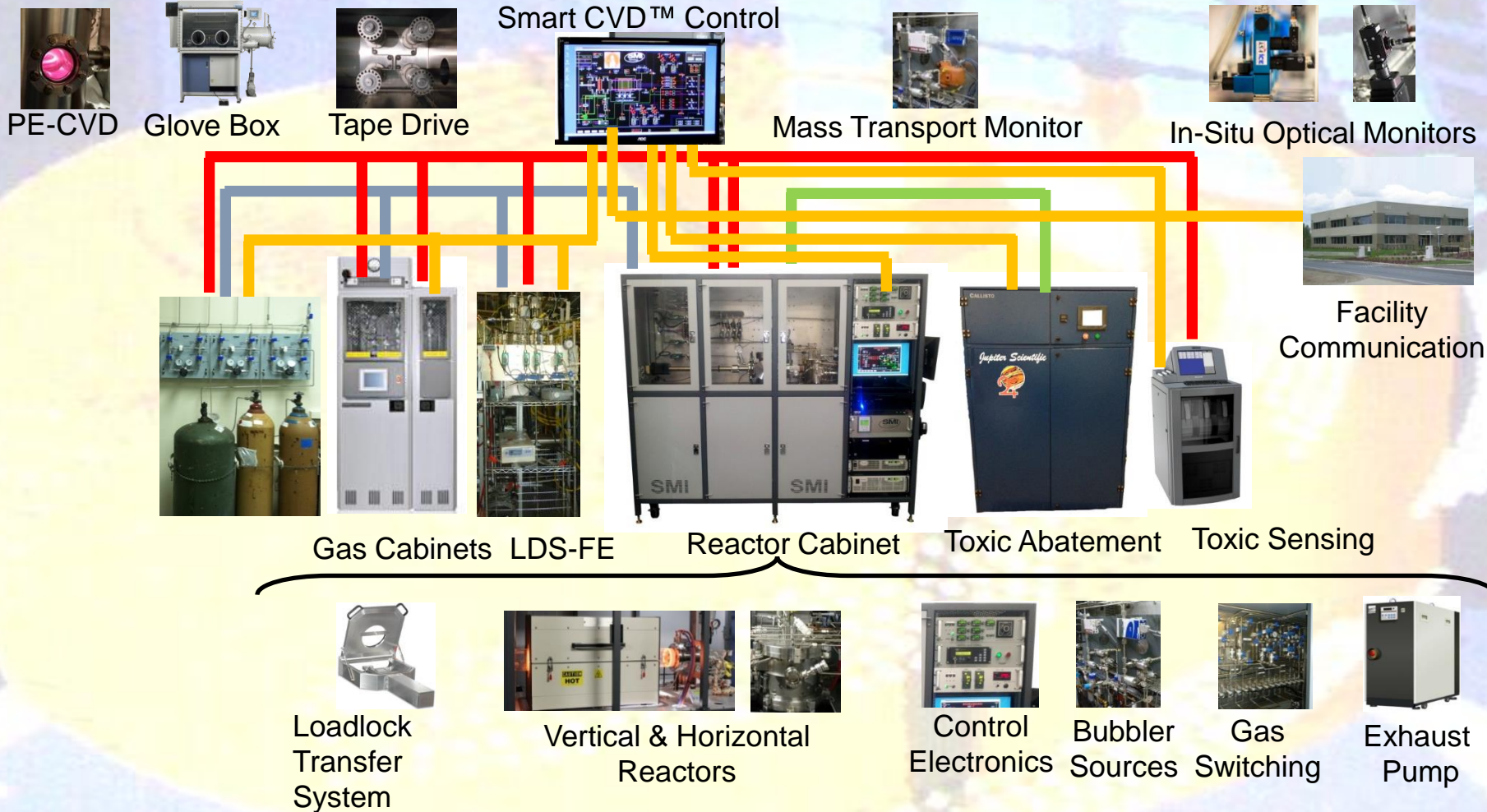
SMI Contract No.: 42199

**Start Date: 04/02/2023, End Date:
04/01/2025**

Phase II Technical Point of Contact:

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Vertical



2400C



Oxides



High Pressure



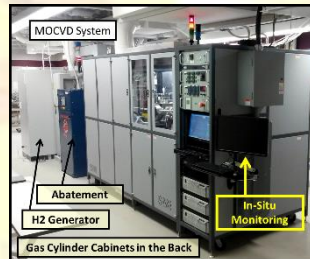
Anneal



VLSI



Horizontal 2D



III-V- II/VI



ALD



Cluster Tool



FB - CVD



HTS Tape



Nitrides / Carbides



Rebuilds & Conversions



ICP-CVD

Diamond -- Annealing -- Components -- Design Services -- Contract Research: Commercial & Government

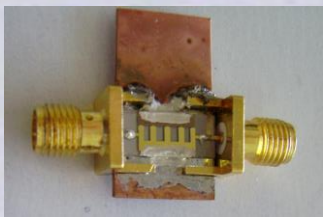
Well Controlled Process – Reproducible Product

Standard Features:

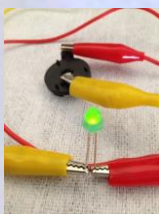
- Low Cost
- Based on commercial software products
- Graphical User Interface in Microsoft Windows environment
- Real time interactive mimic panels of the process system
- Spread sheet interface for process configuration
- Advanced alarm monitoring and management
- Password protection for operator interface

Optional Features

- Real time data logging and displaying
- Network support for distributed control system
- Automated process documentation generation
- Flexible hardware interface (PLCs, commercial instruments, etc...)
- In-Situ Process Monitoring and Interactive Control
- On-Line (Remote) operation, diagnostics, and upgrades
- Maintenance Procedures- Resource Consumption
- Sample/Wafer Tracking
- MECS/SECS Compatibility
- Remote access beyond networking



Tunable X-Band Filter



Battery made from Cathode Material



InN/Graphene Gas Sensor



Display Electrodes



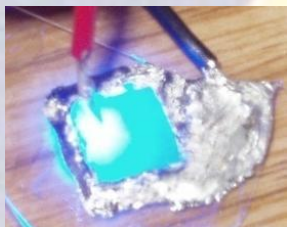
Superconductor Tapes



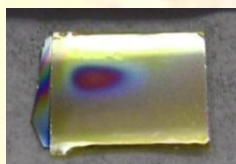
150mm GeSbTe/Si



150mm PZT



Blue LED with ZnO Contacts



CBRAM GeS: Ag on polymer ceramics



Graphene Sensor



Superior LED Contacts



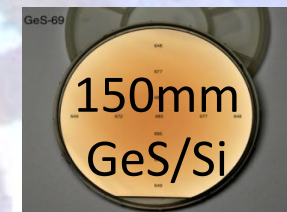
Missile ARCs



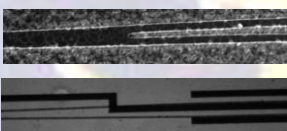
SRAMs and FRAMs



Light Culminating Reflectors



150mm GeS/Si



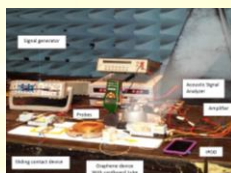
LiNbO3 Waveguide Modulator



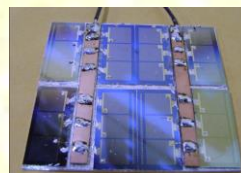
CNT Structures
SMI Logo in CNTs



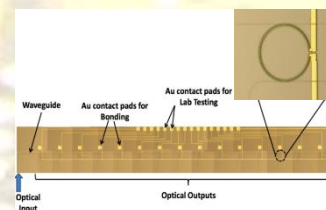
Bulk Crystal Fabrication



Graphene Speaker



PhotoVoltaics & ThermoPhotoVoltaics



Si Photonics



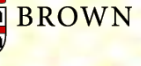
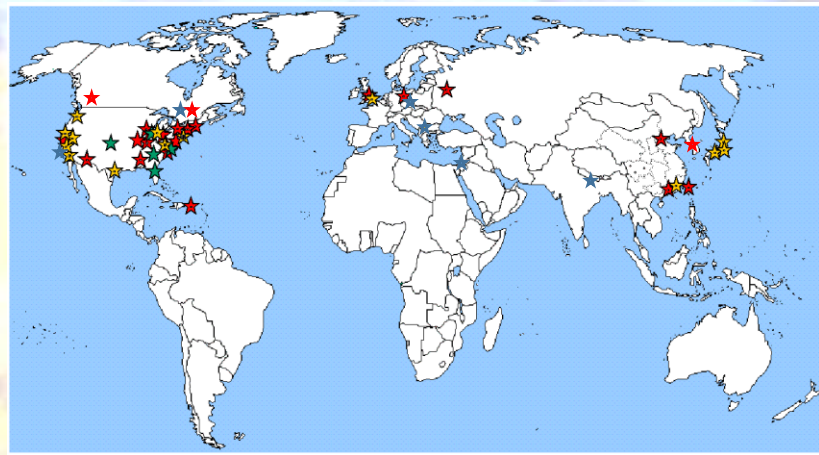
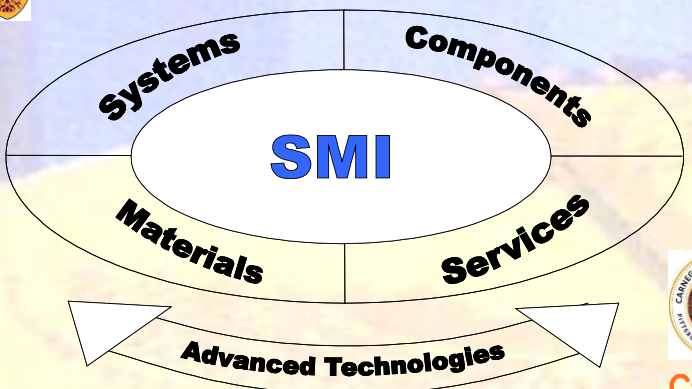
GE Dome Coating



FB-CVD coated with $Ti_{0.5}Si_{0.5}O_2$



75mm X 150mm TCO



Technology Summary:

- We offer a complete fully integrated HTS tape deposition tool
- The developed tool technology will put SMI to manufacture and sell new Generation 4 tools to USA customers.



Proposed Targets:

Metric	State of the Art	SMI
Yield	1.2 km per day	>10km per day
Cost	High	Very low
Coating	Single side coating	Dual-side coating

High-temperature superconducting (HTS) tapes have many potential applications in energy and other fields, including:

- **Electric power:** HTS tapes can be used in motors, generators, transformers, and cables. At low temperatures, they conduct electrical current without resistivity, which can lead to higher power densities and more compact systems.
- **Nuclear fusion:** HTS tapes are used in fusion reactors.
- **Electric grid:** HTS tapes can be used in superconducting cables for the electric grid. For example, the Shingal Project uses a 1 km 23 kV AC HTS cable to connect two substations.
- **Electric aviation:** HTS tapes could be used in electric aviation.
- **Other applications:** HTS tapes could also be used in induction heaters, fault current limiters, power storage, and magnetic levitation devices.

SMI Team



Scientist
Dr. Kannan Vasudevan



President
Dr. Gary Tompa



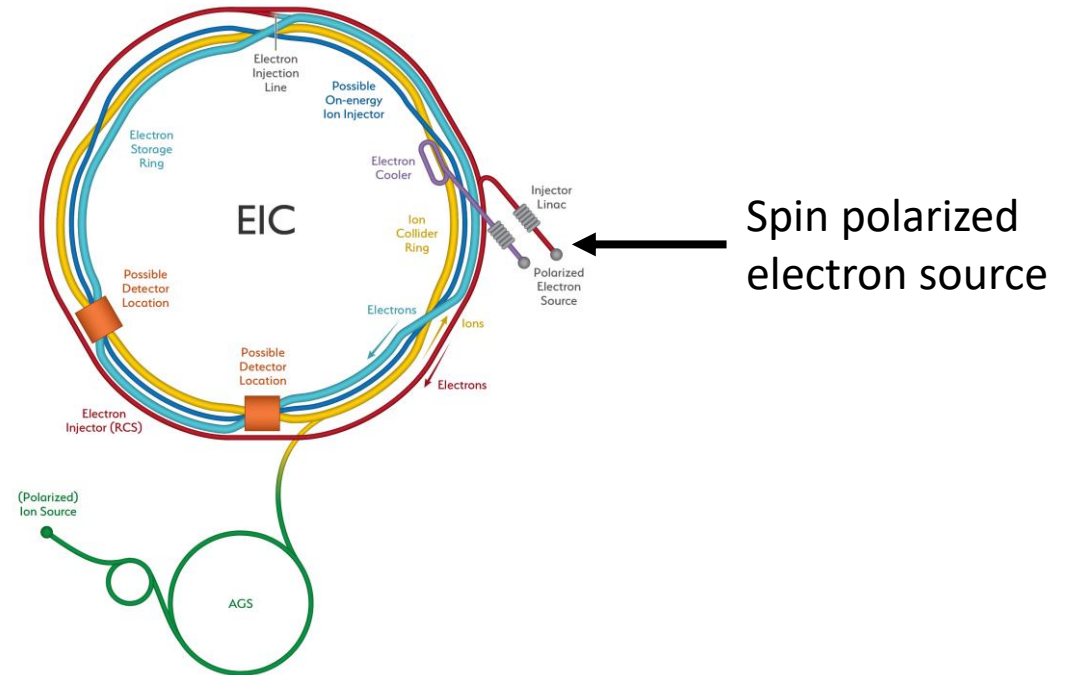
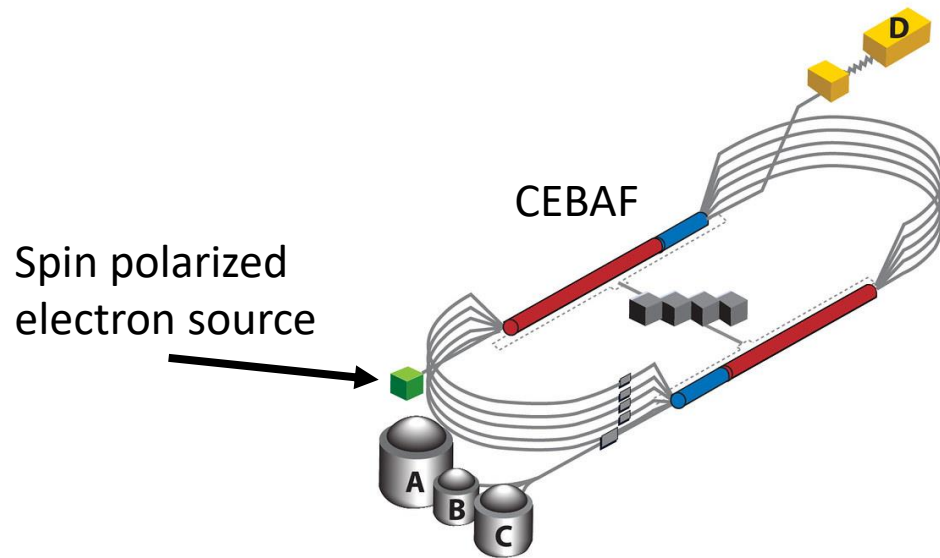
Manager Control
Gary Provost



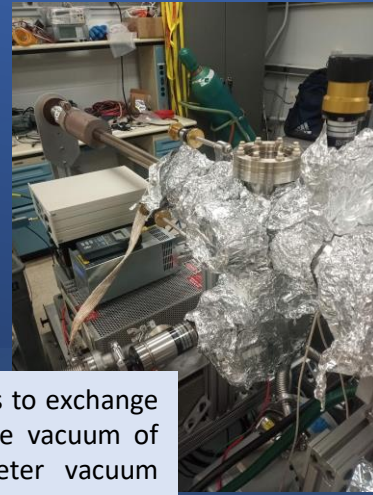
- Team has over 100 years of total experience in tool design, manufacturing, material deposition, device, design, device fabrication, and commercial sales
- We have commercial sales of custom tools and have fielded >70 tools
- As a company, we have 4 patents and 3 pending patents

Need Addressed: *Photocathodes for Spin Polarized Sources*

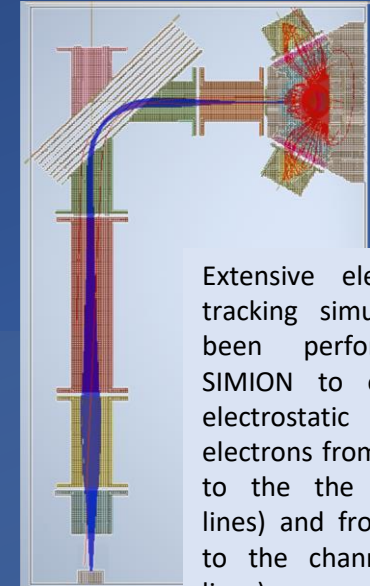
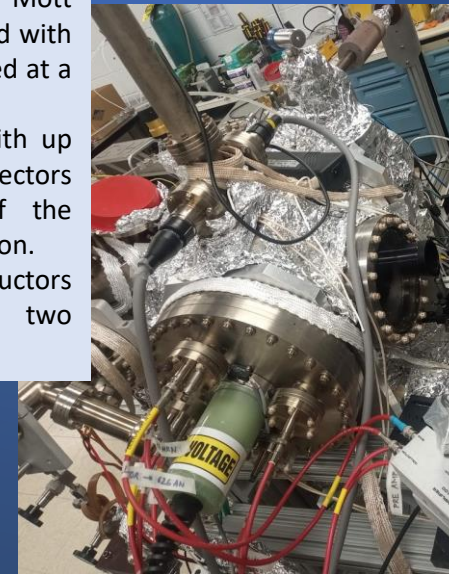
- *Electron Ion Colliders (EIC) need spin-polarized photocathode for examining properties of fundamental particles such as Quarks, Nuclei, Bosons, etc.*
- *Enhanced photoemission properties will also benefit the current and future operation of CEBAF at Jefferson National Laboratory (JLab) as well as future projects at other facilities such as Cornell University*



BNL Photocathode system allows characterization for QE and ESP



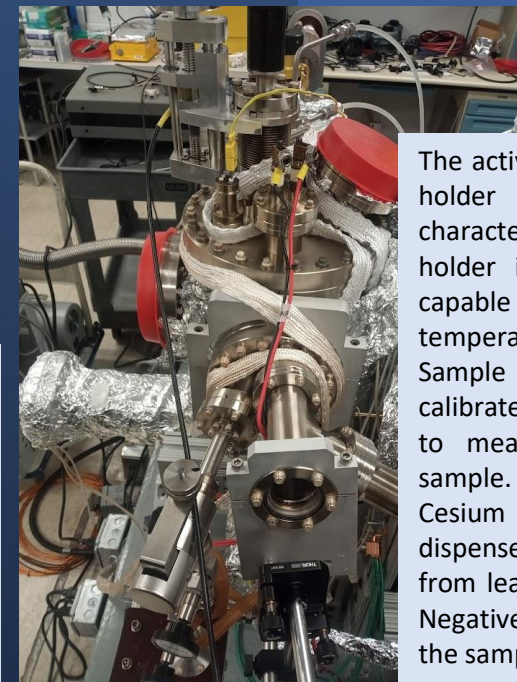
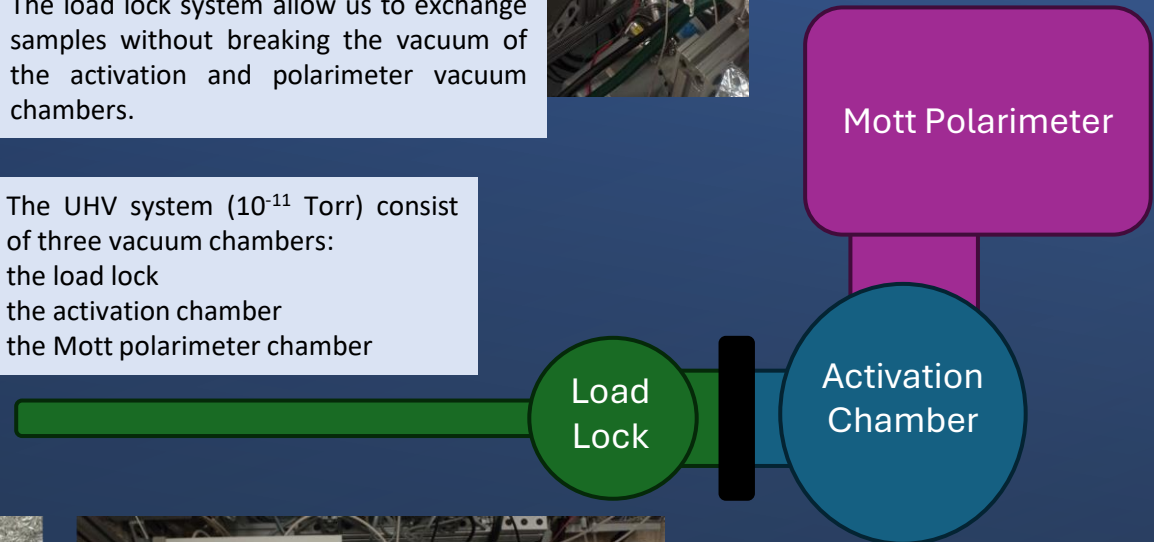
The retarding field Mott polarimeter is operated with an Au target maintained at a voltage of 25 kV. It allows operation with up to 4 channeltrons detectors for the measure of the electron spin polarization. For III-V semiconductors measurement only two channeltrons are used.



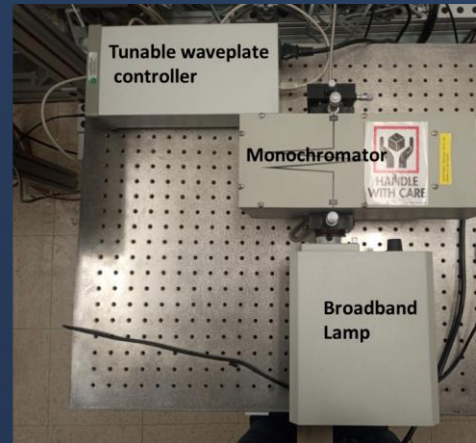
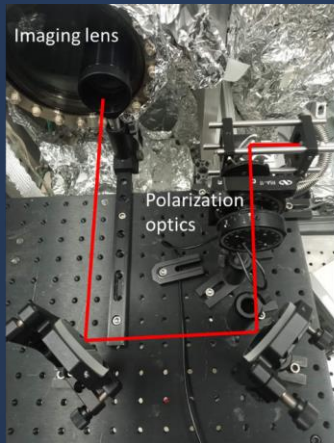
Extensive electron beam tracking simulations have been performed using SIMION to optimize the electrostatic transport of electrons from the cathode to the target (blue lines) and from the target to the channeltrons (red lines).

The load lock system allow us to exchange samples without breaking the vacuum of the activation and polarimeter vacuum chambers.

The UHV system (10^{-11} Torr) consist of three vacuum chambers:
the load lock
the activation chamber
the Mott polarimeter chamber



The activation chamber hosts the sample holder used during activation and characterization of the samples. The holder is equipped with a BN heater capable of bringing the samples to temperatures above 600 C. Sample can be negatively biased and a calibrated K Type thermocouple is used to measure the temperature of the sample. Cesium vapors from a metal chromate dispenser and high purity oxygen coming from leak valve are used to perform the Negative Electron Affinity activation of the samples.



Photons used to illuminate the photocathode during the photoemission experiments are produced by a tungsten halogen lamp. A monochromator is used to select the central emission wavelength with bandwidth of about 10 nm. A combination of a linear polarizer and a tunable liquid crystal retarder are used to produce the left- and right-handed circularly polarized light required to produce spin polarized electrons.

SMI's innovative solution





GaAs	5 nm	$p = 5 \times 10^{19} \text{ cm}^{-3}$
GaAs _{0.62} P _{0.38}	4 nm	$p = 5 \times 10^{17} \text{ cm}^{-3}$
GaAs	4 nm	$p = 5 \times 10^{17} \text{ cm}^{-3}$
GaAs _{0.81} P _{0.19}	300 nm	$p = 5 \times 10^{18} \text{ cm}^{-3}$
AlAs _{0.78} P _{0.22}	65 nm	$p = 5 \times 10^{18} \text{ cm}^{-3}$
GaAs _{0.81} P _{0.19}	55 nm	$p = 5 \times 10^{18} \text{ cm}^{-3}$
GaAs _{0.81} P _{0.19}	2000 nm	$p = 5 \times 10^{18} \text{ cm}^{-3}$
GaAs->GaAs _{0.81} P _{0.19}	2750 nm	$p = 5 \times 10^{18} \text{ cm}^{-3}$
GaAs buffer	200 nm	$p = 5 \times 10^{18} \text{ cm}^{-3}$
GaAs substrate		$p > 1 \times 10^{18} \text{ cm}^{-3}$


} 30 pairs


} 10 pairs



 Highly spin polarized electron source emits electrons upon excitation by a circularly polarized laser beam with energy close to the energy band gap requiring negative electron affinity (NEA) at the surface of the semiconductor:

 BNL designed SL-DBR structure uses strain compensation to mitigate relaxation of strained layer

 This allows for increased number of SL pair for increased optical absorption and hence QE

 Due to the reduced strain (+/- 0.7%) Heavy Hole and Light Holes are separated by only ~66 meV

Technical Approach

- MOCVD is used to grow the components of the designed structure by SRI. The MOCVD system has automated flow ramping, so it is well suited to growing the graded GaAsP needed to accommodate the lattice mismatch of the structure with the GaAs substrate. For the SL active region SRI has used this MOCVD system to grow many SL structures with individual layers as thin as 1 nm.
- SRI has measured photoluminescence of the active region to confirm it is at the intended 780 nm operation.
- Growth of SL active region and DBR was calibrated under the same growth conditions such as temperature, which facilitated growth of the full integrated structure. The proposed device design was developed by Dr. Luca Cultrera.
- MOCVD was selected because it is the de facto production method for compound semiconductors in terms of yield and cost. MOCVD is also versatile in adapting to changing needs. Our approach benefits the research community by developing “commodity” type supply chain.

Major Goals and Objectives of this Project

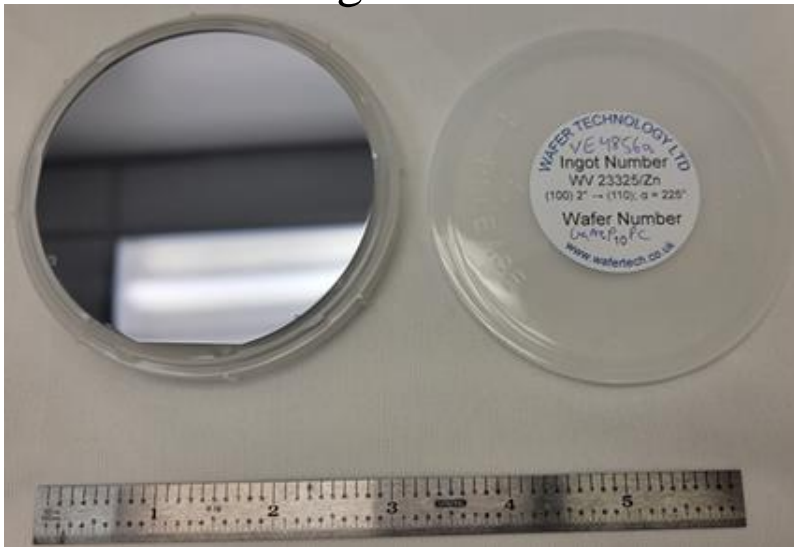
- Refine device design and model-through material and device characterization/performance feedback – with a focus on tuning composition, superlattice (SL) and DBR/F-P layer thicknesses; as appropriate to maximize QE, ESP and lifetimes for operation at 780 nm.
- Mitigate/eliminate oxide formation on top of the device which is suspected/anticipated to decrease the QE and ESP of the photocathode (Starting by using vacuum packaging) and understand impact on ESP if any.

Refine structure tuning to provide optimal performance at 780 nm.

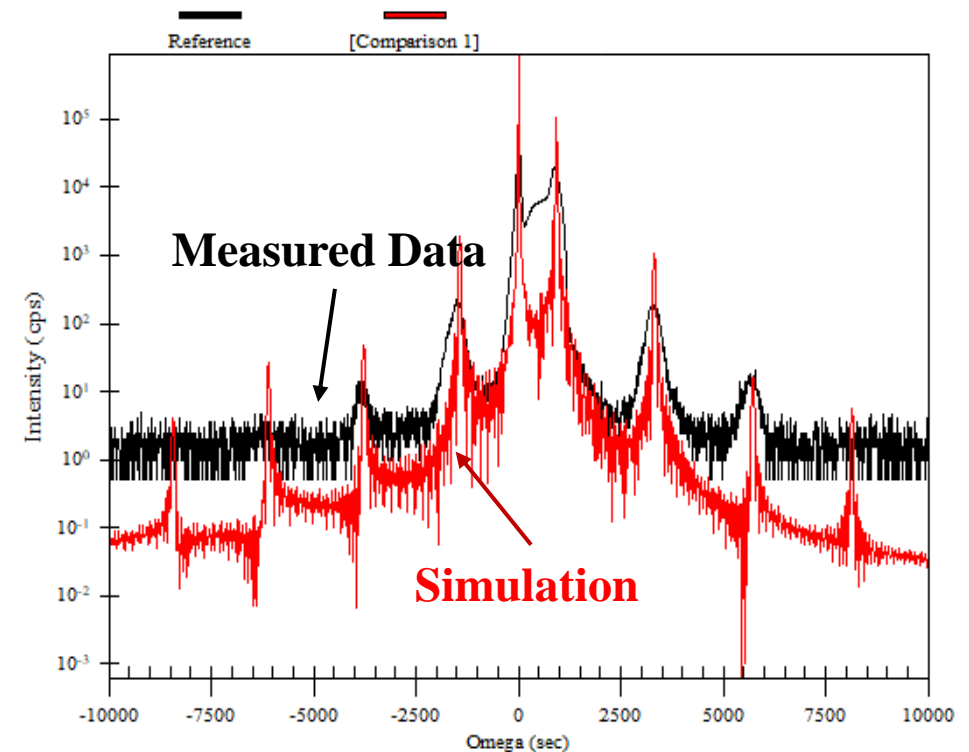
- Determine the commercializable performance specifications of the photocathodes through testing (QE, upper current limit, ESP, operational lifetime, bunch charge achievable, packaging and preparation and compare to commercial values.
- Grow ~ 20 “product” wafers and refine packaging for the application – sampling wafers to end users.
- Demonstrate high performance spin polarized photocathodes at BNL testing laboratory and potentially sample to other interested groups – including Jefferson National Lab, Cornell University, and others yet to be determined or suggested by DOE.
- Refine Phase III production and commercialization pathways – evaluate additional market.

Growth of GaAs/GaAsP SL on base structure

- GaAs_{0.81}P_{0.19} composition, growth rate and doping were calibrated, and base structures were grown.
- Following this GaAs_{0.62}P_{0.38} was calibrated, and SL structures were grown and optimized on existing base structures.
- Two wafers with full structure except DBR sent to BNL for testing.



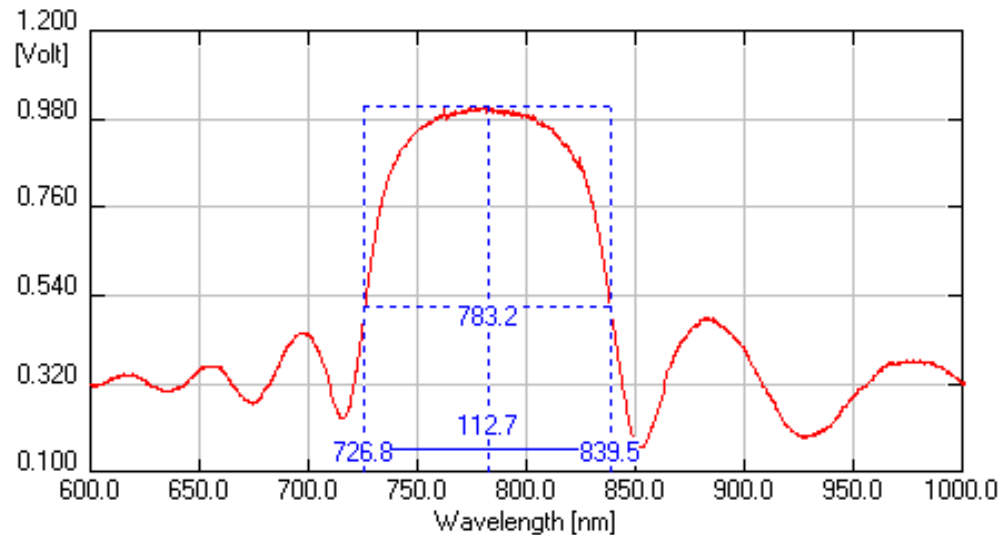
Photograph of 3-inch full wafer structure except DBR



X-ray measured data (black) compared to simulation (red) of full structure except DBR. The measured peak spacing and position match up indicating thickness and composition is close to simulation data.

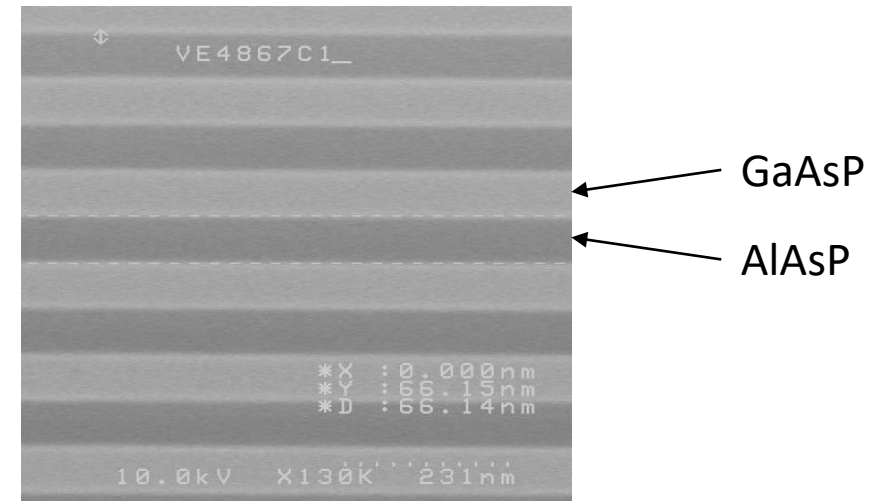
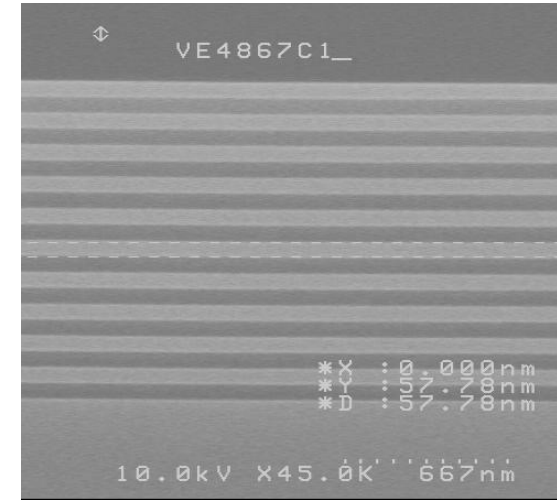
DBR calibration

- $\text{AlAs}_{0.81}\text{P}_{0.19}$ was calibrated and several wafers of DBR on base structure were grown.
- Thickness was adjusted to target reflectance at 780 nm.



Reflectivity of DBR regrown on base wafer centered near target 780 nm.

Proprietary and Confidential to Structured Materials Industries, Inc.



SEM image of cross section of DBR calibration run shows good uniformity and correct layer thicknesses.

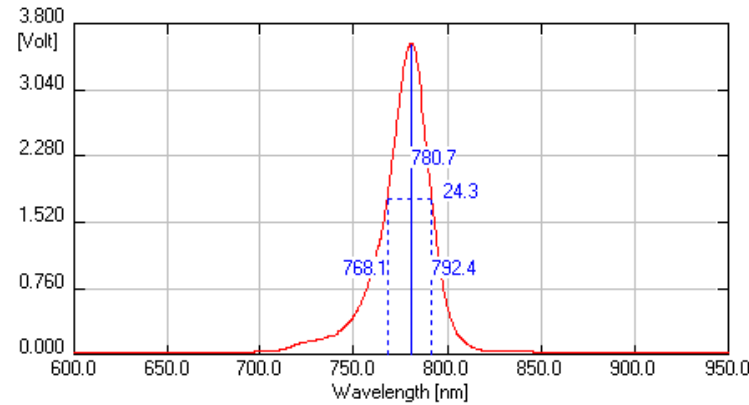
Full structure growth

In Phase I, three wafers of full structure including DBR layers were grown:

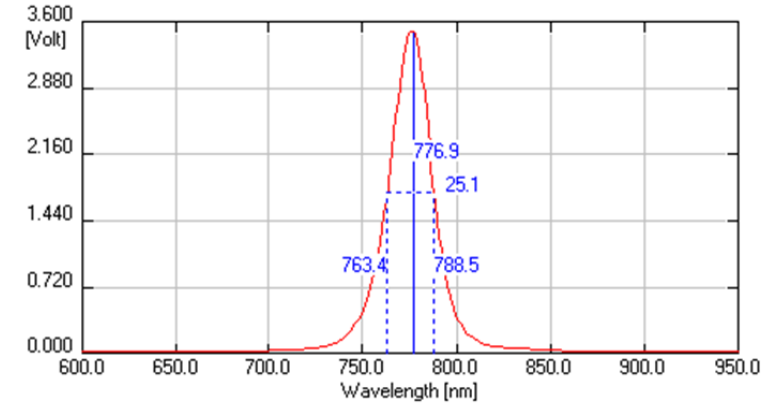
- VE4874c –Targeting as-designed structure but reflectivity had Fabry-Perot dip about 790 nm indicating etalon slightly thicker than target.
- VE4875c –Based on feedback from BNL reduced growth time of top GaAsP layer and SL which shifted FP-dip to 780 nm.
- VE4879c –Reduced target thickness of SL to 3.5 nm each layer and increased GaAsP to compensate. FP-dip still about 780 nm, PL shifted slightly shorter.

Full structure wafers sent to BNL for testing

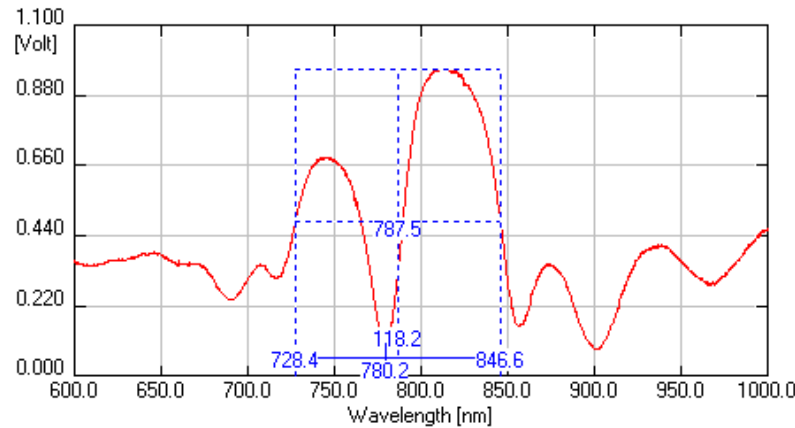
Reactor can grow three 3” wafers.
There is non-uniformity but better than MBE



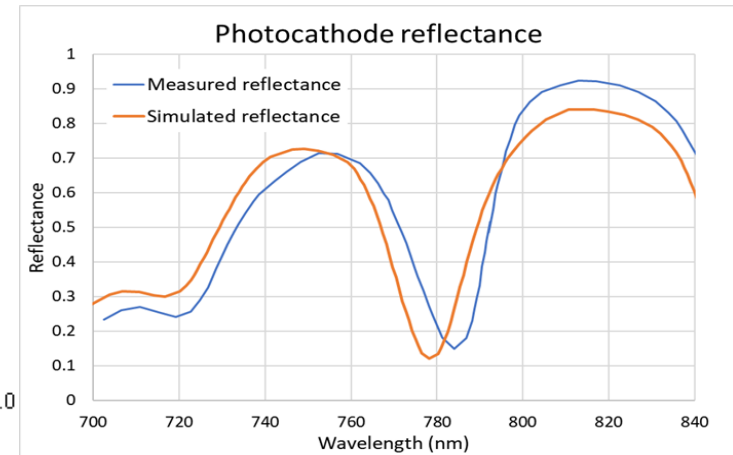
VE4875c: Photoluminescence at center



VE4879c: Photoluminescence at center

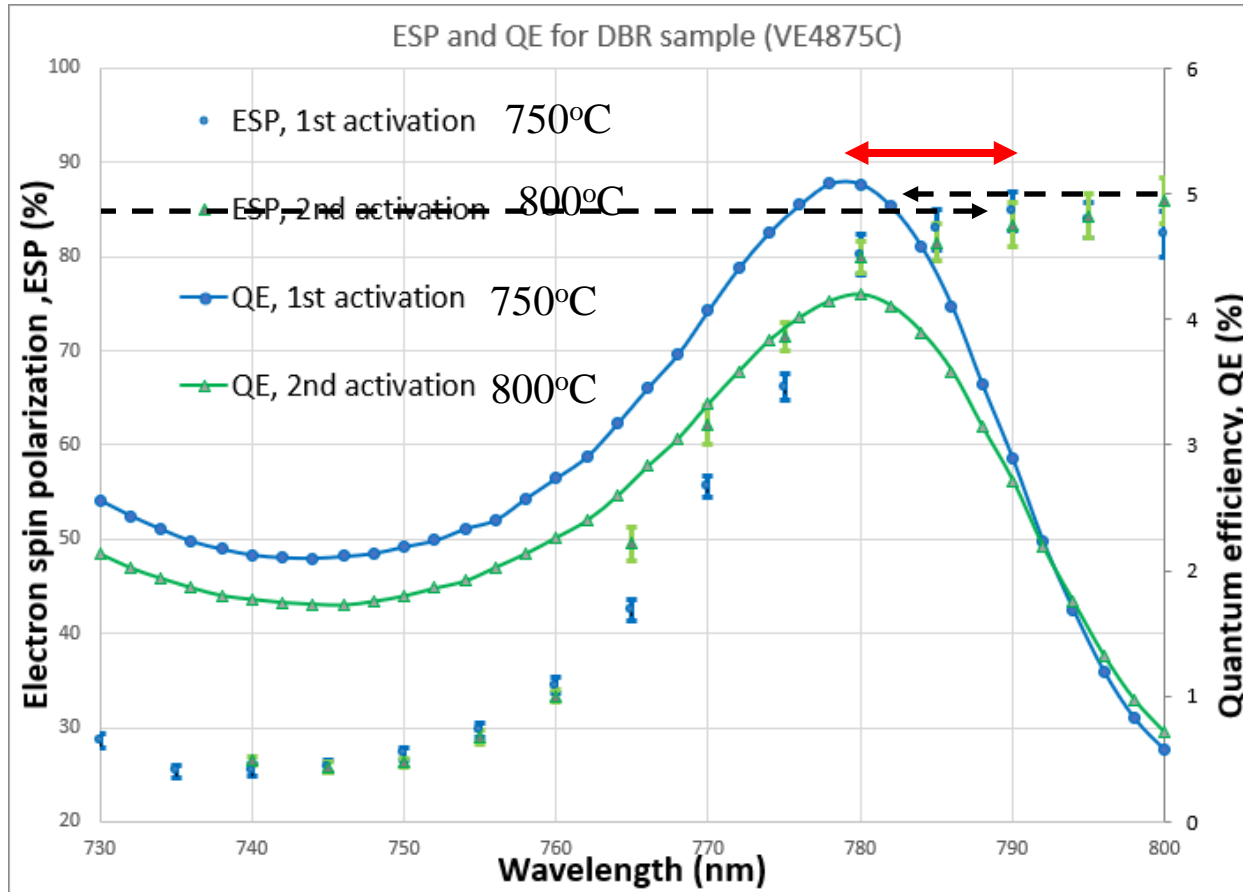


VE4875c: Reflectance at center (left), Reflectance measured is very similar to simulation (right).



Phase I Results

ESP and QE Vs Wavelength for sample with DBR



Sample is not Arsenic (As) capped and oxide is likely formed at the DBR-SL interface and surface.

Heat clean at <600 C will likely not remove all oxide (reported temperatures are for the heater not the sample).

QE > 5%

ESP > 85%

To meet SBIR ideal specs:

Align the peaks ~780

Increase QE >5% (if not 10%)

and push ESP >90%

Phase-II Approach to Increase ESP and QE

Several new growth runs and tests have been performed to further improve ESP and QE. The rationale is as follows:

- **C doping** was tested as literature reports indicate larger optical absorption compared to Zn-doped layer;
 - Zn does not incorporate easily in DBR AlAsP layers;
- **1-step growth:** no interruption between DBR and SL layers to mitigate possible contamination;
- **Tested a new SL-DBR structure** that uses a slightly larger strain ($\pm 0.8\%$) which increases HH-LH separation up to ~ 77 meV;
- **Increased the number of DBR layers** to further increase the reflectivity;
- **Sealed packaging of wafers** to mitigate surface oxidation and facilitate NEA formation during activation.

Phase II full structure growths

Growth	Pseudo substrate	Growth steps	GaAsP dopant	AlAsP dopant	GaAs (SL and cap) dopant	Reflectance FP dip (nm)	PL peak (nm)	SL thickness GaAsP/GaAs	DBR pairs	Differences from phase I	Remaining	QE@780 (%)	ESP@780 (%)	Peak ESP (%)	Peak ESP wave (nm)
VE4875	GaAsP19	2	Zn	Zn	Zn	780	781	4 nm/4nm	10	Best From Phase I		5	80	85	790
VE5360	GaAsP19	2	Zn	C	Zn	788	789	4 nm/4nm	10	C for AlAsP	1/4 air	4	60	65	800
VE5368	GaAsP19	2	Zn	C	Zn	789	748/790	4 nm/4nm	10	C for AlAsP	Two 1/4s no air, 1/4 air				
VE5370	GaAsP19	2	Zn	C	Zn	798	731/795	4 nm/4nm	10	C for AlAsP	1/4 no air	5	50	55	780
VE5371	GaAsP19	2	Zn	C	Zn	783	724/778	4 nm/4nm	10	C for AlAsP	1/4 no air, 1/4 air				
VE5372	GaAsP19	2	Zn	C	Zn	791	792	4 nm/4nm	10	C for AlAsP	1/4 air	5	65	75	800
VE5374	GaAsP19	1	Zn	C	Zn	801	751/800	4 nm/4nm	10	C for AlAsP, 1-step growth	whole no air, whole air (broken)				
VE5378	GaAsP19	1	Zn	C	Zn	774	780	4 nm/4nm	10	C for AlAsP, 1-step growth	whole air	11	46	68	800
VE5379	GaAsP19	1	Zn	C	C	770	772	4 nm/4nm	10	C for AlAsP, 1-step growth, C for GaAs in SL and cap	whole air	15	42	65	800
VE5384	GaAsP22	2	Zn	C	Zn	789	728/791	5 nm/4.5nm	10	C for AlAsP, higher strain, thicker SL	1/4 air				
VE5385	GaAsP22	2	Zn	C	Zn	795	730/795	5 nm/4.5nm	10	C for AlAsP, higher strain, thicker SL	1/2 air	8	45	57	795
VE5386	GaAsP22	2	Zn	C	C	768	729/775	5 nm/4.5nm	15	C for AlAsP, higher strain, thicker SL, C for GaAs in SL and cap, more DBR pairs	1/2air	3	52	75	790

Best of ESP & QE data

	QE (%)	ESP (%)	FoM=QExESP ²
Phase I (SMI/SRI/BNL)	4.5	85	3.26 % @ 780 nm
Phase II-R (SMI/SRI/BNL)	13.5	65	5.70 % @ 790 nm
BNL/SNL	15.5	62	5.96% @ 776 nm [1]
SVT/JLab	6.4	84	5.52% @ 776 nm [2]
JLab	2.9	82	1.92% @ 785 nm [3]

References:

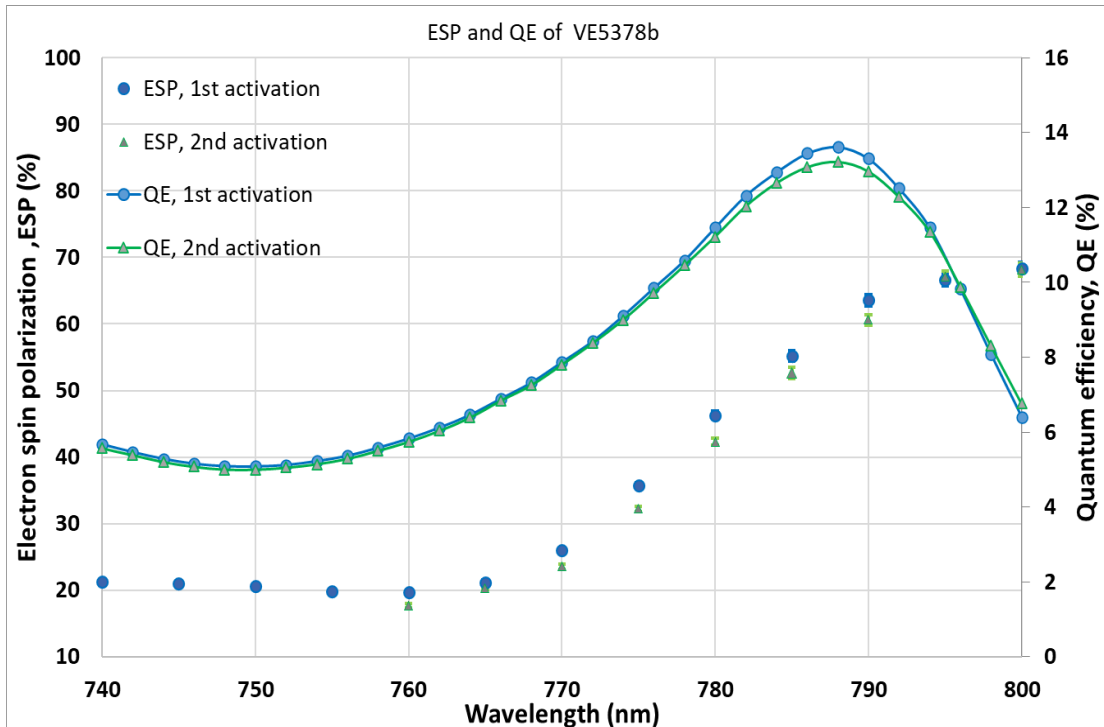
1. Jyoti Biswas, Luca Cultera, et al., *AIP Advances* 13, 085106 (2023).
2. W. Liu, et al., *Appl. Phys. Lett.* 109, 252104 (2016).
3. B. Belfore et al., *Appl. Phys. Lett.*, DOI: 10.1063/5.0170106



Pictures from left full structures sealed in N₂ and never exposed to air, Full structures used for characterization and exposed to air and calibration structures.

Present Status: Exploring Phase Space

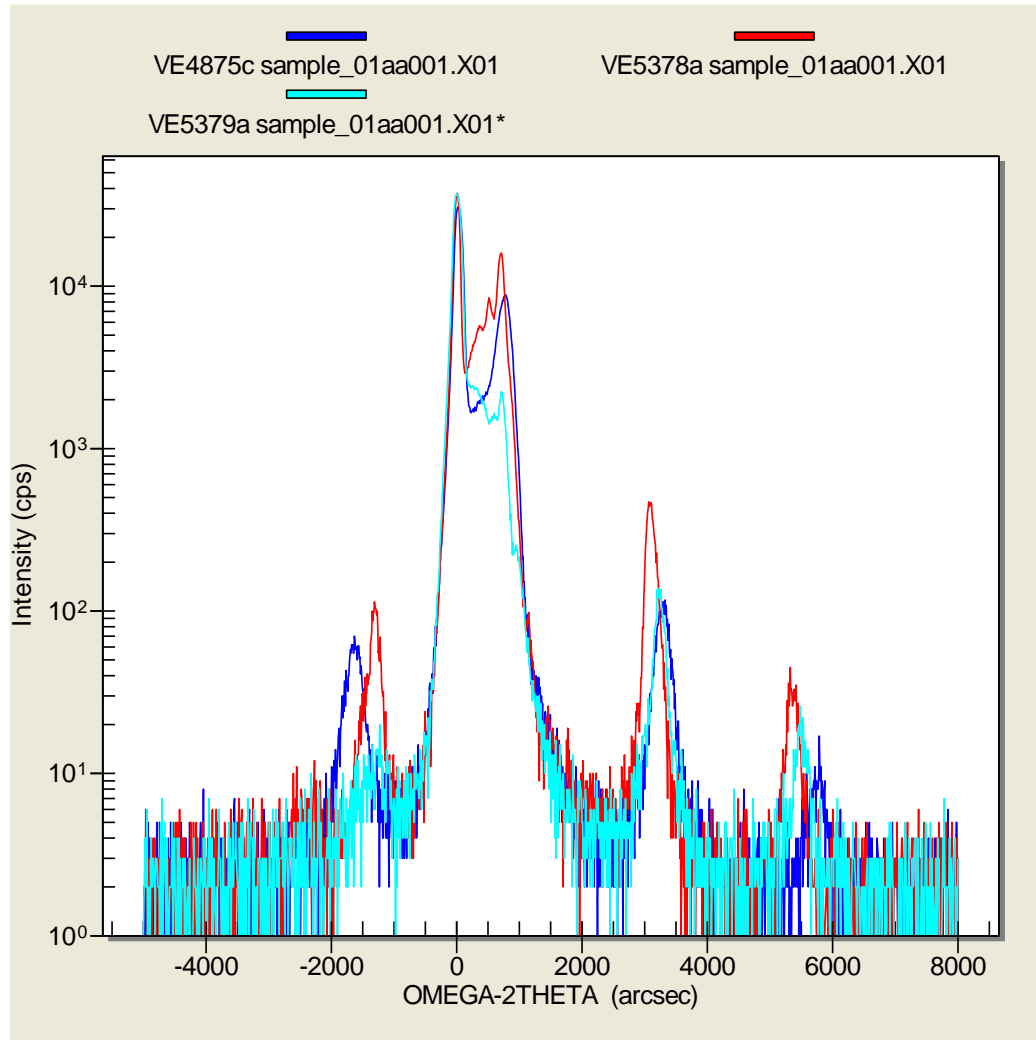
- Proper packing seems to improve QE (>10% @780 nm)
- No improvement in ESP (decreasing)



Exploring new paths:

- **Increasing the thickness of the pseudo-substrate** to decrease the density of dislocation before the SL-DBR growth (from 2 to 4 microns); thereby increasing ESP.
- **Lower the doping on the uppermost GaAs layer** to reduce depolarization as the high achieved QE should mitigate Surface Charge Limit effect (likely reduce to $1-3 \times 10^{19} \text{ cm}^{-3}$);
- **Decrease the strain compensation** in the SL to obtain larger HH-LH energy separation (a design is ready that yield a separation of 100 meV);
- **Decrease the number of SL layer** as we can trade-off QE for mitigating depolarization due to transport from deeper layers (reducing to 20 layers);

Comparison of X-ray measurements of Phase II&I samples

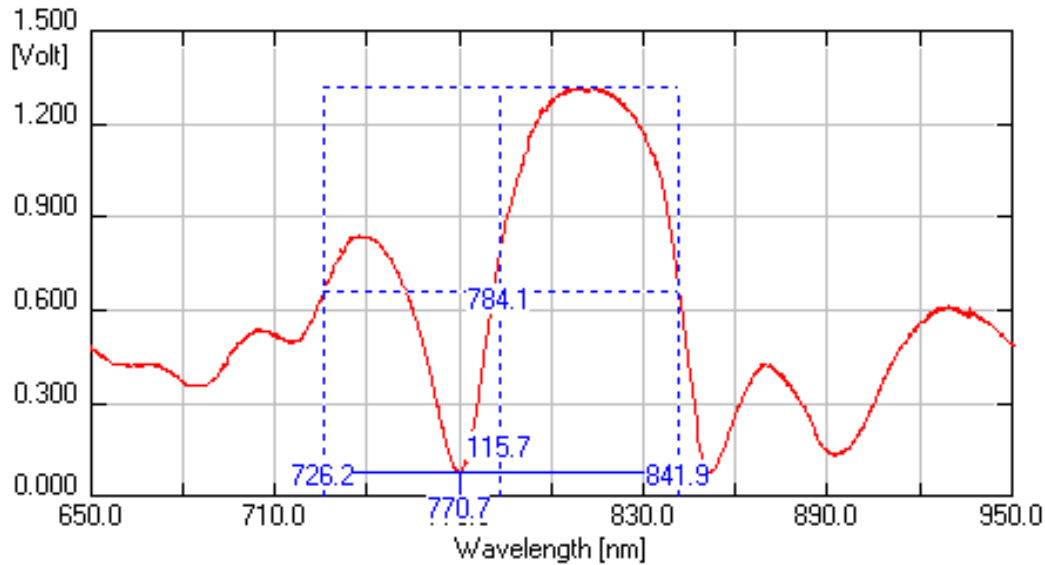


Comparison of the Best Phase I Sample with Phase II Samples in Single-Step Growth

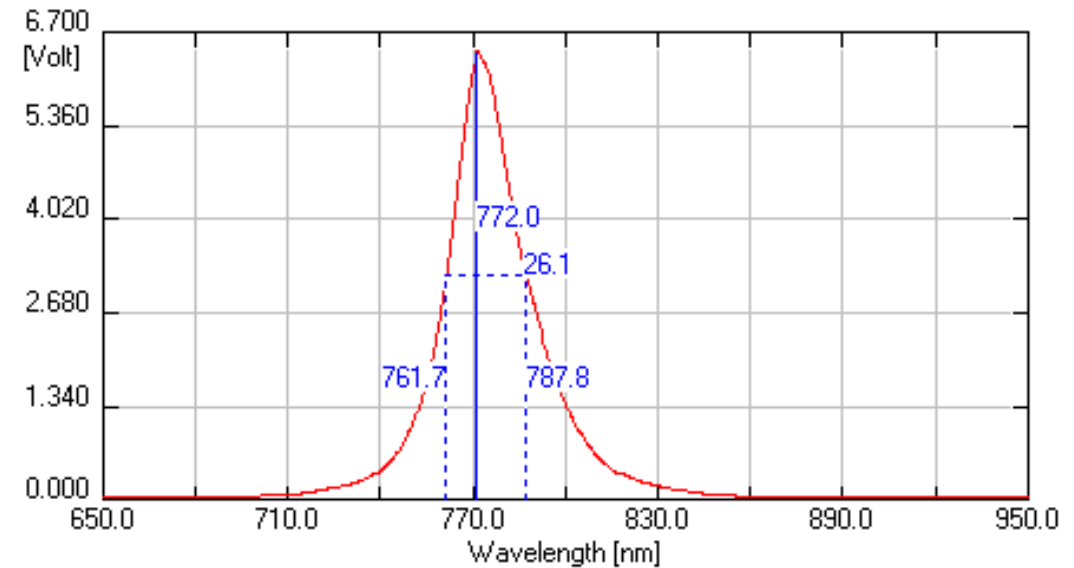
- The spacing between the GaAs pseudo-substrate peak and the GaAs substrate is slightly greater in the Phase I sample.
- This indicates that the GaAs in the superlattice may be slightly more strained.
- The presence of peaks between the GaAs pseudo-substrate peak and the GaAs substrate might suggest incomplete relaxation of the pseudo-substrate.
- The fringe spacing is wider in the Phase I sample.
- This indicates a slightly smaller superlattice period (approximately 7.6 nm in Phase I compared to 8.5 nm in Phase II).
- For future growths, the goal is to achieve a closer match in these parameters.

Comparison full structures grown on GaAsP19 pseudo substrate in Phases I and II

Reflectance and PL measurements on Phase II samples



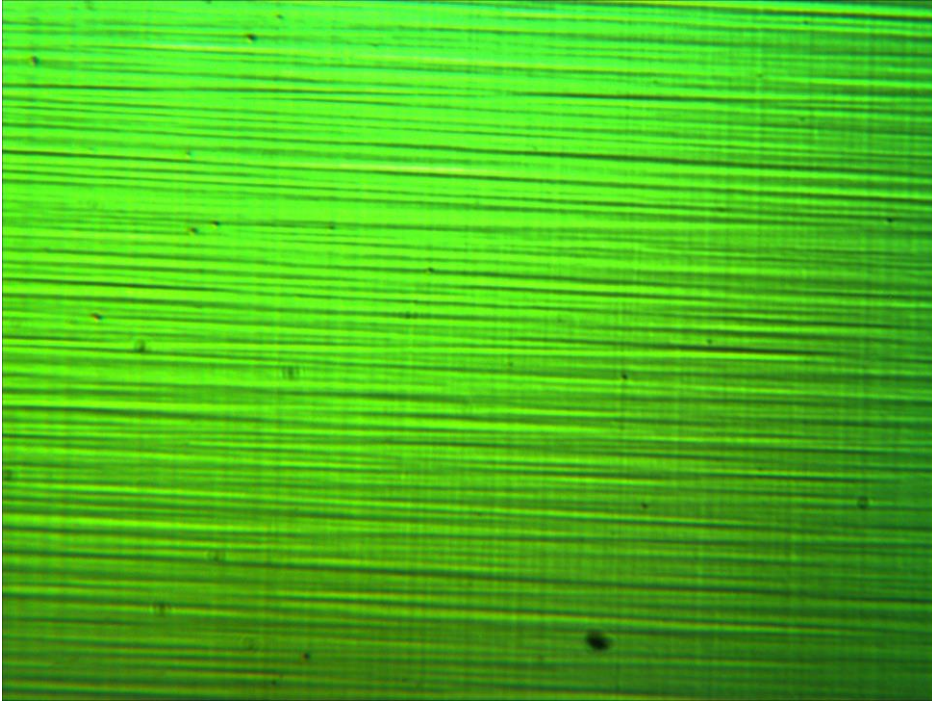
Sample VE5479 Reflectance



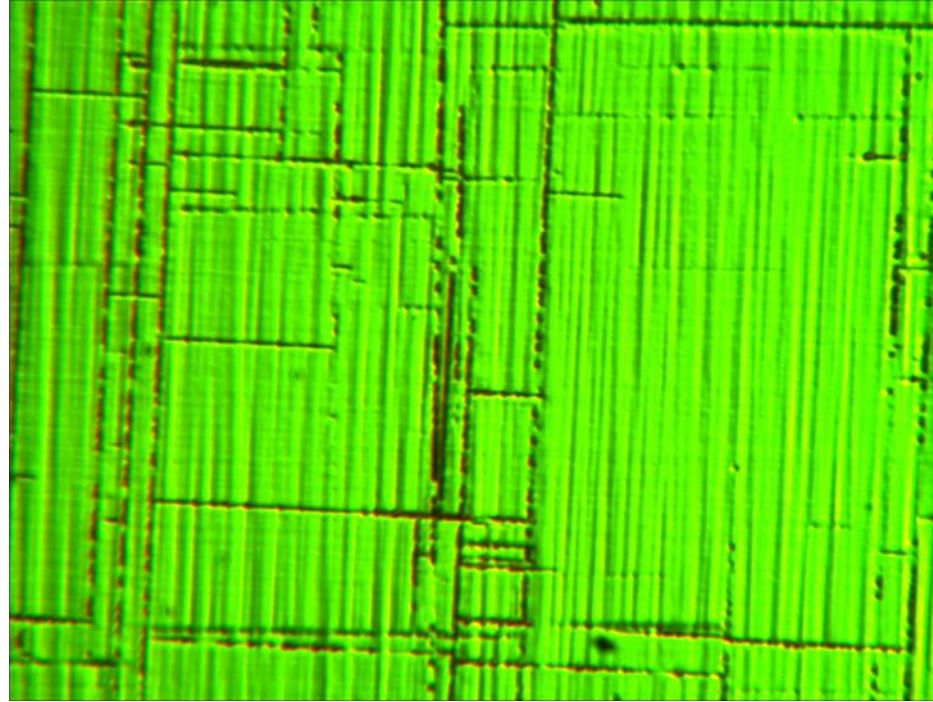
Sample VE5479 Photoluminescence

- FP dip at correct wavelength very important to performance.
- Photoluminescence peak narrow and matching FP peak indication of correct PL wavelength from SL.
- Parameter space will be explored more closely in next growth iteration.

Surface photographs of Phase II full structures



VE5379b (80X)



VE5386c (80X)

- More uniform surface seems to correlate with better QE and possibly better ESP.
- Determine effect of 1-step vs. 2-step growth of structure.
- Determine effect of pseudo-substrate growth. Possible variables include thickness of pseudo-substrate, growth temperature and step-graded vs. continuous graded region.

Work Plan to increase ESP back to >80% while retaining high QE

- High QE achieved (>14%, target >10%)
- Aim to Achieve ESP > 85% and QE>10 % with Figure of Merit > 6
- Increasing Pseudo-Substrate Thickness to reduce dislocation density which is expected enhance ESP.
- Reducing Doping in Upper GaAs Layer to minimize depolarization, thereby increasing ESP.
- Adjusting Strain Compensation to increase ESP- Our design is available that provides a separation of 100 meV between HH-LH.
- Reducing SL Layer Count to reduce depolarization caused by transport from deeper layers.
- Proper packaging helps maintain high QE.

Timeline to deliver “20 Product” wafer to DOE

- *We expect to conclude exploring phase space by Oct.-Nov. 2024.*
- *We will start growing final wafers end of November 2024.*
- *In one deposition run 3x3” diameter wafers can be grown.*
- *About 7 runs will be need to complete 20 - 3” wafers.*
- *We intend to finish growth by the end of December 2024.*
- *Deliver 20 wafers to DoE by January 2025.*

Conclusion/Status:

- *High Figure of Merit Spin Polarized Photocathode grown in the tool available for this project.*
- *Figure of Merit > 5% can be grown routinely.*
- *Working to maximize both QE and ESP.*
- *Plan is to deliver 20 product wafers.*

THANK YOU

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