Pacific MicroCHIP Corp.

An ASIC with a Low Power Multichannel ADC for Energy and Timing Measurements

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OUTLINE

- The company, its specialization/expertise
- Specifications for the multichannel ASIC for energy and timing mesurements
- ASIC core architecture with event-driven backend for detector streaming readout
- Phase IIB project objectives
- Modifications done for the 2nd Gen ASIC
- Assembled parts
- Updated PCB design
- ASIC testbench setup for JESD204B interface and multi-channel operation
- ADC testing results
- Phase IIB project schedule

COMPANY

Pacific MicroCHIP Corp. is incorporated in 2006. It is headquartered in Culver City, California. Main focus – providing IC/ASIC design services and turnkey solutions. The office includes the working space and a laboratory for ASIC testing.

Core expertise:

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (CMOS/SiGe) down to 7nm

MULTICHANNEL ADC ASIC SPECIFICATION

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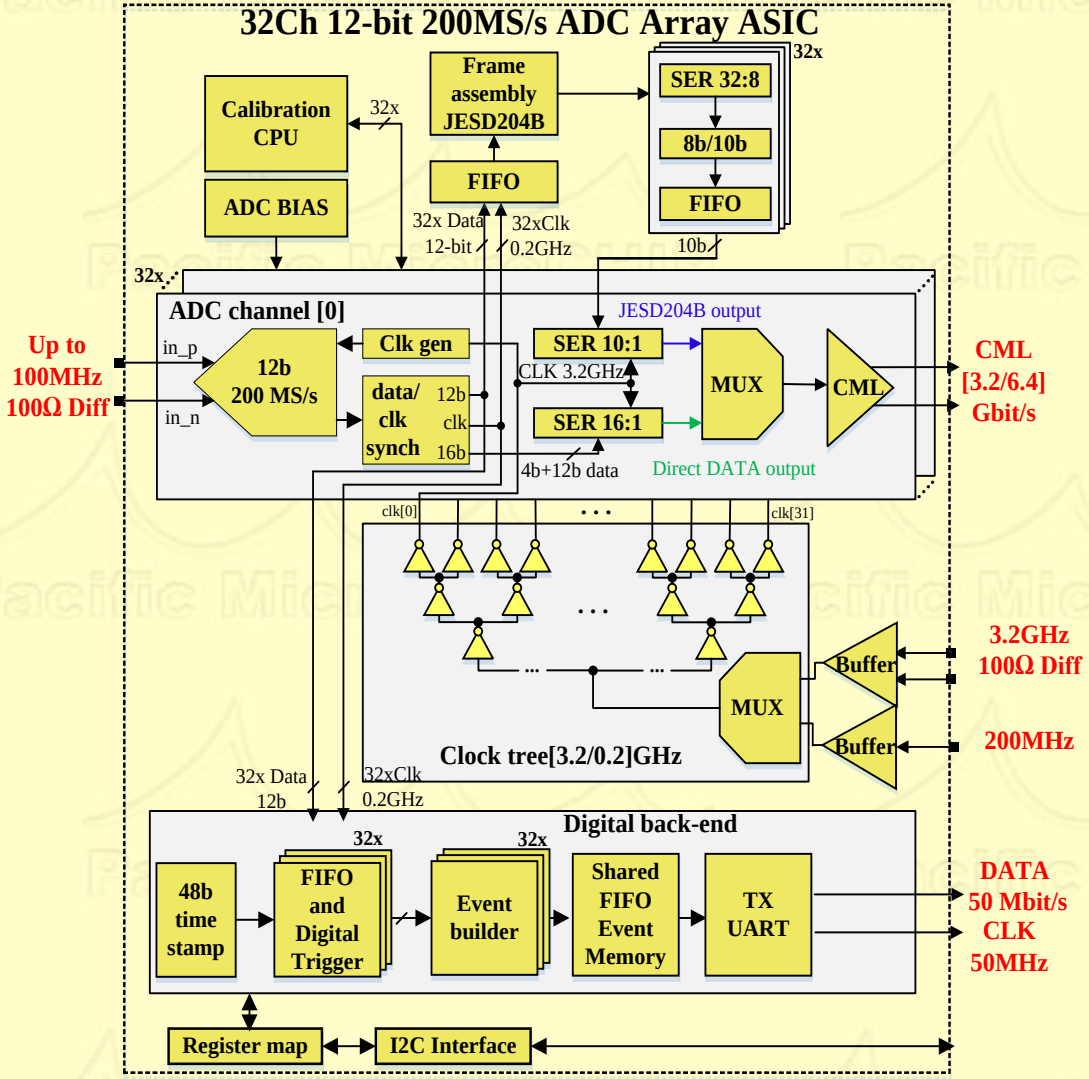
FEATURES:

- 32 independent channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input signal
- ENOB >9-bit
- Programmable input signal bandwidth 0.1-0.3 GHz
- Integrated event-driven digital backend
- JESD204B output data interface
- Extended temperature range
  -40C..+125C
- Low power consumption
- I2C interface for ASIC control

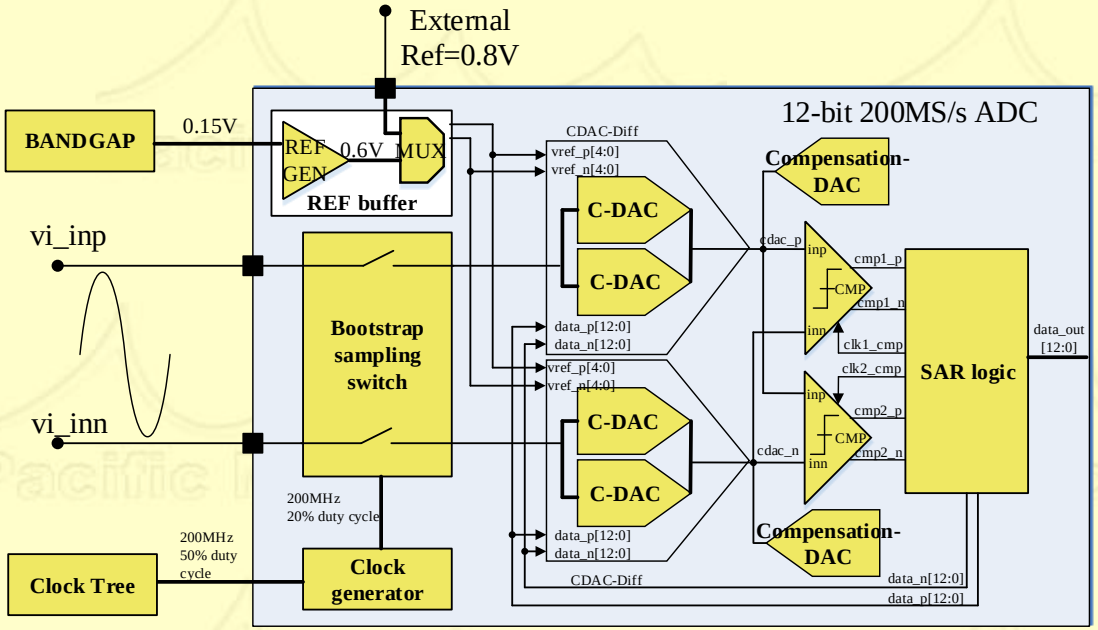


ADC CORE ARCHITECTURE

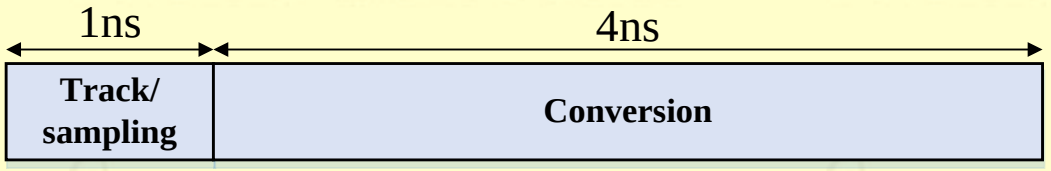
FEATURES:

- 12b SAR ADC architecture
- Segmented 3t-9b CDAC
- Optional external/internal ADC reference voltage source
- Fractional reference voltage
- Dual comparator
- Asynchronous logic
- Built-in FSM for comparator offset compensation
- Built-in FSM for CDAC non-linearity calibration

ADC CORE BLOCK DIAGRAM:



ADC TIMING DIAGRAM:



ADC SPECIFICATION TABLE

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Parameter	Min	Typ	Max	Units	Notes
ADC					
ADC channels	---	32	---	---	Independent
ADC resolution	---	12	---	bit	
ENOB	9	---	9.7	bit	
Sampling rate	---	200	---	MHz	
Data Output					
Number of ADC outputs	---	16	---		Differential
Readout ADC line rate	---	6.4	---	Gb/s	
Event data output		124		bit	For each event
Output impedance	---	100	---	Ω	Differential (LVDS/CML)
Control Interface					
Interface type		I2C			Two wire interface
General Specifications					
Technology for implementation		28nm HPC TSMC+			
Core Power Supply Voltage (VDDD)	0.85	0.9	0.95	V	
Analog Power Supply Voltage (VDDA)	0.85	0.9	0.95	V	
Digital interface Supply Voltage (VDD18)	1.7	1.8	1.9	V	
High-speed output buffers Supply Voltage (VDD12)	1.1	1.2	1.3	V	
Total ASIC power dissipation	---	1.1	---	W	
Total ASIC power dissipation without raw data output	---	400	---	mW	
Single ADC power dissipation	---	11.7	---	mW	Without JESD204B interface
Temperature range (junction)	-40	---	110	C	
ESD (HBM)	2			kV	Low speed I/Os and DC
ESD (HBM)	1			kV	High-speed I/Os
End of life (EoL)	10	---	---	Y	@110C
Package		15x15 BGA			Same as for previous ASIC
TID immunity	500	---	---	Krad	
SEE immunity	---	---	---	---	SEL is expected to be eliminated by using <1V power supply

RAW ADC DATA OUTPUT

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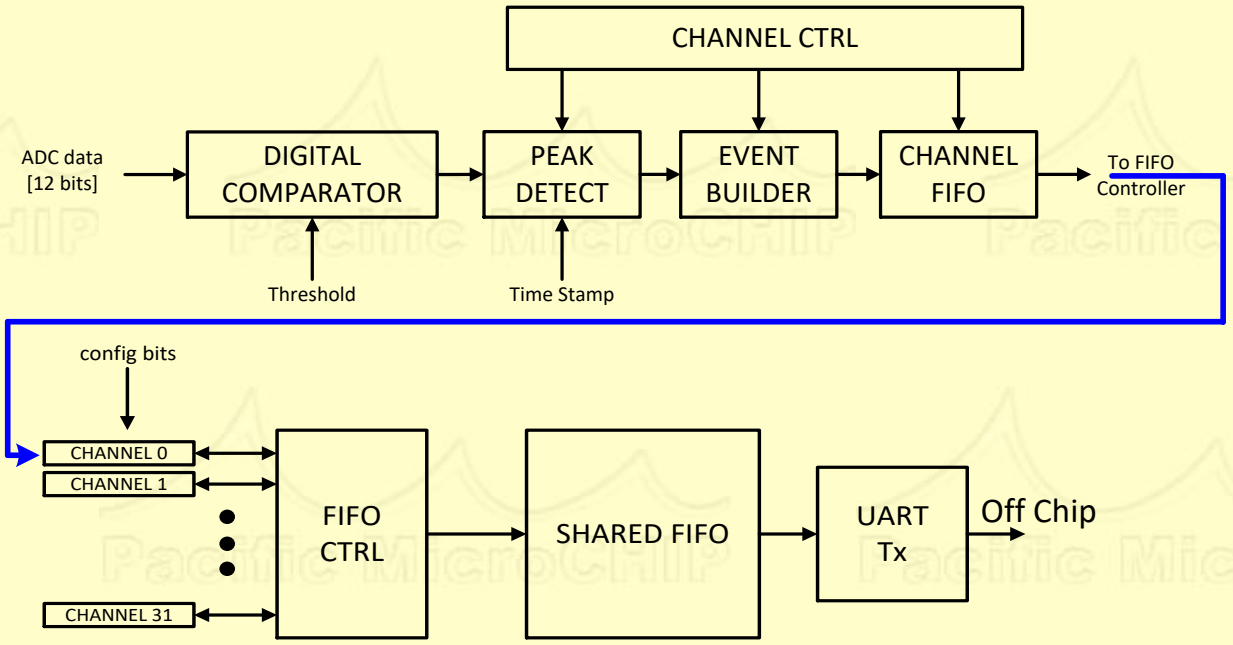
Mode	JESD 204B lanes	ADC per lane	Lane data rate	ADC data rate
Full speed	16	2	6.4Gbps	200MS/s
Half speed	8	4	6.4Gbps	100MS/s
Quarter speed	4	8	6.4Gbps	50MS/s

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate 6.4Gbit per second
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

EVENT–DRIVEN BACKEND

- This ADC output is monitored by a digital comparator with a programmable threshold
- When the ADC input exceeds threshold, a time stamp is assigned, and the peak value of the incoming ADC data is recorded.

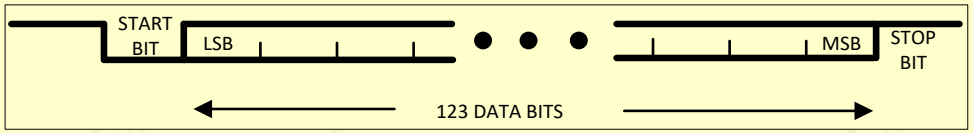


Event-driven digital backend was built in collaboration with LBNL. And we want to thank Dr. Carl Grace for his effort.

- When the event is completed, the relevant information is assembled into a packet by the Event Builder block. When the shared FIFO is ready, events stored in the channel FIFO are read out.

OUTPUT DATA FRAME

Bits	Field Name	Comment
[123]	Parity	Used to monitor integrity of data transmission.
[122]	Event Declaration	0 → test event (see text), 1 → normal
[121:119]	Fixed	Fixed bits - should always read value 3'b011
[118:107]	Window Interval	Determines the number of ADC samples to examine looking for a peak.
[106:102]	Channel ID	5-bit unique identifier.
[101:54]	TOA (Time of Arrival)	The timestamp of where the ADC value passed the threshold. Covers ~16 days at a 200 MHz clock rate.
[53:42]	TOP (Time of peak)	Supports shaper peaking times of up to 20 µs at a 200 MHz clock rate.
[41:30]	TOT (Time over Threshold)	Supports shaper pulse widths of up to 40 µs at a 200 MHz clock rate.
[29:18]	Peak Value	12-bit peak value recorded in the event.
[17:6]	Channel Threshold	12-bit threshold value used during this event.
[5:0]	Shared FIFO usage	For diagnostics and debugging.



50Mbps / 124+2bit / 32ch
≈ 12.4k events per second per channel

PHASE IIB PROJECT OBJECTIVE

The performance parameters of the 1st Gen ASIC are required to be improved in order for the device to be used commercially. Several design mistakes were identified during the chip testing and must also be addressed within Phase IIB in the 2nd Gen ASIC and the evaluation PCB.

Phase IIB objective	Status
Fix issues discovered during 1st Gen ASIC evaluation	Done
Redesign and fabricate the chip (2nd Gen).	Done
Package the chips.	Done
Update the design and fabricate new PCB.	Done
Test and characterize the 2nd Gen ADC ASIC.	Done
Prepare updated datasheet and evaluation board for marketing.	Done
Submit deliverables to the DoE.	Done

ISSUES ADDRESSED WITHIN PHASE IIB PROJECT

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#	Issue Description	Comments	Status
1	VREF/VDDIO bumps are swapped on the chip. As a result, these bumps are incorrectly connected on the PCB.	Significant modification to the PCB is needed.	Fixed
2	An offset calibration FSM does not take into account the 3 MSBs of the 12+1bit ADC output code which uses thermometric encoding to 2 bits, resulting in the 12-bit data. Thus, the 2MSBs of the output data do not behave as the other binary weighed bits. As a result, the calibration algorithm leads to overflow. Consequently, resulting codes for offset adjustment are either at the minimum or maximum possible value.	A modified algorithm was implemented in the CPU and tested. It appears to work as expected. It needs to be implemented on the chip.	Fixed
3	An ADC sampling clock frequency divider is built into the clock distribution network of the ASIC. However, the frequency of the clock going to the DSP is not scaled down proportionally with the divided clock frequency. Thus, using any other than a default clock frequency division option makes the pulse detection to malfunction.	An equivalent frequency divider has to be implemented for the digital clock.	Fixed
4	An older CPU with a bug was implemented on the ASIC. The bug prevents the CPU from executing the first instruction properly and to read back the program memory through the I2C interface after writing it.	The CPU needs to be updated to the most recent version.	Fixed
5	The two inverted (N) outputs of the offset compensation DAC are shorted together. This causes much greater offset compared to what can be compensated. This was confirmed through Monte-Carlo simulations.	After removing the short using FIB, the offset compensation showed performance much closer to what was expected.	Fixed
6	It was found that the comparator design has a missing wire between differential offset cancellation transistors. This causes the offset compensation range to be slightly smaller than expected.	The bug needs to be fixed in the ADC.	Fixed
7	A clock duty cycle adjustment is sensitive to the power supply voltage, when, for example, the UART is injecting noise to the digital power supply. This is verified by observing the noise floor improvement when the UART is switched off. Additionally, if more delay cells are used to lower the duty cycle, the spur power increases on the ADC output spectrum.	The duty cycle generator block's sensitivity to the power supply voltage should be reduced.	Fixed
8	When the power supplies of the ASIC are switched off, the VREF voltage has a low-impedance path to ground. This can cause excessive power dissipation from a reference voltage, and damage system components. The VREF voltage should be applied after the ASIC is powered on.	A circuit is needed to prevent the VREF low-impedance path when the ASIC is off.	Fixed
9	When the Radj code for the input LPF is set to 0, the termination resistor to the on-chip VCM generator is in the Hi-Z mode. In this mode, the external VCM controls the input to bootstrap the sampling switch, but the VCM for bootstrap switch output is still set from the internal VCM.	The bootstrapped switch VCM circuit should be improved for better stability and control of the VCM.	Fixed
10	The UART clock and data outputs operate at 50MHz. Implemented output buffers are not capable of driving a significant external load. This requires external buffers to be implemented on the PCB.	The output buffer driving capacity should be improved.	Fixed

CHIP FLOORPLAN AND LAYOUT

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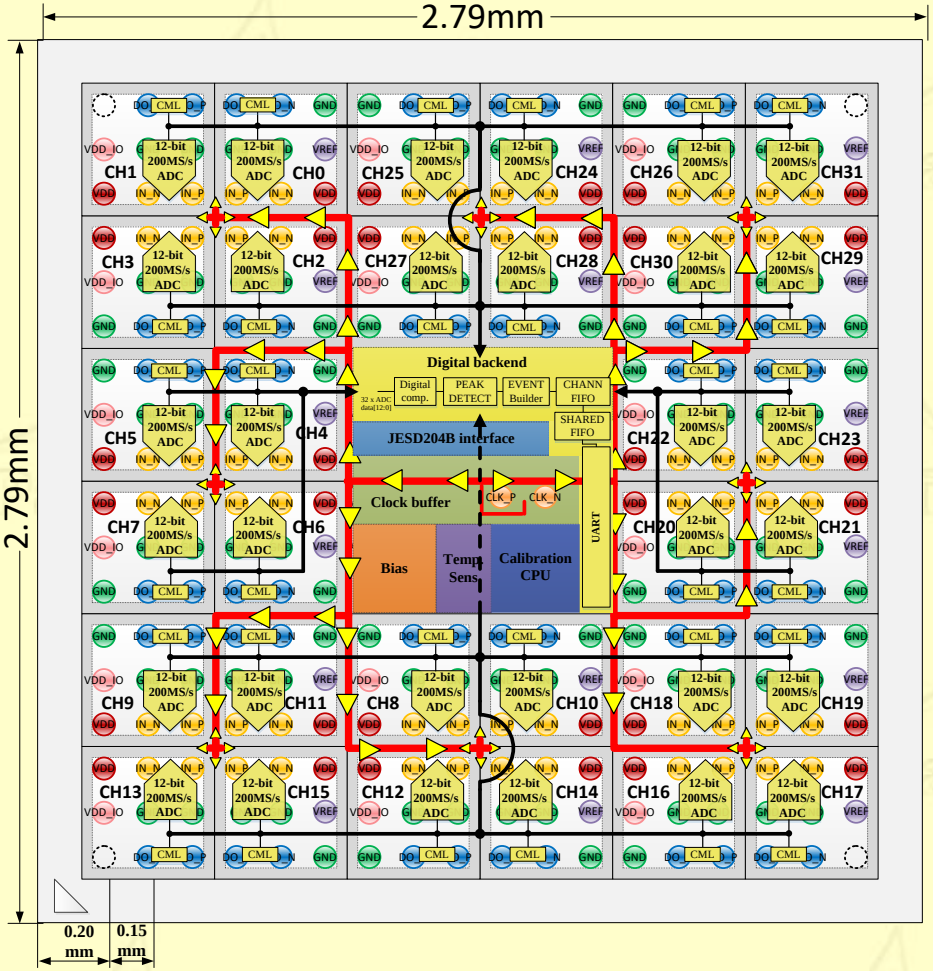
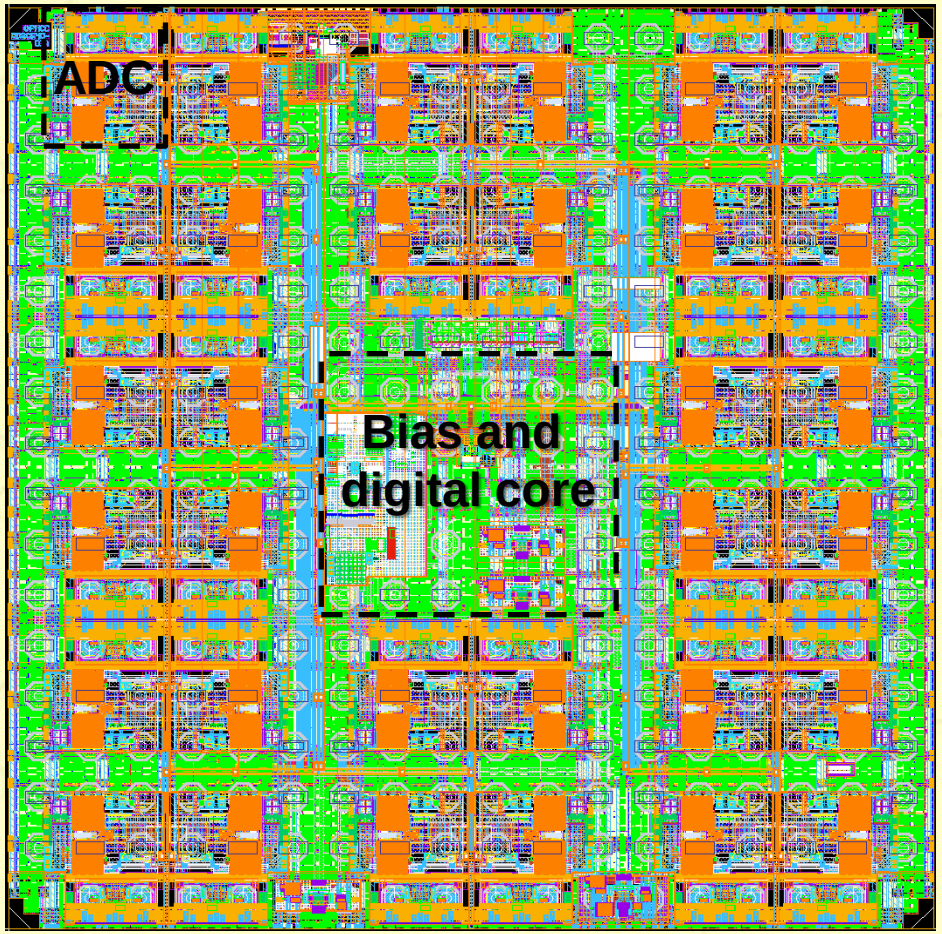
ASIC top level floorplan:



2nd Gen ASIC top level layout:



2nd GENERATION CHIP AND ASSEMBLED PART

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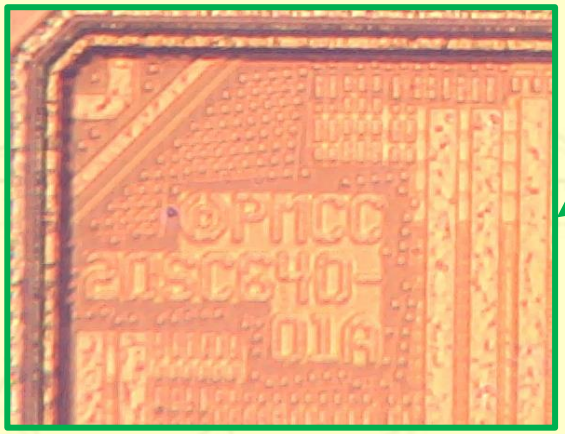
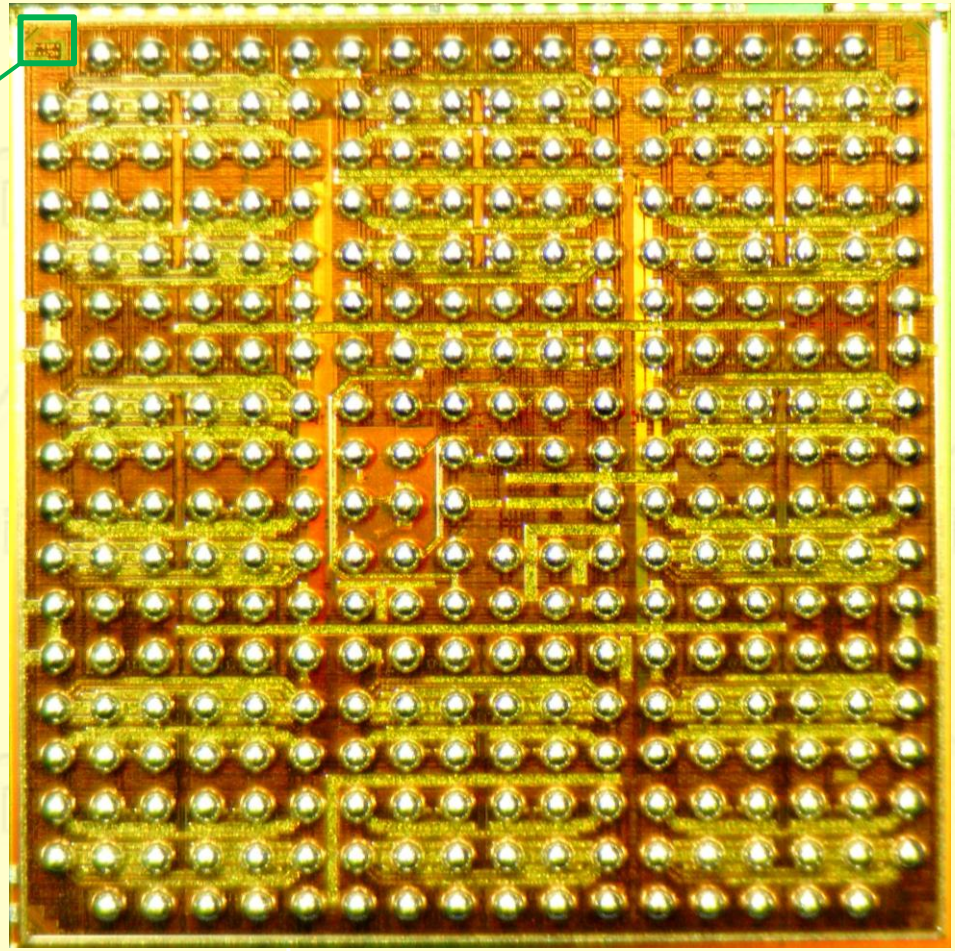
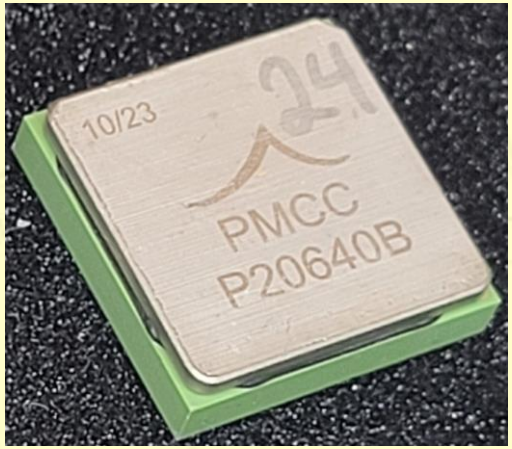
2nd Gen ASIC label @PMCC20SC640-01A



2nd Gen ASIC bumps



P/N: P20640B



2nd GEN ASIC TESTBENCH SETUP

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Signal generator

Test PCB

Clock source
200MHz and 3.2GHz

GUI

Power supply

JESD204B INTERFACE VERIFICATION TESTBENCH

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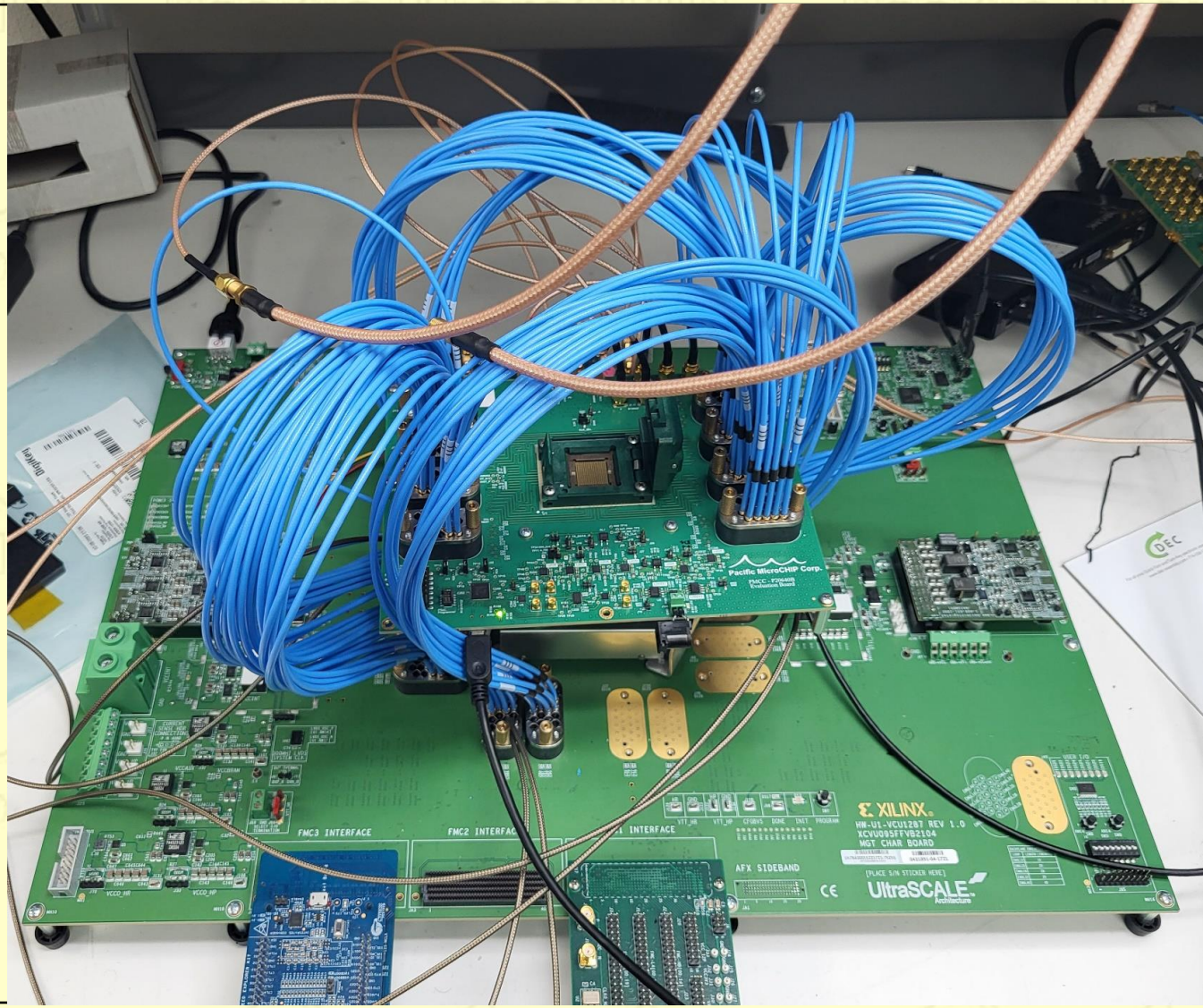
VCU1287 FPGA PCB along with the P20640B ASIC evaluation PCB. This FPGA board was used to generate 32 pulse channels and receive 16 JESD204B data lanes.

Only 17 out of the 97 assembled chips have reliable JESD204B data stream at the default 900mV supply voltage. If the supply voltage is increased to 950mV, the JESD204B link operates reliably in 49 ASICs.



AUTOMATED TESTBENCH SETUP

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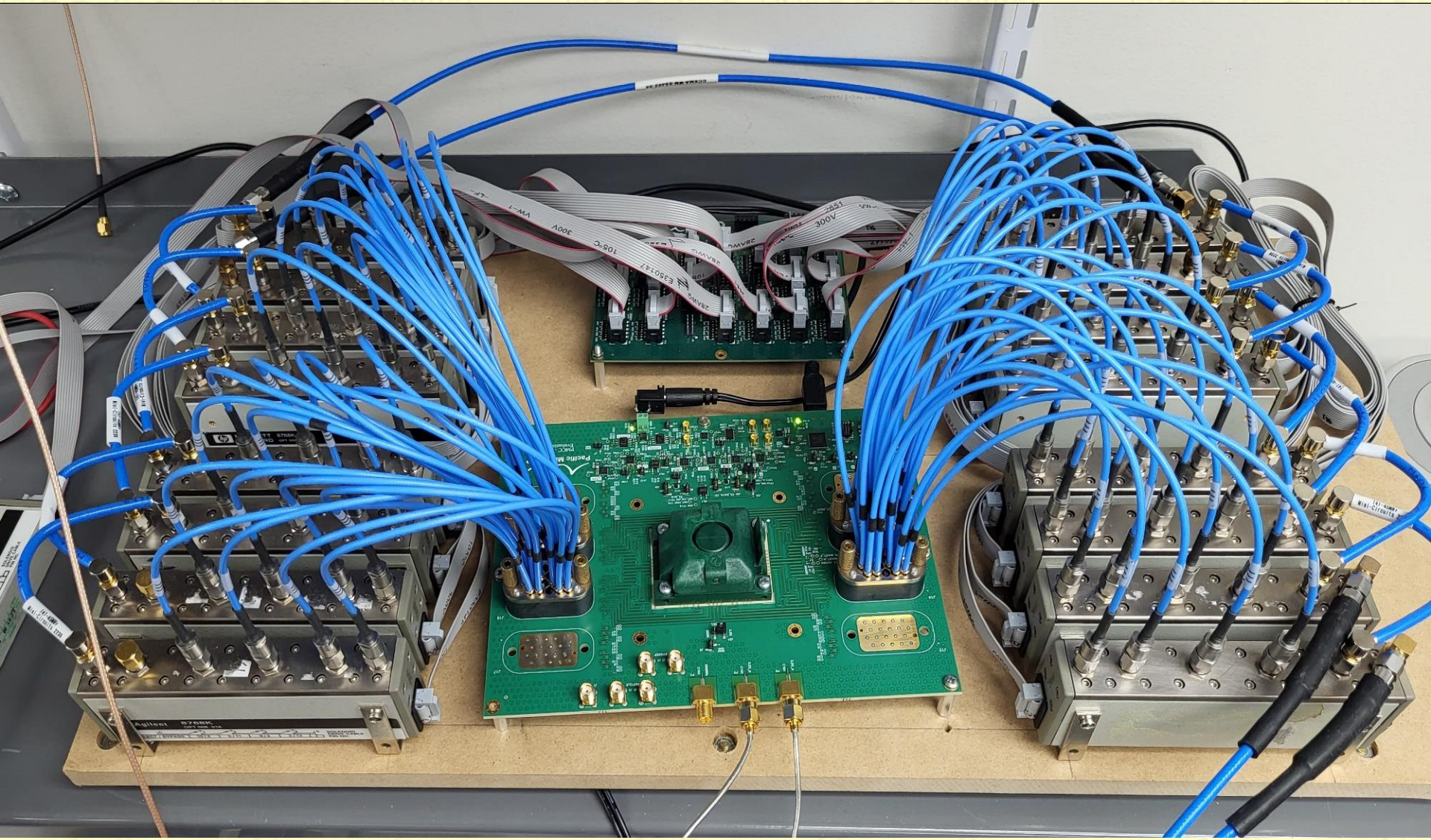

EVENT DRIVEN DIGITAL BACKEND TEST RESULTS

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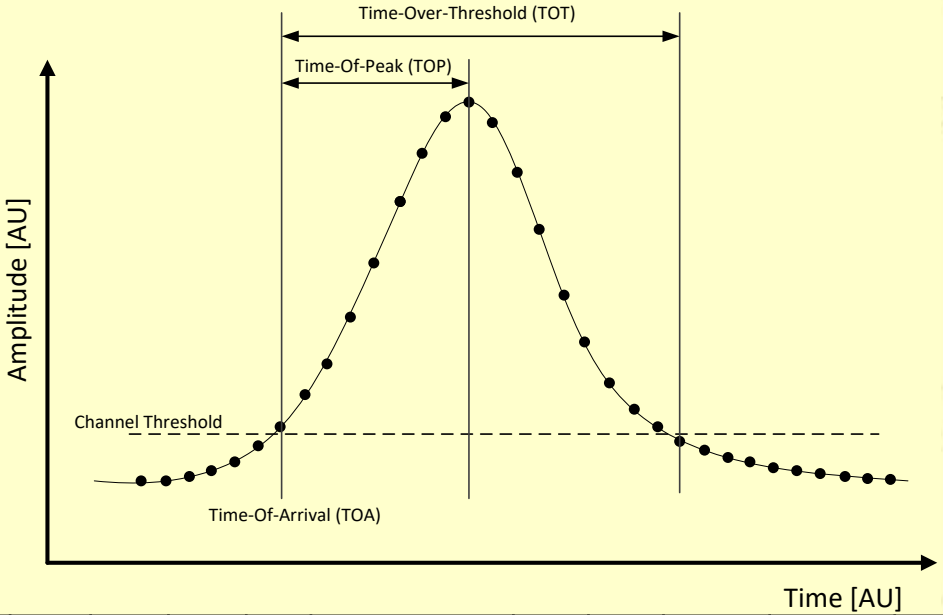
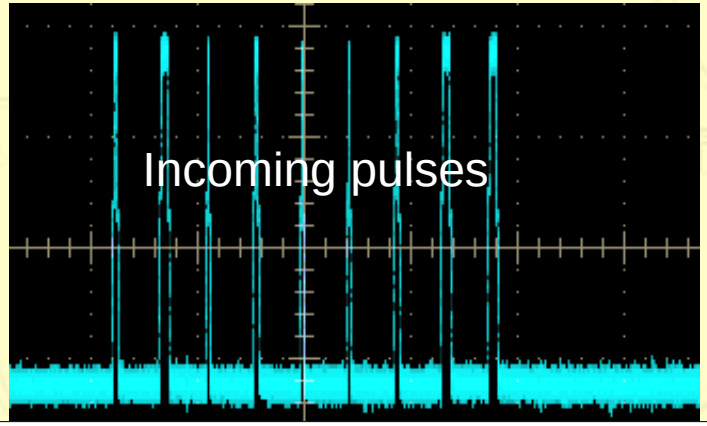
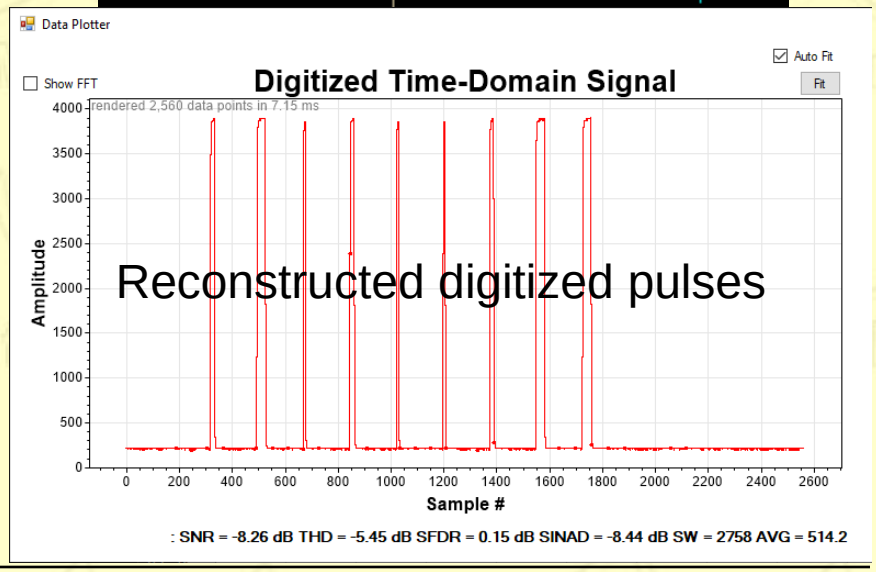
The event-driven backend was designed in collaboration with Dr. Carl Grace of LBNL. It is capable of extracting the TOT, TOP, TOA, and the peak amplitude of incoming pulse signals.





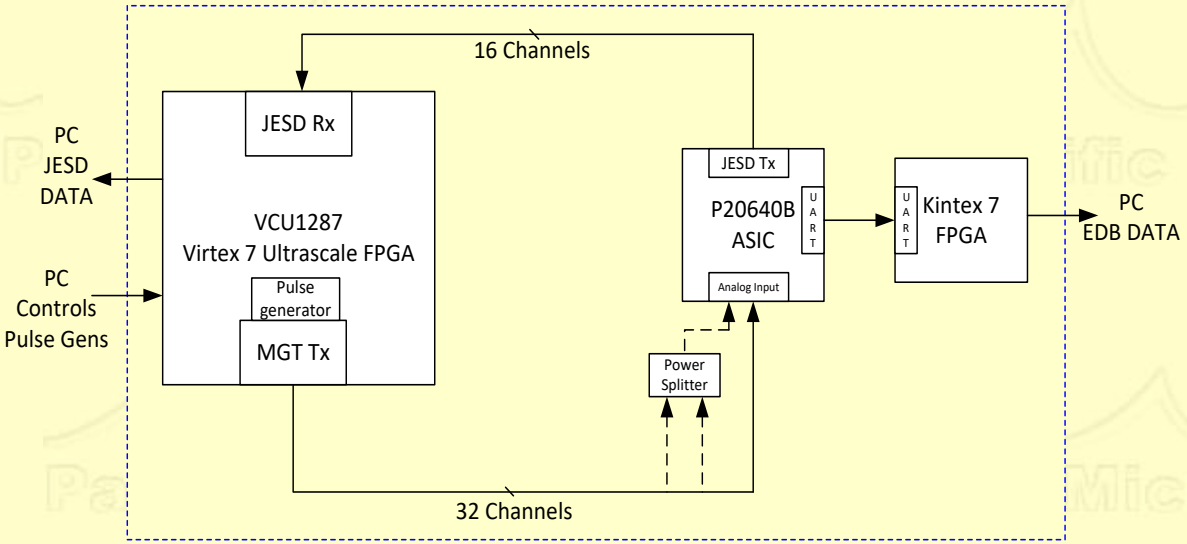


Par0	Event	Fixed	Wind	CH	TOA	TOP	TOT	PEAK	THRESHOLD	SHARED
1	1	3	64	4	578680317105	13	17	3893	1024	0
1	1	3	64	4	578680317281	11	33	3893	1024	0
1	1	3	64	4	578680317457	6	9	3861	1024	1
0	1	3	64	4	578680317633	13	17	3893	1024	1
0	1	3	64	4	578680317809	6	9	3861	1024	2
1	1	3	64	4	578680317985	6	9	3861	1024	3
1	1	3	64	4	578680318161	14	17	3893	1024	3
1	1	3	64	4	578680318337	14	33	3893	1024	4
0	1	3	64	4	578680318513	31	33	3904	1024	5

EVENT DRIVEN BACKEND VERIFICATION

- To test the event driven back-end (EDB) functionality, 32 pulses were supplied to the ASIC input.
- Pulses were generated using a Virtex 7 Ultrascale FPGA on the VCU1287 evaluation platform.
- The EDB data, which is streamed through the UART interface, was captured using a Kintex 7 FPGA on Genesys-2 evaluation board.
- Multiple pulse generator outputs were combined using a power splitter. This allowed different pulse amplitudes to be produced.

The test bench setup for the EDB verification



EVENT DRIVEN BACKEND VERIFICATION

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Raw data
518500f6b811a05a032030030030030
e07902d0300304f00d20500320304d8

Channel id	0	
Fifo Counter	0	

Packet id	10
Packet id	11

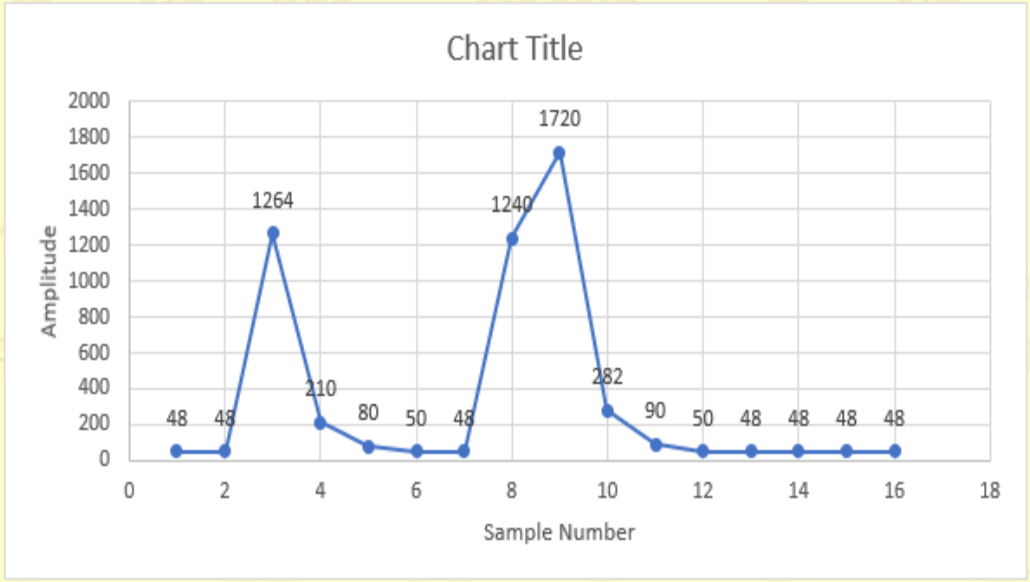
Samples	hex	decimal
0	30	48
1	30	48
2	4f0	1264
3	0d2	210
4	50	80
5	32	50
6	30	48
7	4d8	1240
8	6b8	1720
9	11a	282
10	05a	90
11	32	50
12	30	48
13	30	48
14	30	48
15	30	48

	[29:26] ('b)	[25:20]	[19:6]	[5:0]	
TOA	4'b1001	6'b101101	14'b10001100001010	6'b01111	325869903

Peak Mode

Peak location 9
Threshold 64
Pre samples 8

small pulse width 4ns
Big pulse width 8ns



The samples for pre/post event represent the two supplied pulses, as expected. The operation mode was configured for 8 pre-event samples before the peak.

EVENT DRIVEN BACKEND VERIFICATION

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A pulse was applied simultaneously to 14 analog input channels.
Each pulse occurred at approximately the same time (TOA). The pre-sample setting was set to 11.

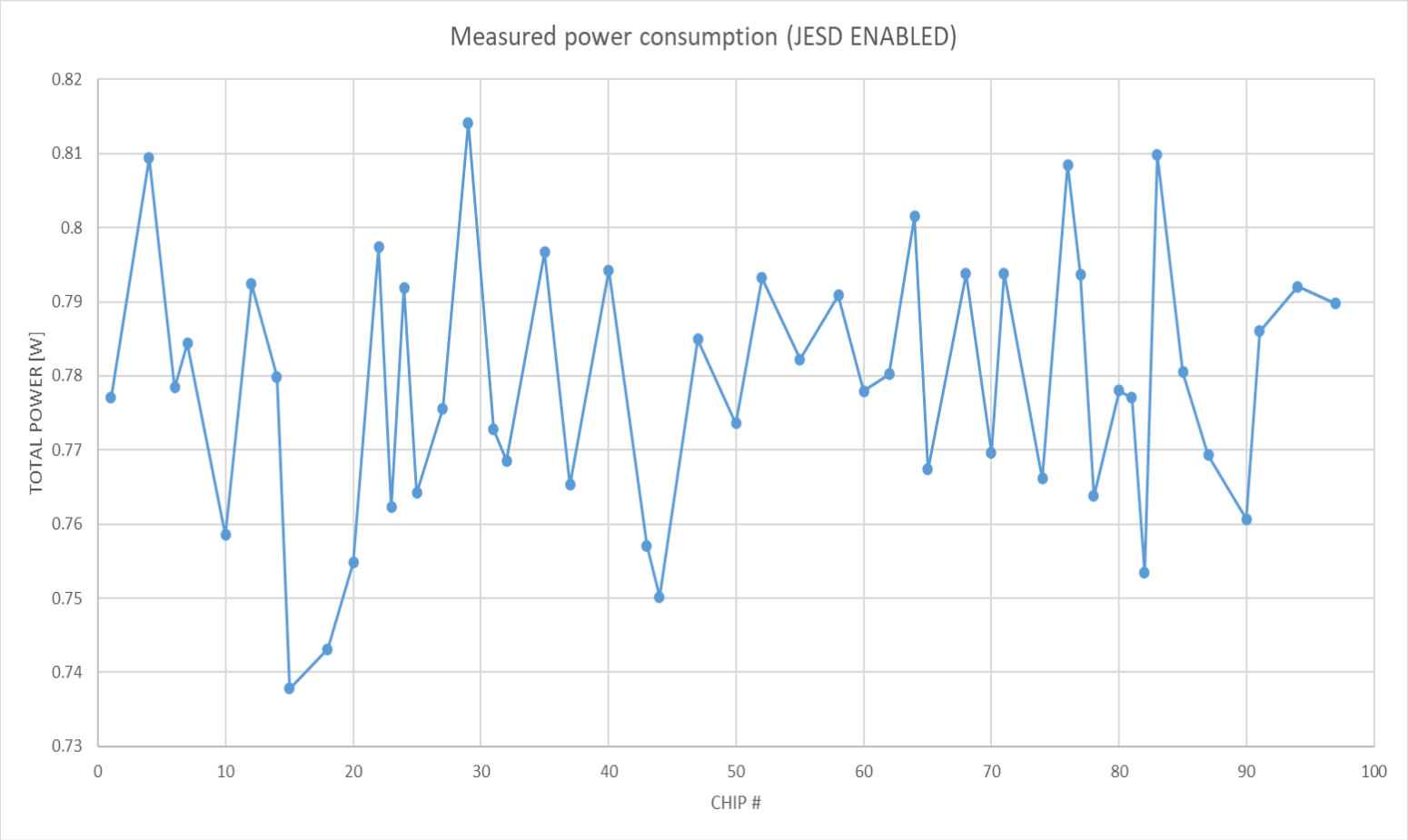
Partiy P1	Parity P1	Parity P2	Parity P2	Packet ID P1	Packet Id P2	Channel Id P1	Channel Id P2	Time of Arrival	FIFO Counter	Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	Sample 8	Sample 9	Sample 10	Sample 11	Sample 12	Sample 13	Sample 14	Sample 15
1	1	0	0	2	3	10	10	274294741	0	0	0	0	0	0	0	0	0	0	0	0	2832	560	0	0	0
0	0	1	1	2	3	0	0	274294742	1	0	0	0	0	0	0	0	0	0	3500	4024	4088	561	27	0	0
1	1	1	1	2	3	1	1	274294742	3	0	0	0	0	0	0	0	0	0	0	0	3416	2832	255	0	0
0	0	1	1	2	3	2	2	274294742	5	16	16	16	16	16	16	16	16	16	16	16	3500	1270	176	48	19
0	0	0	0	2	3	3	3	274294743	7	0	0	0	0	0	0	0	0	0	2656	3636	4095	1619	805	0	0
0	0	1	1	2	3	4	4	274294742	9	0	0	0	0	0	0	0	760	3640	4040	4091	4095	1023	112	10	0
1	1	0	0	2	3	5	5	274294742	11	0	0	0	0	0	0	3048	3954	4072	4094	4095	4095	2958	375	31	4
0	0	1	1	2	3	8	8	274294742	13	0	1736	3880	4095	4095	4095	4095	4095	4095	4095	4095	4095	3690	380	0	0
0	0	1	1	2	3	9	9	274294742	15	0	0	0	0	0	0	0	3056	3544	4095	4095	4095	959	222	0	0
1	1	0	0	2	3	11	11	274294742	17	0	0	0	0	3468	4006	4074	4090	4094	4094	4095	4095	587	63	19	3
1	1	0	0	2	3	12	12	274294742	19	0	0	0	3082	3798	3940	4044	4095	4095	4095	4095	4095	3512	727	255	81
1	1	1	1	2	3	14	14	274294741	21	0	0	0	0	2854	4048	4095	4095	4095	4095	4095	4095	819	0	0	0
1	1	1	1	2	3	15	15	274294742	23	0	0	0	0	0	1616	4060	4095	4095	4095	4095	4095	310	0	0	0

Testing of pulse analysis mode, which provides time of peak (TOP), time over threshold (TOT), and pulse peak values. An example data packet showing a pulse being simultaneously applied to inputs of 14 analog channels

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Parity	Parity Exp	Event Dec	Fixed Bits	Window interval	Channel Id	TOA	TOP	TOT	Peak	Channel Threshold	FIFO Counter	
2	0	0	1	3	100	0	3.83573E+11	9	12	3856	1024	0	
3	1	1	1	3	100	1	3.83573E+11	11	13	3910	1024	0	
4	0	0	1	3	100	2	3.83573E+11	12	11	3714	1024	0	
5	1	1	1	3	100	3	3.83573E+11	4	13	3784	1024	0	
6	1	1	1	3	100	4	3.83573E+11	4	13	3854	1024	0	
7	0	0	1	3	100	5	3.83573E+11	10	12	3850	1024	0	
8	1	1	1	3	100	8	3.83573E+11	11	12	3939	1024	0	
9	1	1	1	3	100	9	3.83573E+11	11	12	3948	1024	0	
10	0	0	1	3	100	10	3.83573E+11	10	12	3888	1024	0	
11	1	1	1	3	100	11	3.83573E+11	12	10	3822	1024	0	
12	1	1	1	3	100	12	3.83573E+11	3	13	3992	1024	0	
13	0	0	1	3	100	14	3.83573E+11	10	12	3940	1024	0	
14	1	1	1	3	100	15	3.83573E+11	4	12	4095	1024	0	
15	1	1	1	3	100	0	3.83573E+11	4	6	3832	1024	12	
16	1	1	1	3	100	1	3.83573E+11	6	0	3888	1024	12	
17	1	1	1	3	100	2	3.83573E+11	5	6	3688	1024	12	
18	0	0	1	3	100	3	3.83573E+11	3	7	3793	1024	12	
19	0	0	1	3	100	4	3.83573E+11	3	6	3848	1024	12	
20	1	1	1	3	100	5	3.83573E+11	5	0	3840	1024	12	
21	1	1	1	3	100	8	3.83573E+11	5	6	3929	1024	12	
22	1	1	1	3	100	9	3.83573E+11	4	5	3952	1024	12	
23	1	1	1	3	100	10	3.83573E+11	5	6	3865	1024	12	
24	0	0	1	3	100	11	3.83573E+11	5	6	3812	1024	12	
25	1	1	1	3	100	12	3.83573E+11	3	6	3992	1024	12	
26	1	1	1	3	100	14	3.83573E+11	6	5	3920	1024	12	
27	0	0	1	3	100	15	3.83573E+11	2	5	4095	1024	12	
28	0	1	0	0	0	0	0	0	0	0	0	0	

ADC PERFORMANCE FOR ALL CHANNELS

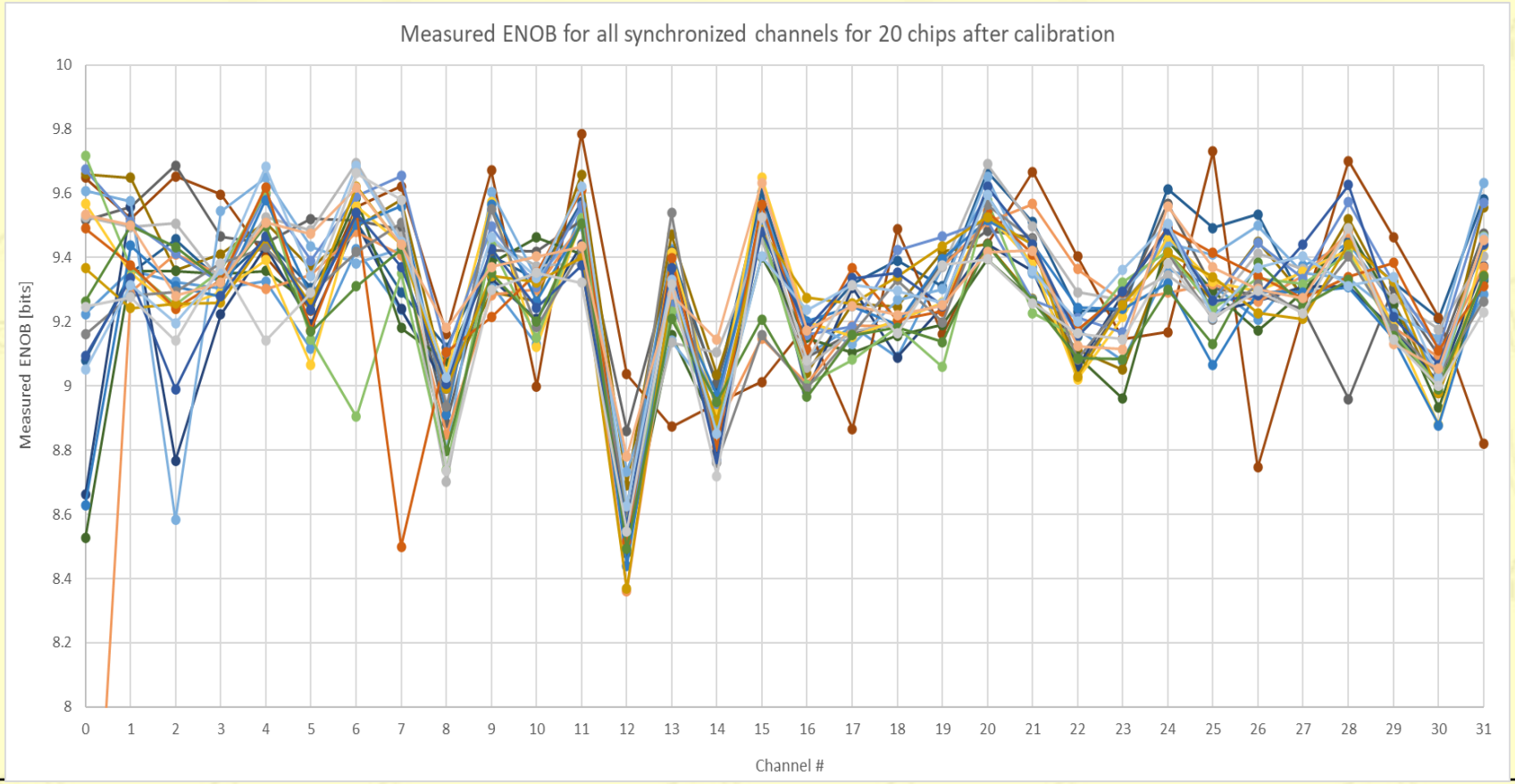
When the JESD204B interface is enabled, and 950mV is used to power the digital core to avoid the JESD204B interface issues, the typical power consumption of the ASIC is 780mW. This number averages to approximately **24.5mW per ADC channel**.



ADC PERFORMANCE FOR ALL CHANNELS

Pacific MicroCHIP Corp.

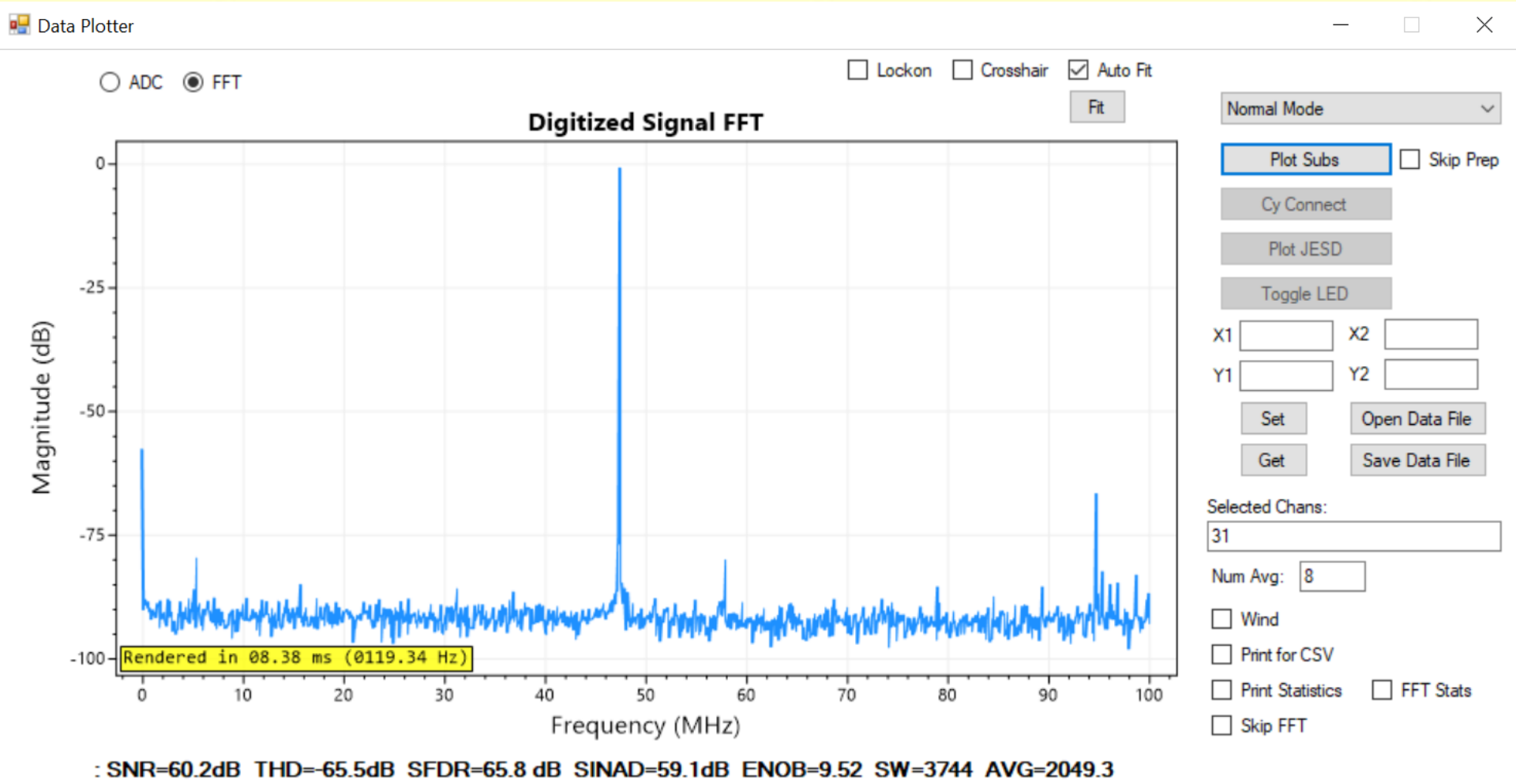
Measured ENOB value for all 32 ADC channels of 20 chips. Impact of the ADC switching cross-talk:
ADC channel #20 has a minimum ENOB value of 9.4 bits in all chips. However, the channel #30 has a maximum ENOB of 9.2 bits. If the channels were desynchronized, the channel #20 can show less than 9 bits of ENOB, while the channel #30 can show up to 9.7 bits of ENOB.



TESTING RESULTS:
ADC OUTPUT SPECTRUM CH 31

Pacific MicroCHIP Corp.

Channel 31 <u>after calibration</u>: SFDR 65.8dB / ENOB 9.52 / SNR 60.2dB



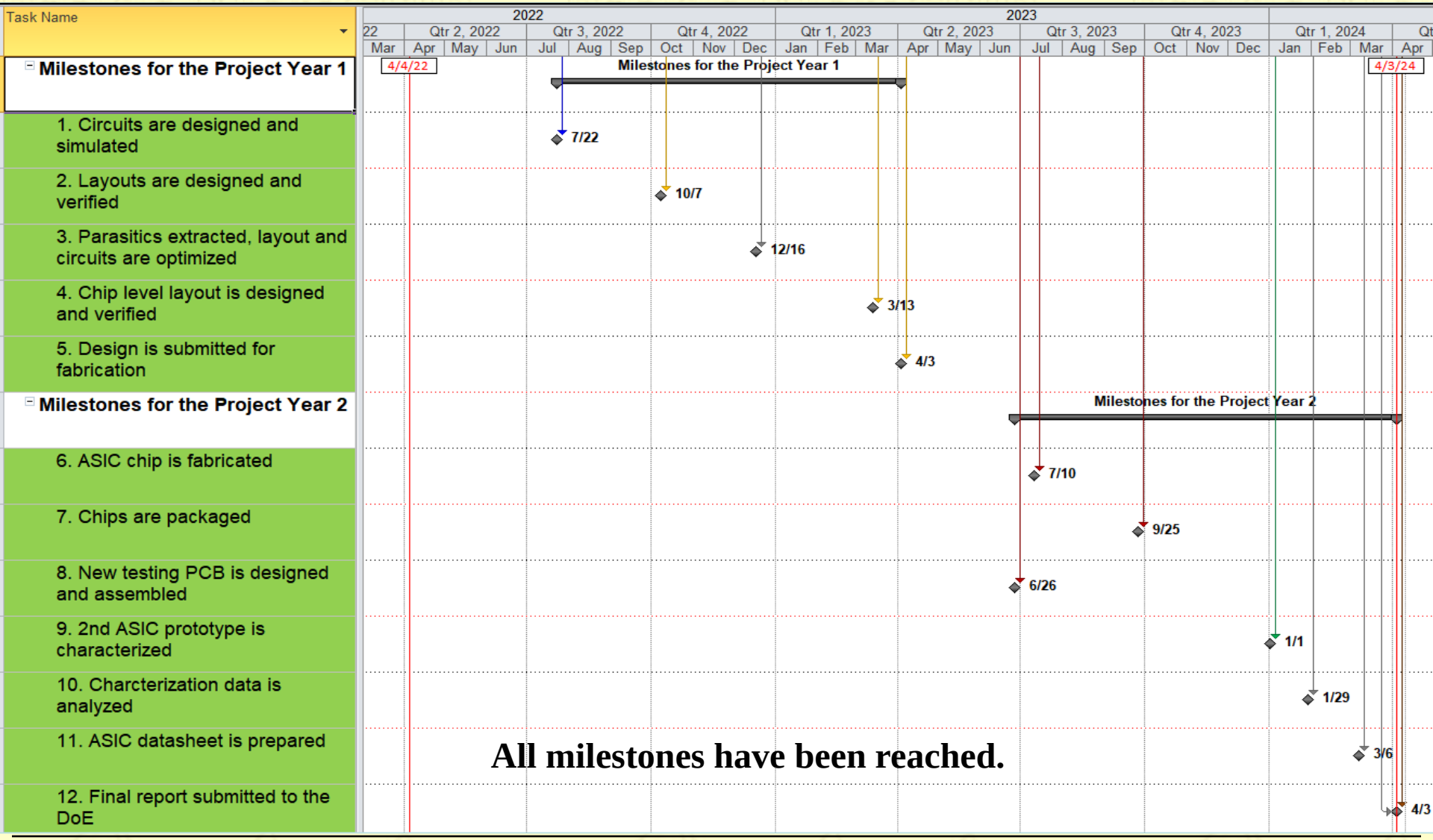
TESTING RESULTS:
ADC PERFORNACE SUMMARY

Pacific MicroCHIP Corp.

CHANNEL	CALIBRATION CODES						ADC PERFORMANCE			
NUMBER	CMP 1 ofs	CMP 2 ofs	CDAC C14	CDAC C15	CDAC C16	CDAC C17	SNR (dB)	SFDR (dB)	SINAD (dB)	ENOB (Bit)
0	144	20E	2E	2C	32	2F	59.5	67.5	58.7	9.45
1	164	1D3	2D	2D	35	33	58.7	70.7	58.4	9.41
2	1B7	1DB	2F	2D	35	35	60	67.3	58.9	9.5
3	19B	1D0	2B	27	2F	2D	57.9	72.4	57.6	9.28
4	15B	20A	2D	2B	37	37	59.7	67.7	59	9.51
5	144	22D	2F	2D	31	35	60.2	66.2	59.2	9.54
6	195	23C	30	2F	43	43	59.8	66.8	58.6	9.44
7	15A	201	2D	2D	35	31	59.4	65.5	58.4	9.4
8	14A	1BA	2F	2F	35	31	59.5	68.3	58.9	9.49
9	1B8	218	36	34	38	40	56.4	74.2	56.2	9.04
10	161	1B2	2B	27	2B	2D	59.7	67	58.4	9.42
11	15D	22C	2B	23	2B	2B	57.8	68.1	57.2	9.21
12	155	23B	2D	2B	37	33	60.4	67.7	59.5	9.59
13	1C6	236	2F	35	47	45	57.2	66.7	56.6	9.1
14	181	203	2B	25	2F	2F	59.1	67.8	58.4	9.41
15	1A0	1F3	30	31	37	33	56.9	71.1	56.6	9.12
16	192	1D3	30	34	45	43	58.8	62.7	57.3	9.22
17	142	205	2D	2B	33	33	59	70.3	58.6	9.44
18	162	216	2F	2F	35	35	60.4	66.9	59.2	9.54
19	145	203	2D	25	2D	2D	59.9	67.6	59.1	9.52
20	191	1B5	2D	2F	43	41	59.5	67.4	58.7	9.46
21	1A6	1E4'	2D	25	33	31	59	70.9	58.5	9.43
22	204	20E	31	37	45	47	60.7	67	59.3	9.55
23	147	20B	2D	25	2F	2F	58.8	67	58	9.35
24	1B8	205	2F	2F	41	35	59	66.2	58.2	9.37
25	1A5	202	2E	2E	35	33	61.1	66.6	59.9	9.67
26	182	203	32	33	43	43	59.9	66	58.9	9.5
27	192	1E1'	2B	27	2F	2D	59.6	67.5	58.9	9.49
28	186	1C3	2D	27	2B	2B	60.8	67	59.7	9.62
29	183	21E	2D	27	2D	2B	60.5	66.5	59.3	9.55
30	183	205	33	37	49	49	60.3	65.9	58.6	9.44
31	153	1E3'	2F	31	37	37	61.3	66.9	60.1	9.7

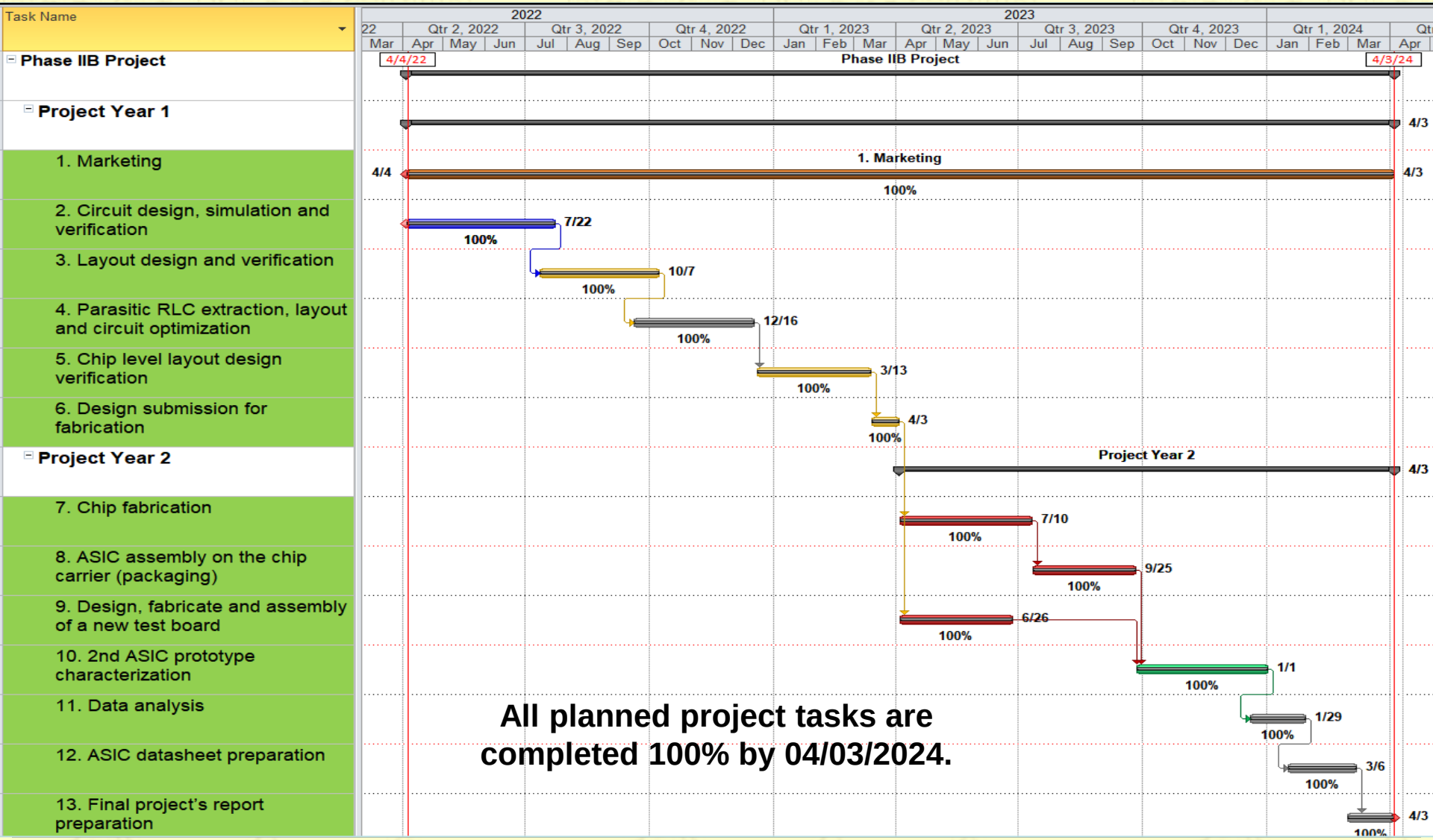
PHASE IIB PROJECT SCHEDULE

Pacific MicroCHIP Corp.



PHASE IIB PROJECT SCHEDULE

Pacific MicroCHIP Corp.



THANK YOU!

Application Ideas for the ADC ASIC are appreciated!