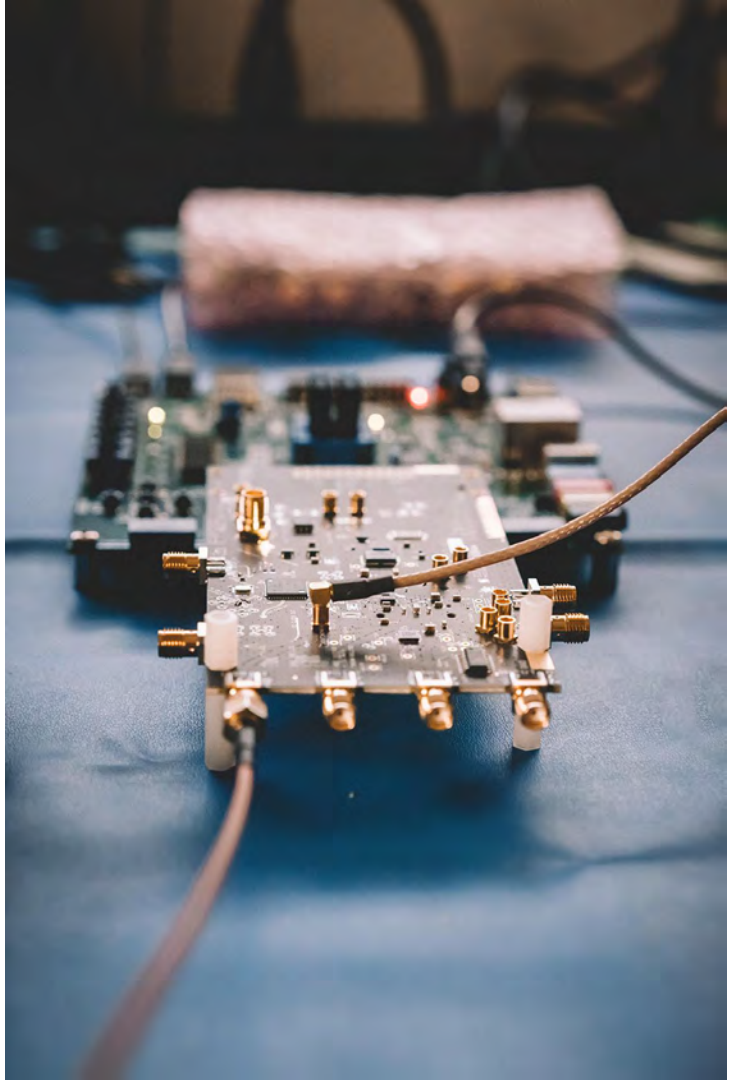


NALU SCIENTIFIC
ENABLING INNOVATION

Design, Fabrication of the HDSoC- High Density Digitizer System-on-Chip

A High channel-density Waveform Digitizer for direct interfacing of optical sensors Application Specific Integrated Circuit (ASIC).

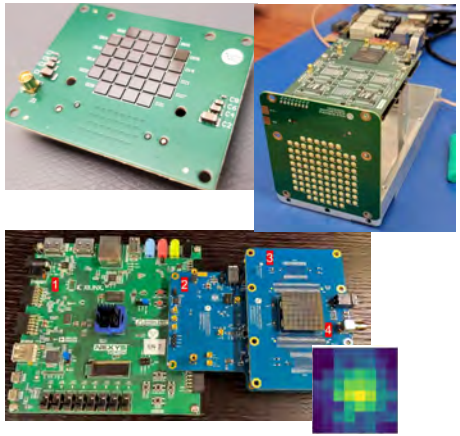
Aug 14, 2024
Isar Mostafanezhad, Ph.D
Founder and CEO at Nalu Scientific LLC

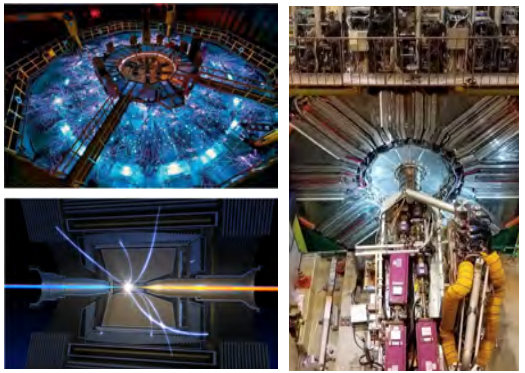
Work funded by DE-SC0020457

NCE: 8/31/24

NALU SCIENTIFIC
ENABLING INNOVATION

Core Technology:
Data Acquisition Microchips





1. Front-end Chips:

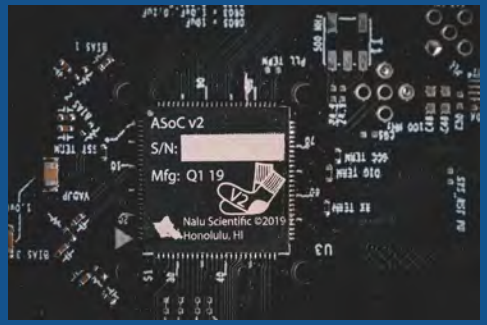
- Event based digitizer+DSP
- 4-64 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

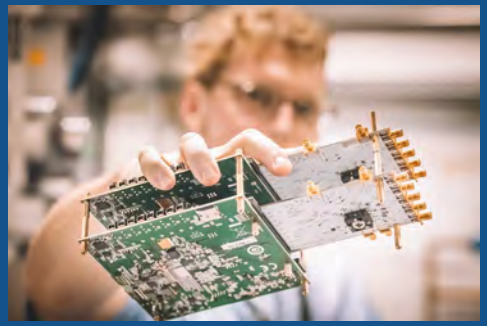
2. Integration:

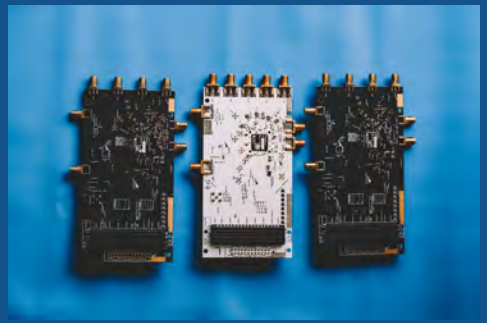
- SiPM
- PMT
- LAPPD
- Detector arrays

3. Applications:

- NP/HEP experiments
- Astro particle physics
- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging







ABOUT NALU SCIENTIFIC

Agile Small Business in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- Staff members with PhDs, MSc, and BSc
- Access to advanced design tools
- Rapid design, prototyping and testing

Vertically Integrated Team:

Microelectronics	Analog + digital System-on-Chip (SoC)
Hardware	Complex multi-layer PCBs
Firmware	FPGAs, CPUs, Embedded
Software	Data science, GUI, documentation
Scientific	Plasma, medical, physicists, space

Past Accomplishments:

- 5x Phase I/II SBIRs transitioned
- Developed microchip from R&D to COTS (available via CAEN)
- 3x US Patents Issued
- Over $3M in non-SBIR sales of products and services

CAEN Technologies Inc.

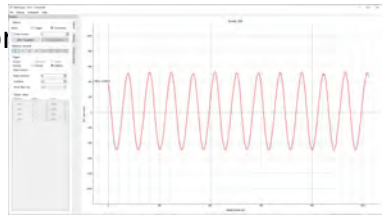
Nalu = 'wave' in native Hawaiian language

NALU SCIENTIFIC
ENABLING INNOVATION

Current ASIC Projects

Project	Sampling (GHz)	BW (GHz)	Buffer (Samples)	Number of Channels	Timing Res. (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-2	0.6	2k	32/64	80-120	Rev 2 avail
AARDVARC	8-14	2.2	16k	8	10	Rev 4 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5	4k	16	10	Rev 1 avail

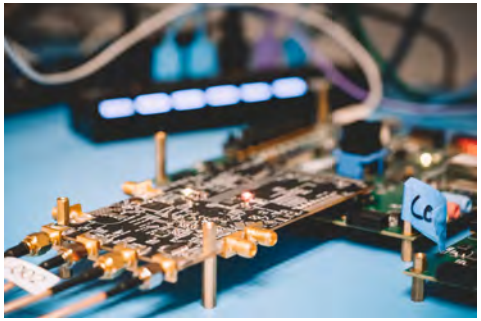
- DOE Phase I/II SBIRs
- Low SWaP-C specialty digitizers for
  - Radiation detection
  - Photonic sensors
  - Time of Flight (ToF)
  - Medical imaging
  - Space
  - Rad hard and harsh
- Evaluation PCBs available
- Extensive suite of software tools
- All microchips and tools available through CAEN Technologies USA



Software

Eval PCB

Microchips



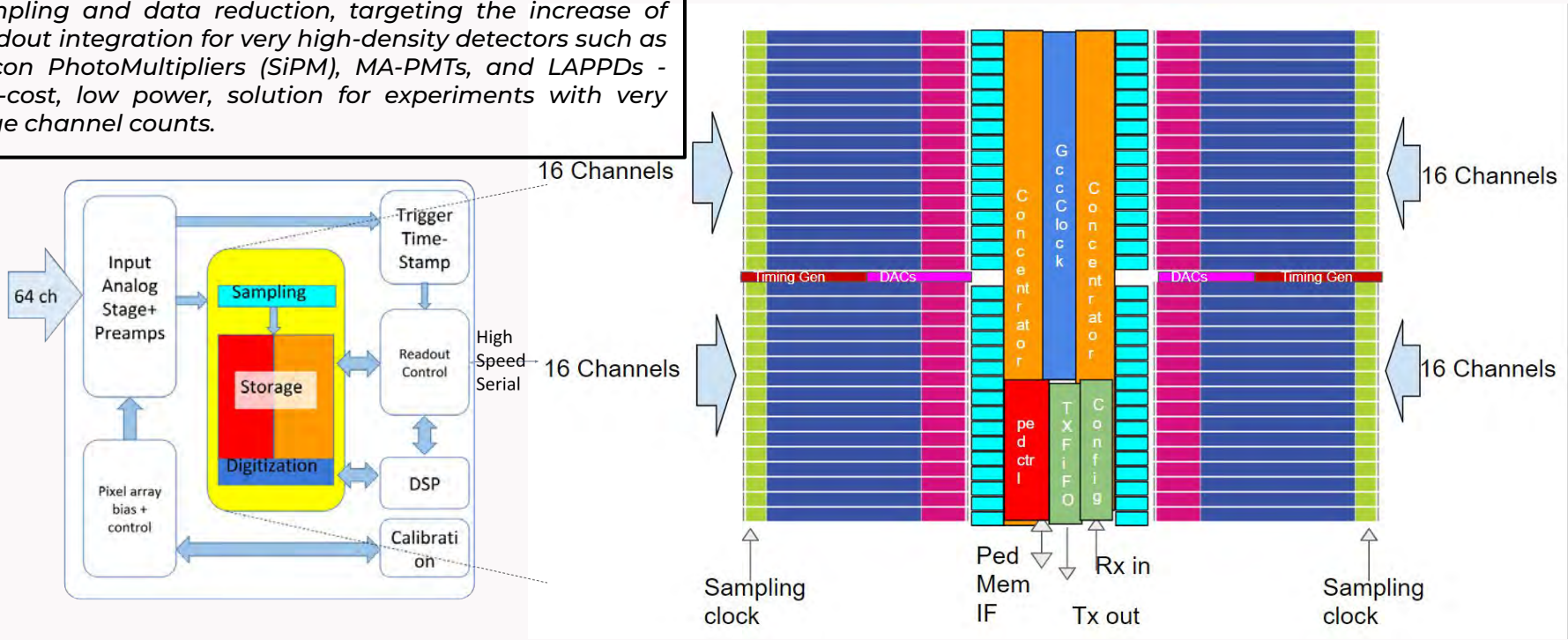
HDSoC project - Summary

- Part I:
  - Topic Introduction - The need
  - HDSoC concept
  - Rev. 1 design and Fabrication
- Part II:
  - Rev. 1 testing fixtures
  - Rev. 1 initial evaluation
  - Rev. 1 extensive testing
- Part III:
  - Rev. 2 Design
  - Rev. 2 Fabrication
  - Rev. 2 Testing
  - Applications and conclusions

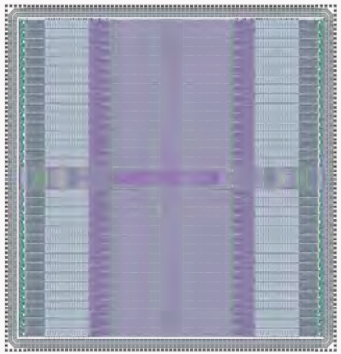
Part I:
High Density Digitizer SoC - concept and Design

64-Channel HDSoC Block Diagram

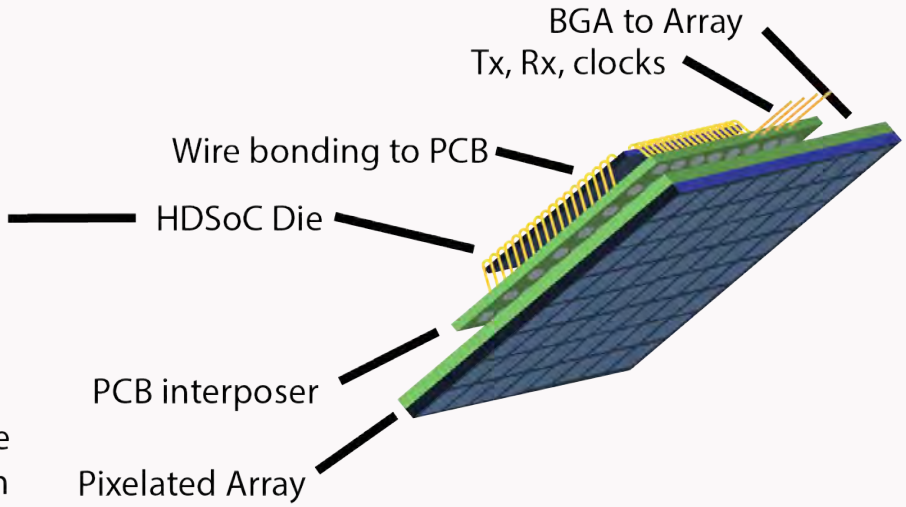
"HDSoC": High channel count ASIC with full waveform sampling and data reduction, targeting the increase of readout integration for very high-density detectors such as Silicon PhotoMultipliers (SiPM), MA-PMTs, and LAPPDs - low-cost, low power, solution for experiments with very large channel counts.



64-Channel HDSoC concept



Nalu Scientific
HDSoC V1 64 channel estimate
64 channel = 7.2 mm x 7.4 mm



HDSoC DESIGN CONCEPT DETAILS

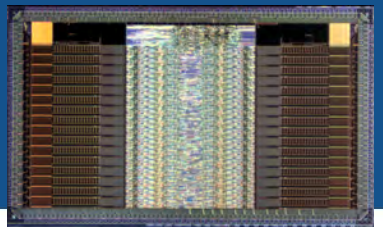
High density waveform digitizer

- High Density: 64 channels (V1:32, V2:64)
- Full waveform sampler and digitizer
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

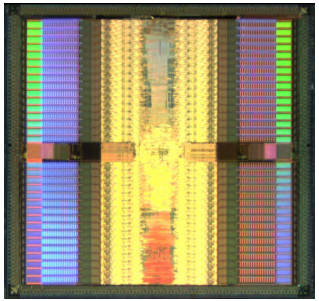
Parameter	Target Spec
Sampling Rate	1-2 GSps
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~2 us (@1Gsps)
Deadtime	0**
Channels	32/64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	20-45mW/ch

- On chip TIA
- Serial interface (up to 500 Gsps)
- Discriminator for self-triggering and zero suppression - exported in dedicated serial stream
- Virtually dead-timeless (buffer virtualization)
- Feature Extraction
- 32 ch and 64 ch proto chips fabricated
- Phase II SBIR almost complete

**If average rates compatible with maximum limits - currently 220kEvents/second



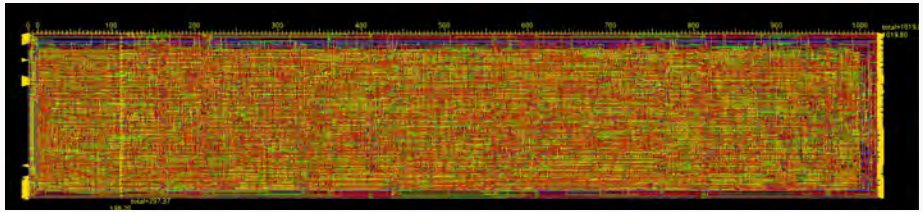
HDSoC v1 die shot



HDSoC v2 die shot

HDSoC Rev. 1 Layout - 32 ch proto

HDSoC Rev. 1 Channel Layout (Mixed signal and digital control)

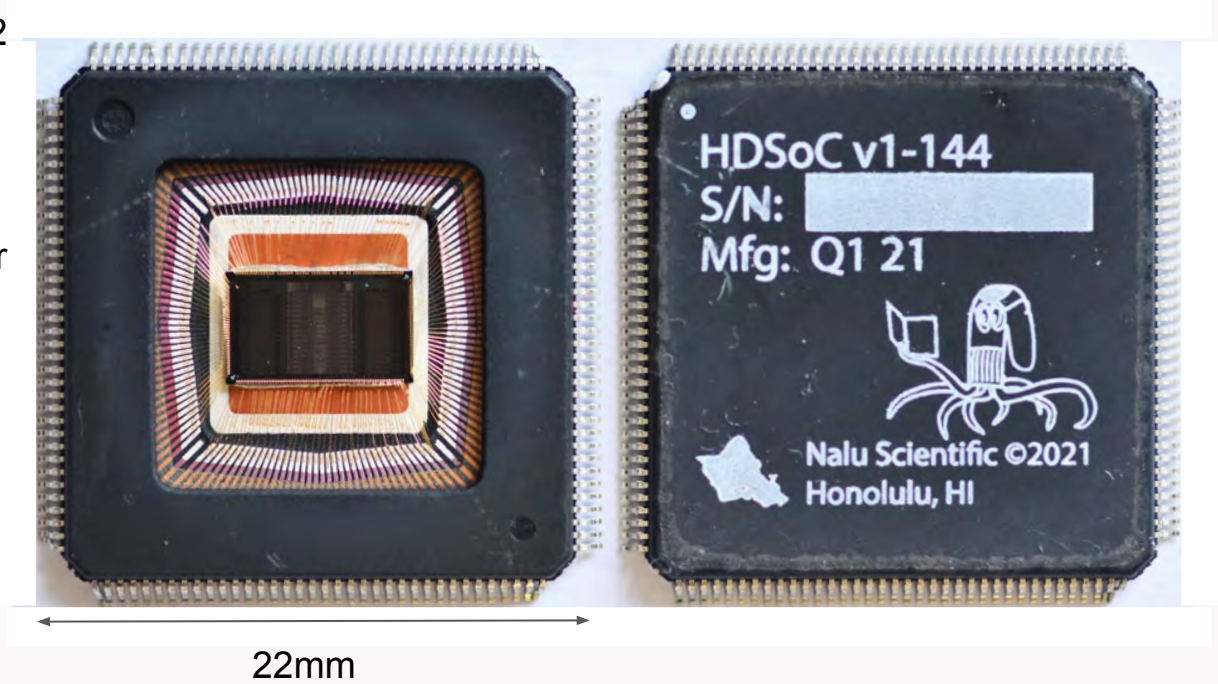


HDSoC Rev. 1 Package

Packaged in QFP144 (22 mm side)
All I/Os connected:

- Serial IF
- Parallel IF

After validation, a smaller package (LQFP128 - 16mm side) with only serial interface can be used. 144 pins are sufficient for the 64 channel device.
A custom package could be used to reduce the footprint.



Part II:
High Density Digitizer SoC Revision 1 Testing

HDSoC v1 specs and Measurements

Specifications	
Sampling Rate	1-2 GSPS
ABW	0.6GHz
Depth/channel	2048 Samples
Trigger Buffer	~2 us
Max rate	14kHz/all channels 220 kHz/hits
Channels	32
Supply/Range	2.5V/0.5-2.0V
ADC bits (stated res.)	12
Timing accuracy	<90ps
Technology	250 nm CMOS
Serial Interface	500MHz
Power	47mW/ch

Confirmed at 1-1.5 GSPS

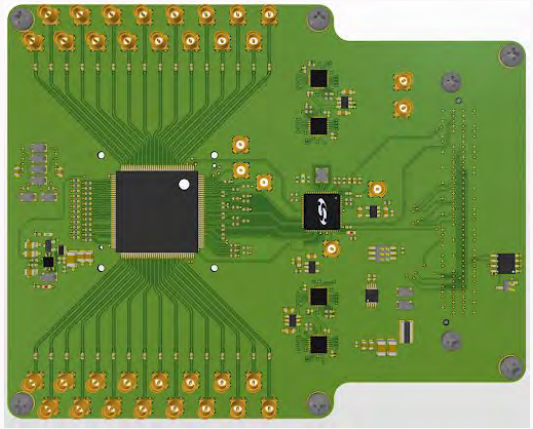
Measured

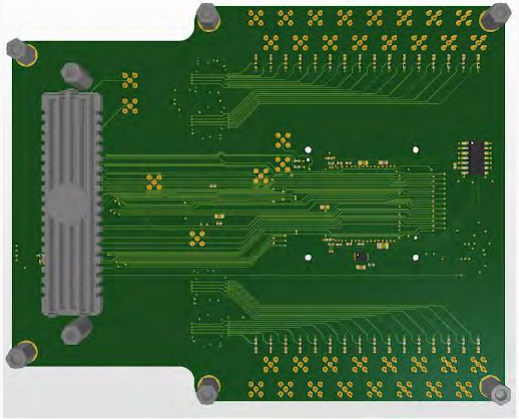
Maximal including header and 8b10b encoding overheads - assumes full readout of 1 window (32 samples) and operation at maximum speed for serial interface (500 Mb/s) and system clock (125 MHz) - current tested limit 13.2kHz @312.5MHz serial interface and 31.25MHz system clock.

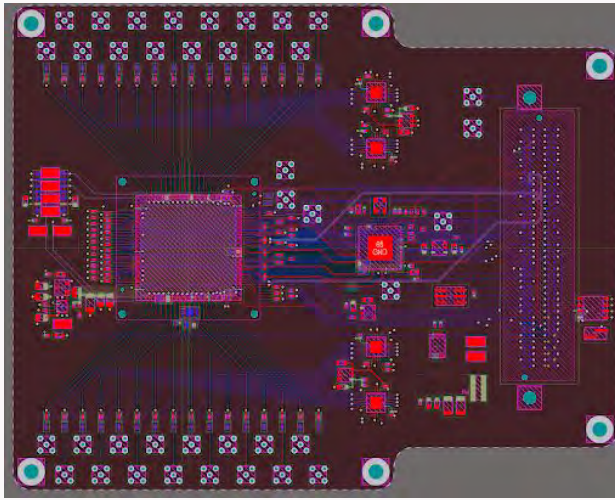
Linear range with ~5 ADC count sigma = 0.8-2.0V

Measured with pulses - currently testing with SiPM
Measured to 312.5MHz
Some sources of extra power identified - reduced in V2
Includes: sensor bias, amplifier, trigger, data transfer.

Test boards Design

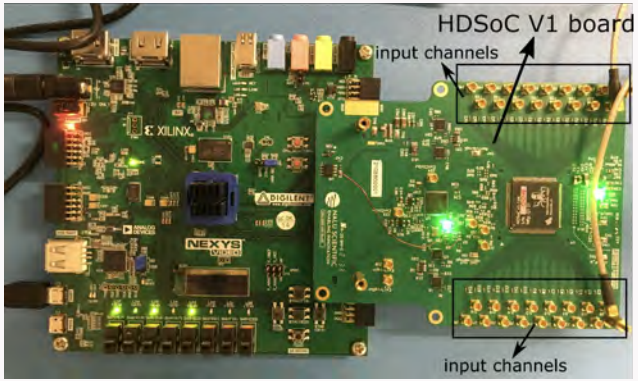




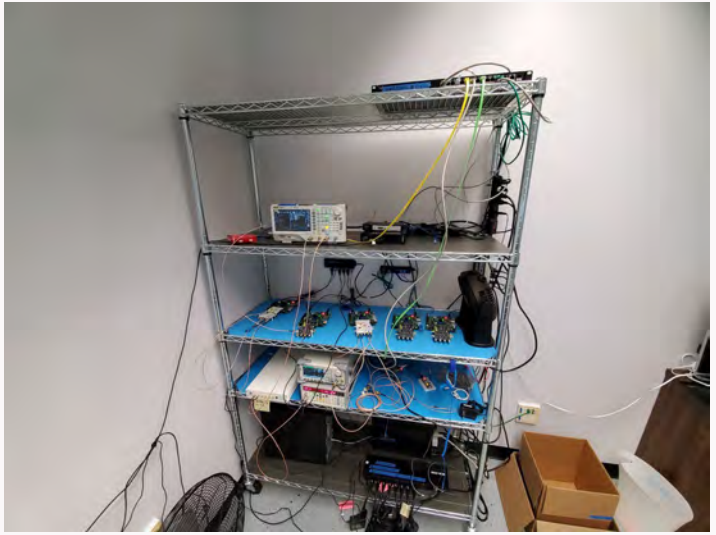


- All 32 channels accessible via MMCX connectors
  - Individual channel biasing
- On board clock generation
- Interface to readout board via standard FMC connector
  - Permits testing of all modes, including serial interface

Test boards setup

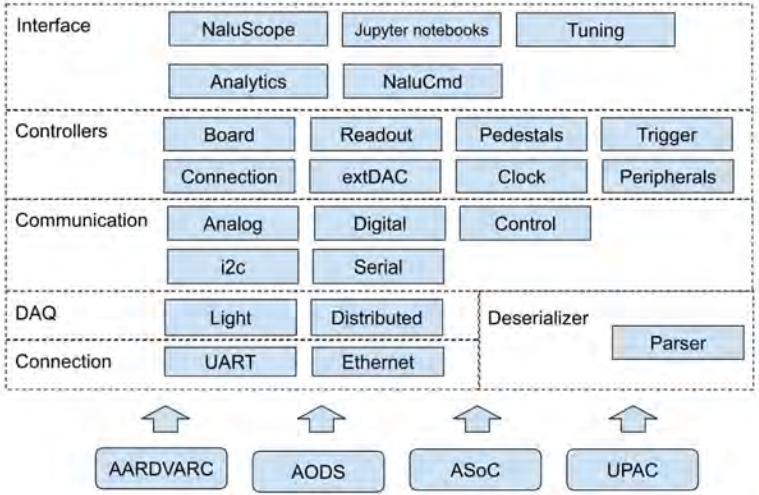


Evaluation Board - now available to interested customers through CAEN - connects to inexpensive readout board with Ethernet connectivity



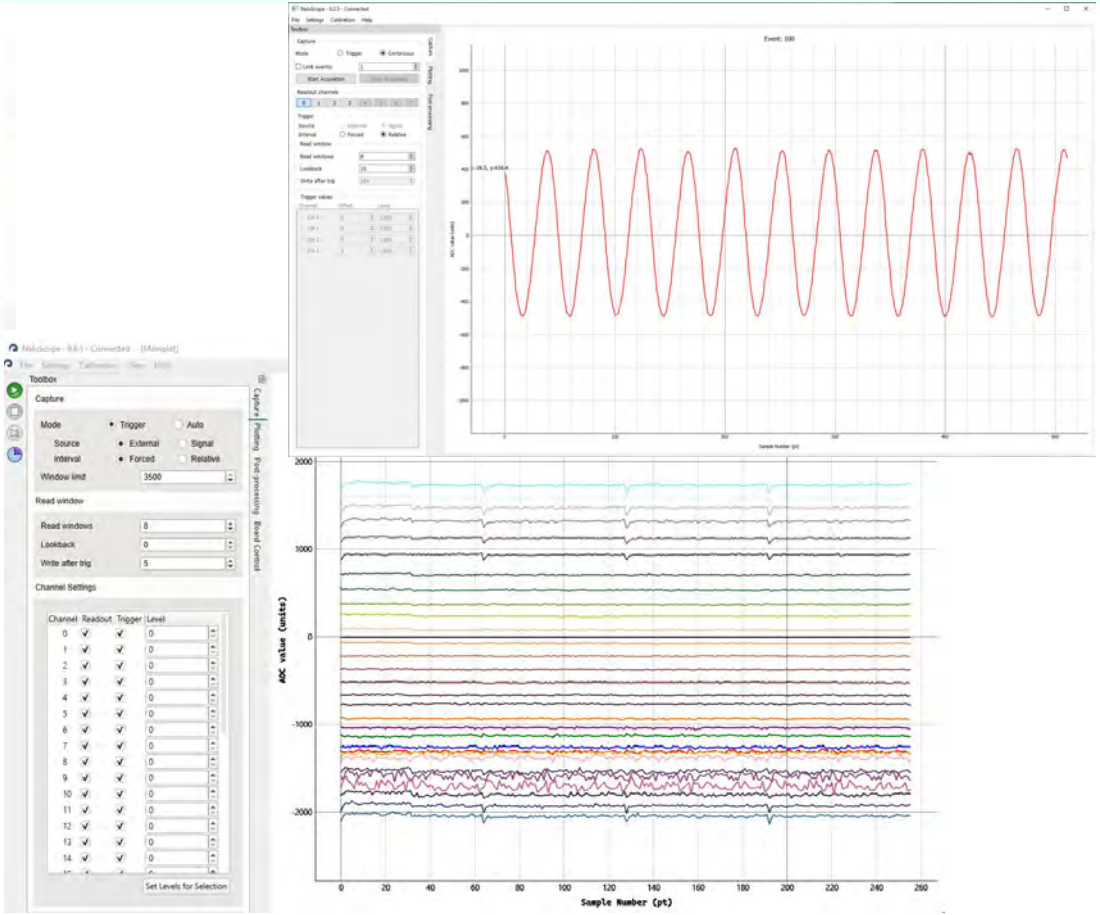
Test Rig at Nalu - full remote access to boards, including signal sources - a lifesaver during COVID days....

NaluScope Common Software and GUI



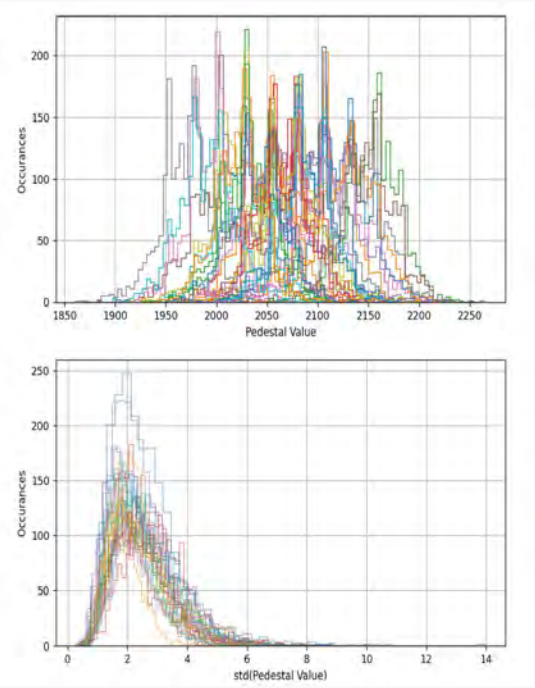
The Nalu software is built around reusable modules, allowing multiple use cases and UIs.

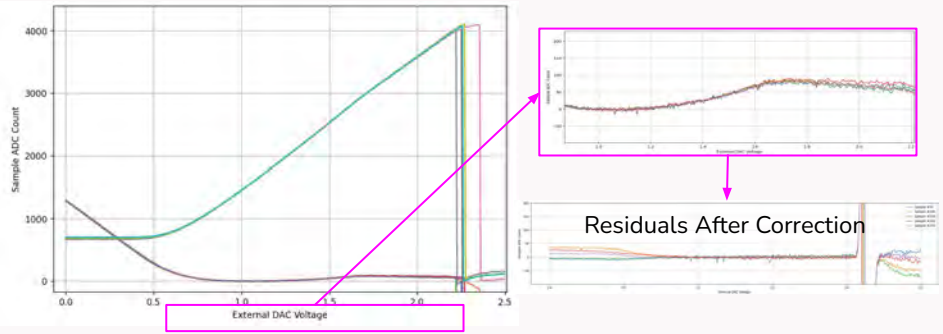
- Windows/Linux PC
- USB interface
- 1GB Ethernet
- GUI, CLI interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage



HDSoCv1 Static accuracy

- "Pedestal" evaluation:
  - Due to internal offsets the individual sample values need to be calibrated
  - Statistics on the individual readout for the calibration can be used to estimate the "static error" at bias level -> ~2 ADC count standard deviation
- Varying the input bias to the chip allows studying the overall non-linearity of the conversion - pattern can be calibrated in a large range (1.2V) with residual of ~5 ADC counts (3 ADC counts for a central range of ~200mV)

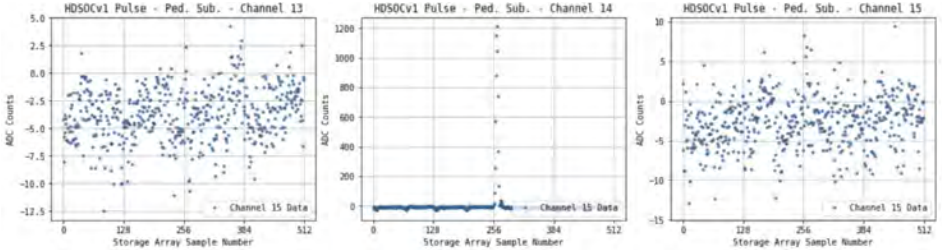




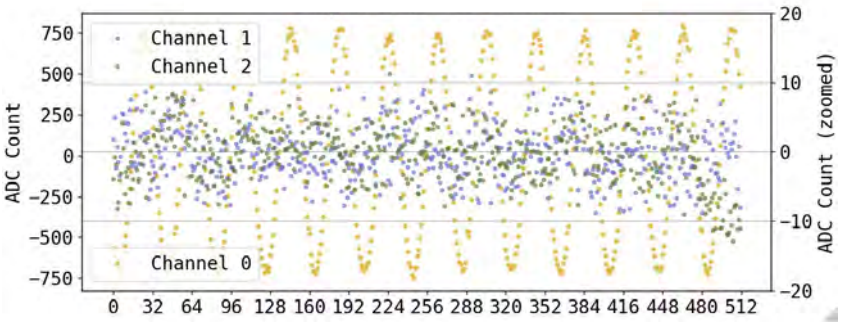
Crosstalk: Pulse and Sine Wave Inputs

No signs of significantly visible crosstalk on neighbor channels

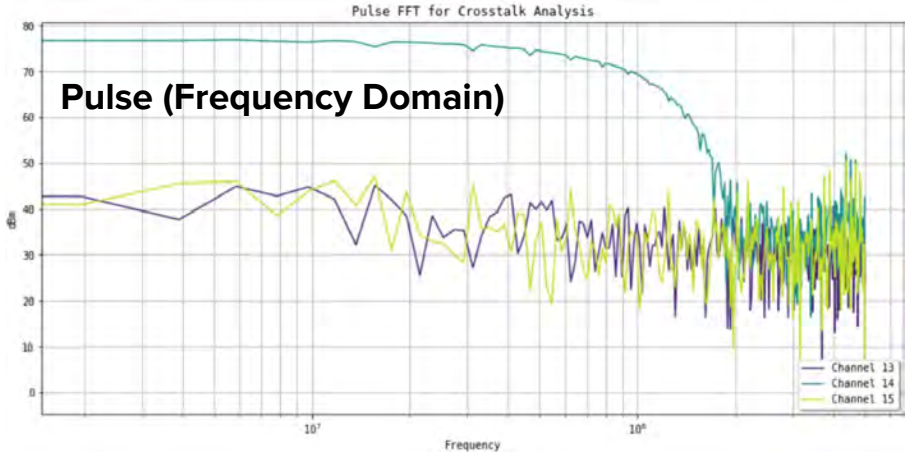
Pulse (Time Domain)



Sine Wave



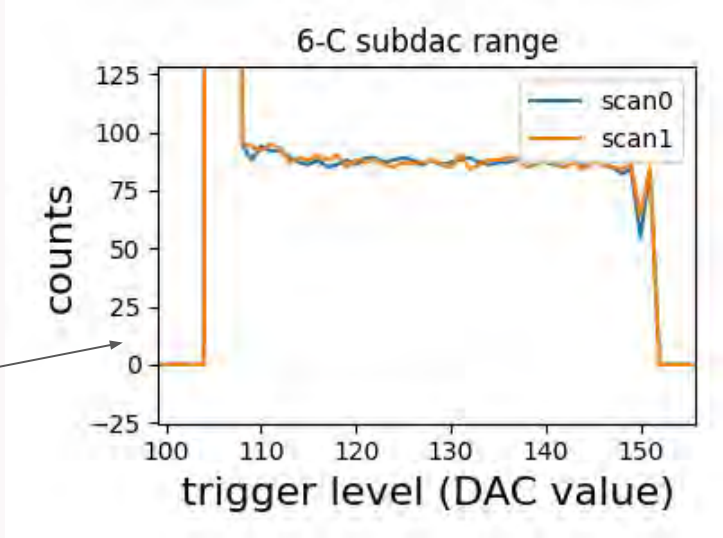
Pulse (Frequency Domain)



Note: signal and noise on difference scales

Digital Partition Features testing

- Different acquisition modes (ROI, self-triggering)
  - Self triggering
  - RoI (zero suppression based on internal thresholds)
- Verification of output trigger streaming
- Internal Scalers to perform threshold scans
- Serial interface (functionality and speed)
- Max event rate: 14kEvents/s for all channel readout, 220kEv/s for single channel

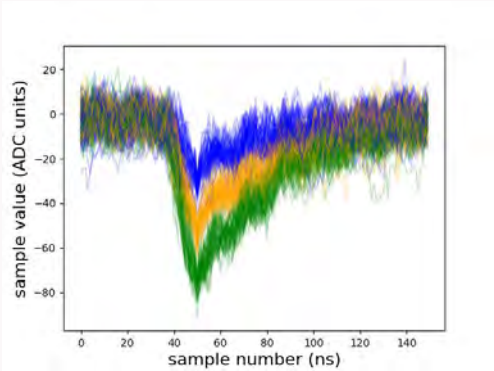


SiPM readout experiments

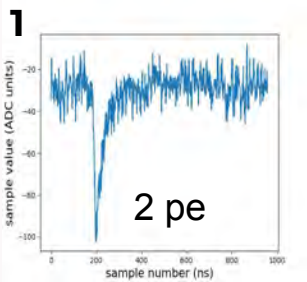
HDSoC V1 connected to a SiPM array. Onsemi J-Series 4x4 array of 3 x 3 mm2 SiPMs. HDSoC V1 channel 0 was set to trigger on signals corresponding to two PEs and above

1. SiPM pulses acquired via HDSoC self-triggering capability
2. SiPM pulse template (via averaging) calculated.

   A spline fit was used to smooth the averaged pulse.
3. Template fit to estimate the amplitude of the pulse peak.
4. Pulse peak histogram shows maxima for 2 PE, 3 PE depending on the trigger threshold - (2, 3 and 4 PEs resolved at 24.4 ± 4.7, 48.2 ± 4.9 and 72.3 ± 4.7 ADC units)



1



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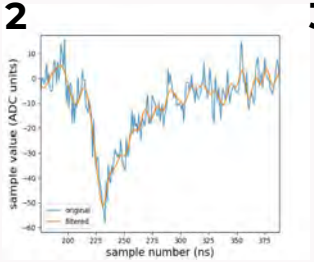

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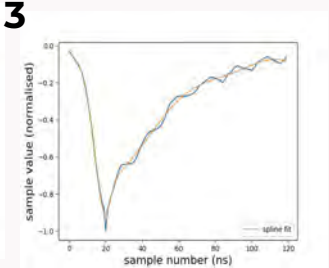

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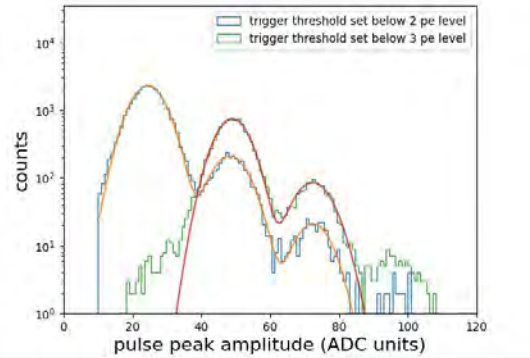


Timing Measurements and calibration

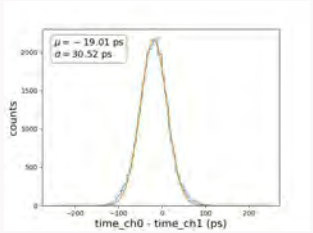
Estimating timing accuracy:

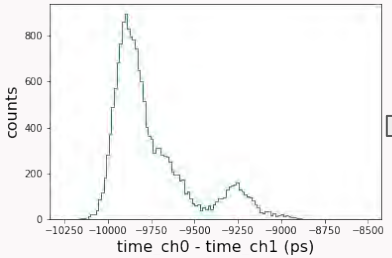
1. Identical Split pulse to two channels: ~30ps - (100 MHz 450 mV unipolar sine burst)

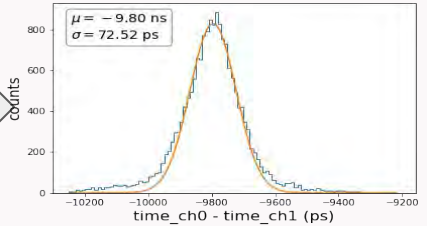
2. Intra-channel accuracy: signal delayed ~10ns: with timing calibration ~ 72ps

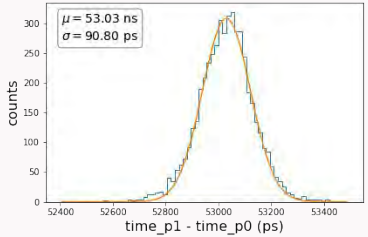
Note: Timing calibration performed using bin-occupancy fraction method on channels 0 and 1

3. Inter-channel accuracy with “far” signals and timing calibration ~90ps

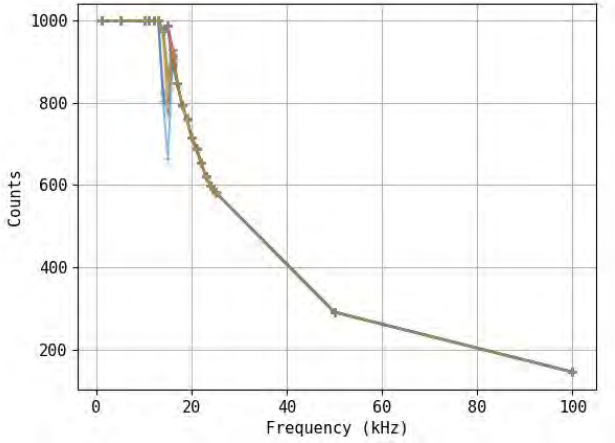




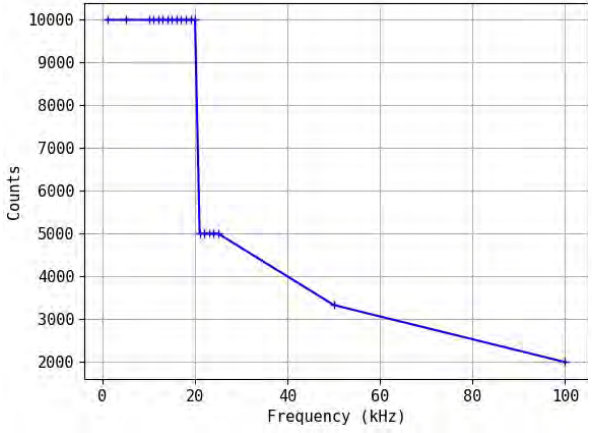




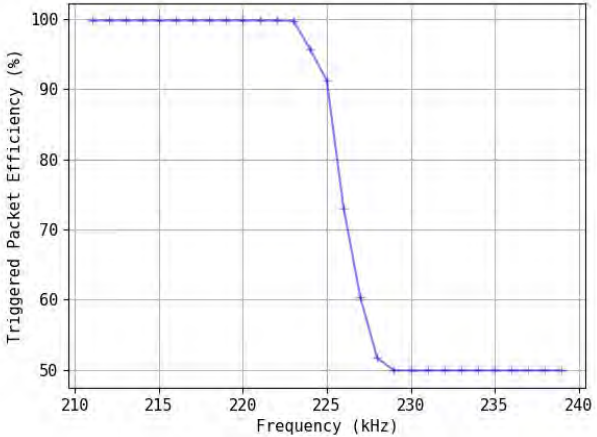
Rate estimation



- External trigger
- Maximum external trigger rate between 13kHz and 14kHz
- Graceful decrease from 17kHz trigger rate on



- Self-trigger on all channels identically triggered
- Maximum self-trigger rate between 20kHz and 21kHz

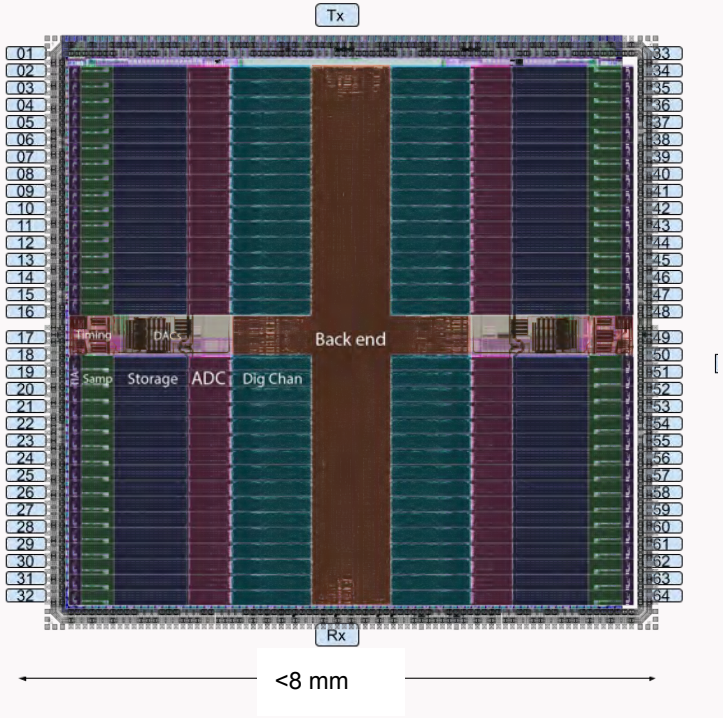


- Self-triggered - single channel
- Maximum self-trigger rate between 223kHz and 224kHz (consistent with expectations with current readout speed and clocking)
- Multi-channel self triggering falls between the 2 extremes, as expected (i.e. 3 channels at 157kHz, 4 channels at ~100kHz).

Part III:
High Density Digitizer SoC Revision 2 Design and Fabrication

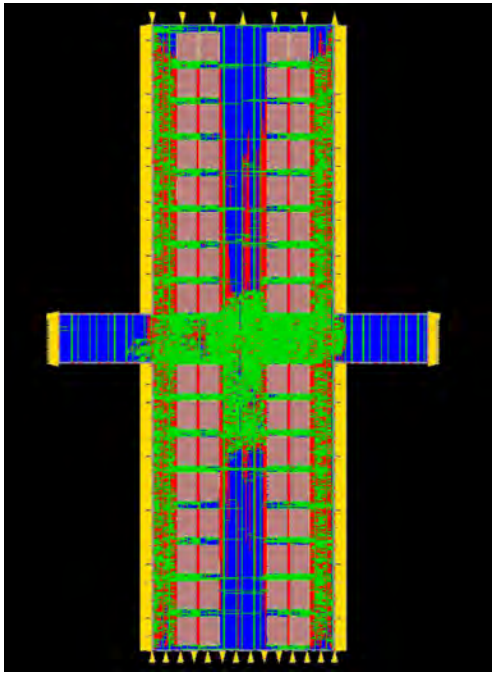
HDSoCv2 design

- HDSoC v2
  - Main improvements:
    - 64 channel device
    - Proper timing up to 2 GSPS
    - Reduced power consumption/chan
      - DAC uniformity
      - Clock gating
      - Triggering and Scalers reduction
    - Improved TIA
      - Correct low BW issue (input stage)
      - Complete redesign to target better integration with SiPMs, controllable internal and SiPM biasing
    - Improved signal quality:
      - Analog/digital isolation
      - Biasing control (current- based)
      - Comparator biasing
      - Power domain separation

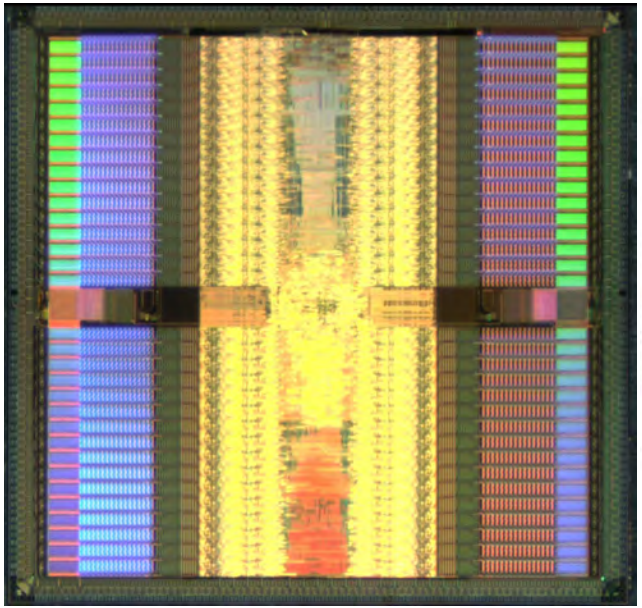


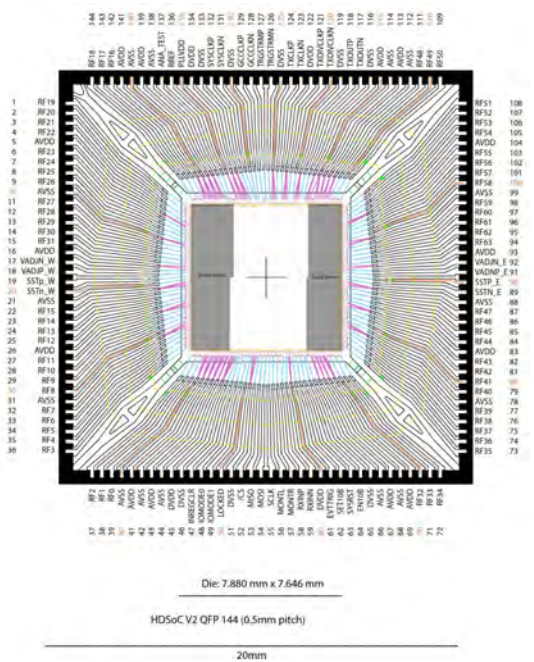
HDSoCv2 - digital Improvements

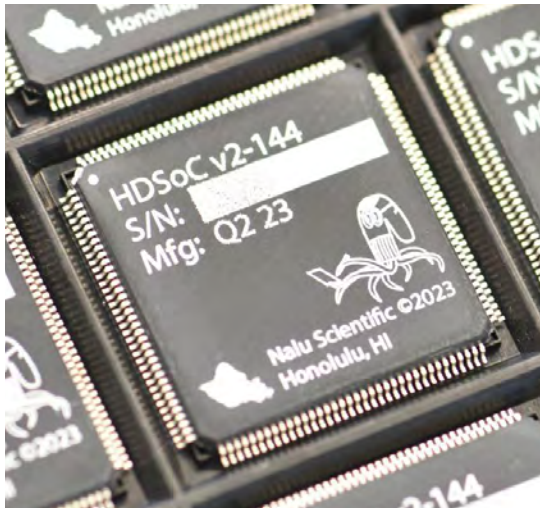
- PLL for internal generation of clocks:
  - Only one reference clock required for sampling, conversion, readout
- Simplified SPI-like interface for configuration:
  - Rev. 1 - fast LVDS proprietary interface (still available)
  - Rev. 2 - slower single-ended and simpler interface with chaining to reduce system constraints
- Design of internal calibrations SRAM and Feature extraction mechanism to reduce rates - not included in production due to scheduling constraints, but available for next revision.
- Some minor corrections:
  - Added Header information for ROI mode.
  - The internal scalers changes to avoid double counting
  - Added programmable masking for channel
  - External triggering changed from level trigger to edge trigger to simplify the system level requirements.
  - Command to trigger and request a single event



HDSoCv2 Layout - Fabricated die

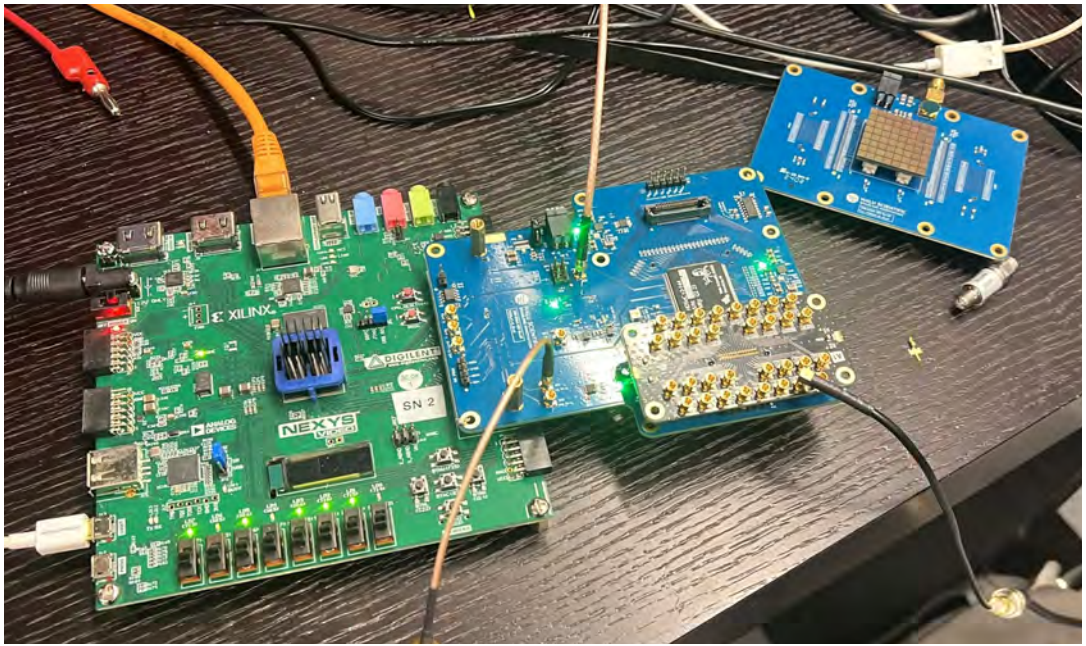






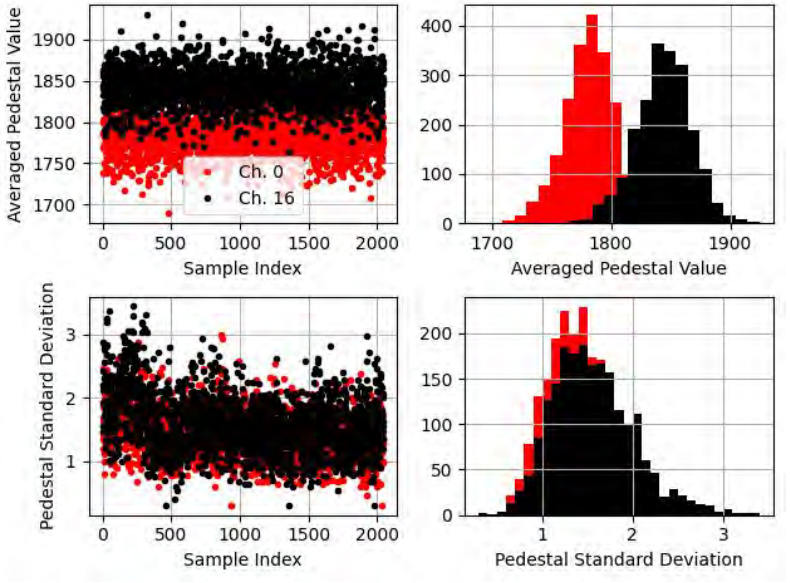
HDSoCv2 Testing

- Evaluation board designed
- Permits full evaluation of the functionality
- 2 separate types of daughter cards:
  - individual access to each of the channels via coaxial connectors,
  - house a commercial 64-pixel SiPM array.
- The board itself operates in conjunction with a commercial FPGA board.



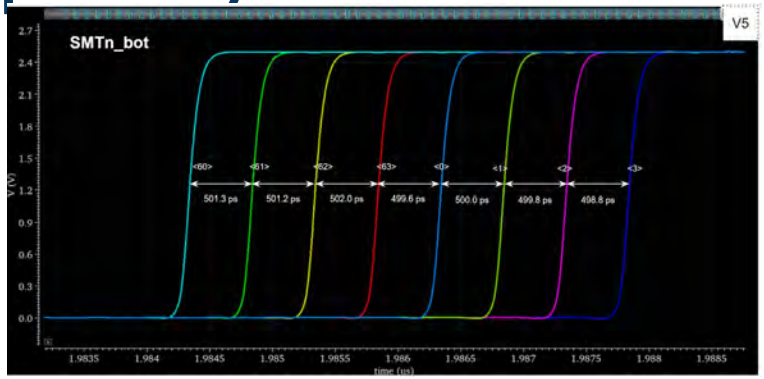
HDSoCv2 - data quality - calibration

- As in HDSoCv1 - need for offset calibration
- RMS on those was shown to be below 2 ADC counts, or ~1 mV error

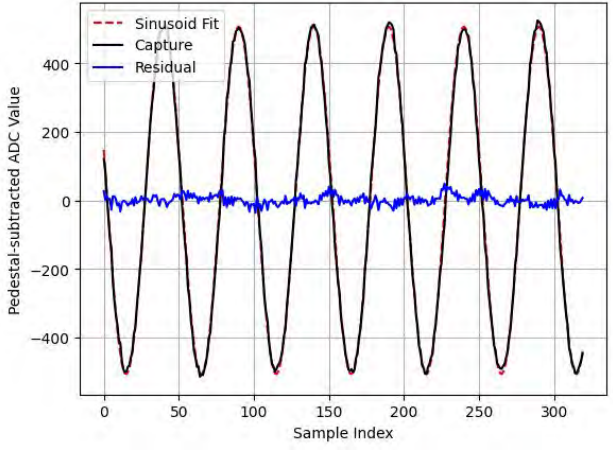


HDSoCv2 - data quality

- HDSoCv2 timing generator redesigned to guarantee more uniform sampling intervals and reduce as much as possible the “stitching” between 2 successive sampling periods.



- Measurements of sine waves demonstrated the improvement (no additional fitting error at the window boundaries

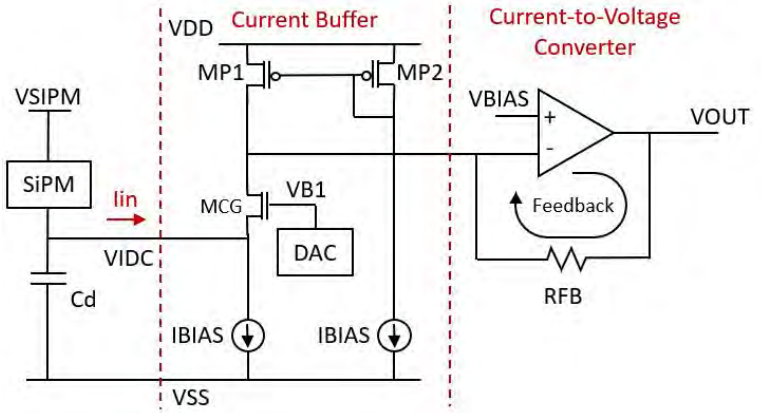


HDSoCv2 - other considerations

- **Power:**
  - Critical issue for very large channel count
  - Few power saving mechanisms were implemented
  - First measurements show an improvement of ~20% compared to the HDSoCv1 (37mW/channel)
  - Some further tuning might be possible.
- **Serial interfaces for control and configuration**:
  - "Old" serial communication interface from HDSoCv1 that was used in the first revision
    - Dedicated differential (2 pins)
    - Fast configuration
    - Point-to point (requires individual links to control electronics)
  - New SPI-like interface:
    - 4 pins, daisy chaining of devices
    - slower rates
    - can be shared between different chips and using simpler programming devices (i.e. microcontrollers instead of FPGAs).
  - Configuration can be performed both with the "legacy" serial interface and the SPI interface

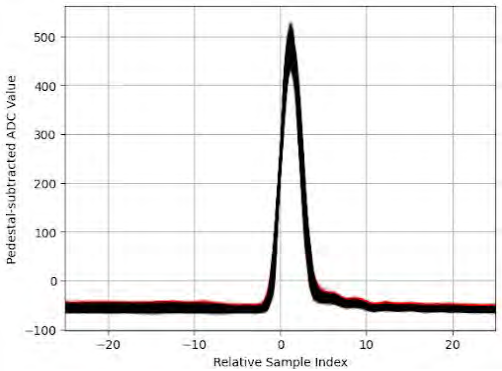
HDSoCv2 - New TIA

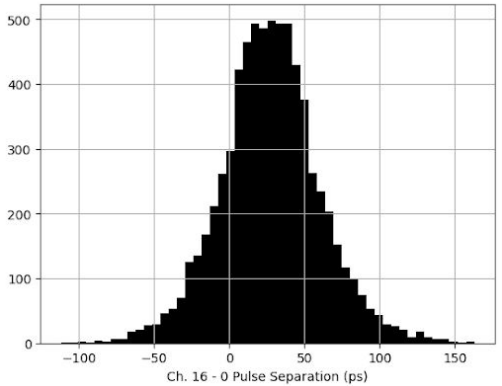
- New architecture for the TIA:
  - cascade current buffer and current-to-voltage converter
- Initial readout with input calibration:
  - some feedthrough effects from the clock network
  - First order correction via pedestal subtraction
  - Demonstrated full readout from a SiPM array
  - Calibration and TIA gain and bandwidth in development



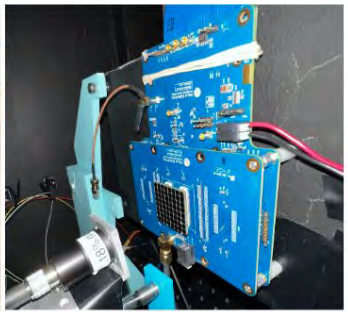
HDSoCv2 - Timing

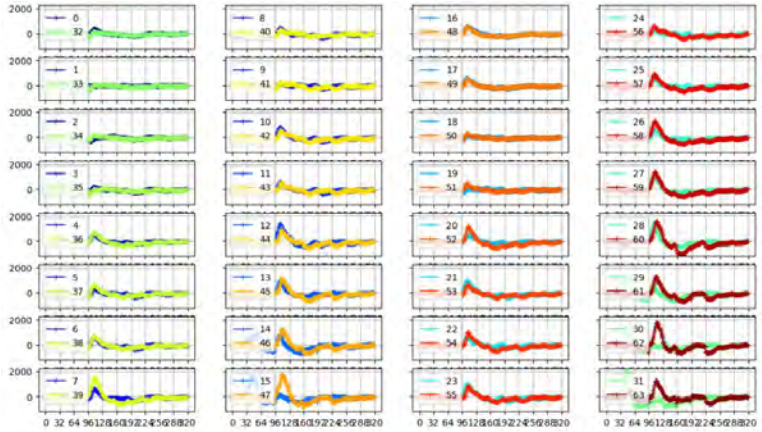
- Experiment to assess channel to channel timing:
  - split pulse into 2 separate channels (channel 0 and 16)
  - pulse asynchronous to chip clock (any position of the sampling and storage array)
  - arrival time estimated by thresholding and interpolating between the closest samples
- Results:
  - Histogram of the measured pulse separation shows minor skew and small standard deviation of 33.4ps.
- Similar experiments performed to assess intra-channel timing accuracy,
  - Require the development of timing correction.
  - Uncorrected data shows results comparable to the HDSoCv1



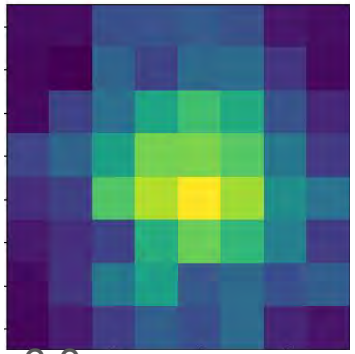


HDSoCv2 - SiPM readout example

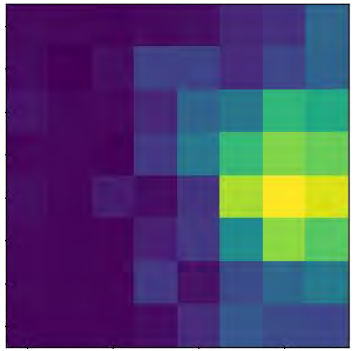




Laser at x=0mm



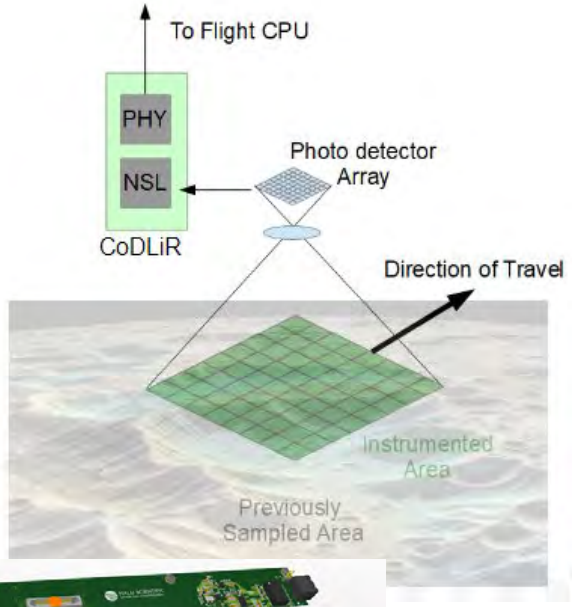
Laser at x=6.0 mm



Partially funded by
NASA

HDSoC - Applications

- CoDLIR: (Compact Digitizing Lidar Receiver)
    - Nasa project (SBIR phase II just started)
    - Permits reduction in space and power requirements for each channel of a LiDAR system would allow for a system with significantly more channels or allow for a system small enough to fly on CubeSat-scale vehicles.
- ADAPT: currently considered for a balloon experiment.
- Might be of interest for various other experiments (e.g. PIONEER)
- Currently in use in national labs and universities for benchtop testing and technology evaluation.
- Eval board available through our distributor (CAEN)
- EIC possibilities



Presentations at 2023 IEEE NSS-MIC

NALU SCIENTIFIC
ENABLING INNOVATION

N-27-03 – Design and initial Measurement Results for the second revision of the High Density Digitizer System on Chip (HDSoCv2): A 64 Channel 1 GSa/s Waveform Digitizer for High Density Detectors (#2284)

N-27-04 – Design and First Measurement Results for the Revision 4 of AARDVARC Waveform Sampling System On Chip (#2302)

N-19-05 – Installation and Time Resolved Measurements of Accelerated Electron Beam Halo Using Diamond Detector at FACET (#2395)

N-32-04 – The ScIDEP Project at the Egyptian Pyramid of Khafre (#2104)

TS-03-01 – Waveform Digitizing Front-end Electronics For High Density Detector Re

N-01-171 – Testing of the GRAPH ASIC for Processing Photon Event Positions on Cross Strip Anodes (#2365)

N-01-075 – Timing optimization and timing resolution for the AARDVARC chips (#2424)

N-11-110 – Measurements on HDSoCv1 performance and rate handling for acquiring fast silicon photomultiplier signals (#2396)

Conclusions and future work

- **HDSoC v1 (32 channel)**
  - Proper multi-window, multi-channel acquisition, self triggering, output streaming
  - Some issues with noise and power/ TIA BW
  - Test boards available through our U.S. distributor, CAEN - together with FW/SW/GUI and support.
- **HDSoC v2 (64 channel with input TIA)**
  - Fabricated and tested - some features of conversion and front end still being investigated
  - Used in another NASA project (CODLIR)
  - Possibly adopted in other NP experiments
  - HDSoC v1/2 may be used in beam tests for various EIC sub detectors
  - Opportunity to implement EIC specific (sensor, backend) needs in future revisions or branches
  - Test boards available through our U.S. distributor, CAEN - together with FW/SW/GUI and support.
- **HDSoC is a novel streaming readout capable, waveform- sampling ASIC**:
  - Low Cost, low power, scalable
  - Works with a variety of sensors arrays: GEMS, TPCs, SiPMs, MA/PMTs, MCP PMTs
  - Tracking and PID
  - Portable radiation imaging systems
  - Compact, high-efficiency neutron scatter cameras for non-proliferation national security missions.
- Various conference presentations and live demos

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