DE-SC0020500

Digital Data Acquisition with High Resolution and Linearity

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Principal Investigator

SBIR Exchange, August 15, 2024 11:30am

SkuTek Instrumentation
SkuTek.com

Outline

- The company and its capabilities.
  - Customers.
- The ADC Nonlinearity problem.
- Nonlinearity example from Majorana Demonstrator.
- Demonstration of the Differential Nonlinearity (DNL) with our test digitizer.
- The nonlinearity correction.
- The remaining steps.
- Future plans.
- Acknowledgements.

The company and its capabilities

- The team: three physicists / engineers, a senior software engineer, a junior research engineer, engineering associate, a part time physicist, and a manager. We regularly work with a local Electrical Engineering consultant.
- We worked with several interns listed on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, astrophysics, etc.

Our capabilities: Development of electronic instruments for Nuclear Physics.

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, either hard silicon or soft cores.
- Algorithm implementation in FPGAs and in embedded processors.
- Processing data from nuclear detectors of any kind.
- Development of detector assemblies using scintillators, PMTs, PIN diodes, or SiPMs.

SkuTek Instrumentation

Our customers

University of Rochester

Houghton College

The University of Tennessee Knoxville

SFU Simon Fraser University Engaging the World

Université Laval

Augustana University

上海交通大學 Shanghai Jiao Tong University

Los Alamos National Laboratory

Fermilab

Brookhaven National Laboratory

NSCL National Superconducting Cyclotron Laboratory

Albert Einstein Center for Fundamental Physics

Universität Bern

Brown University

Wiener Plein & Baus, Corp.

Northrop Grumman

Nonlinear Response of the Pipelined ADC

The Problem:

- Pipelined ADC architecture causes semi-periodic nonlinearities of the response, due to imperfect matching of the ADC stages.
- Nonlinearity is impacting resolution in high precision measurements
- Example was described in the Majorana Demonstrator paper.

N. Abgrall, et al, *ADC Nonlinearity Correction for the MAJORANA DEMONSTRATOR*

https://arxiv.org/pdf/2003.04128.pdf

Nonlinearities in Majorana Demonstrator Analysis

Both graphs should be flat for an ideal ADC

Nonlinearities of the GRETINA digitizer (AD6645) were reported by Majorana Demonstrator.

N. Abgrall, et al, ADC Nonlinearity Correction for the MAJORANA DEMONSTRATOR

https://arxiv.org/pdf/2003.04128.pdf

Ideal responses should be flat!

Figure 3
DNL measured with slow analog ramp.

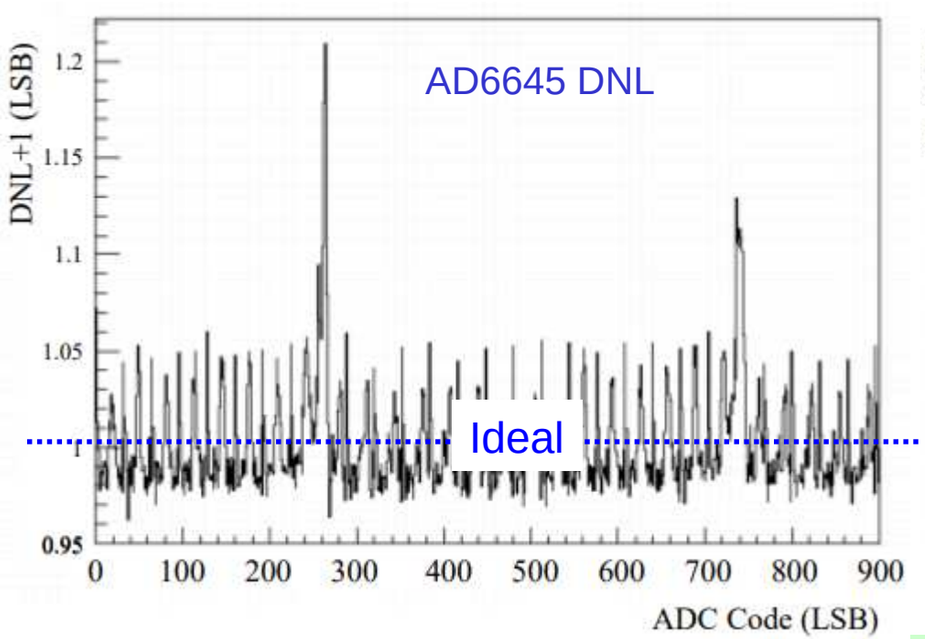
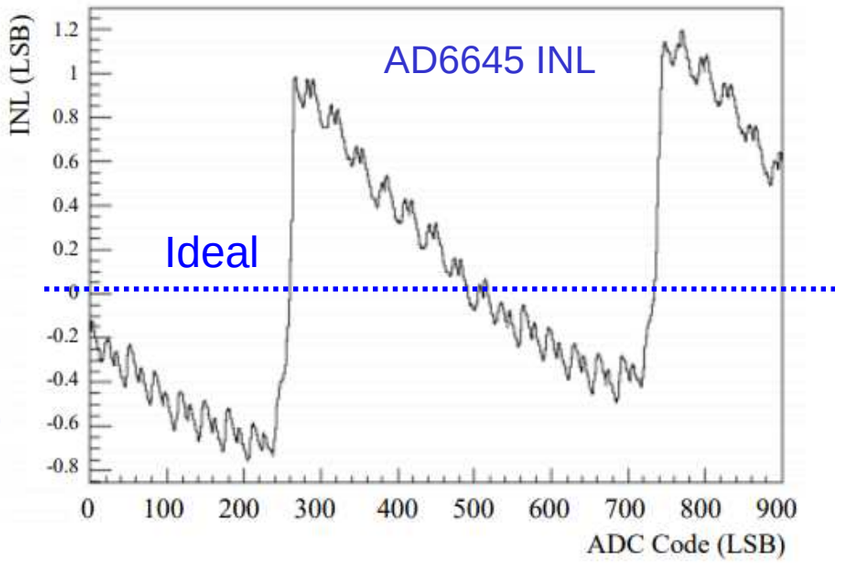
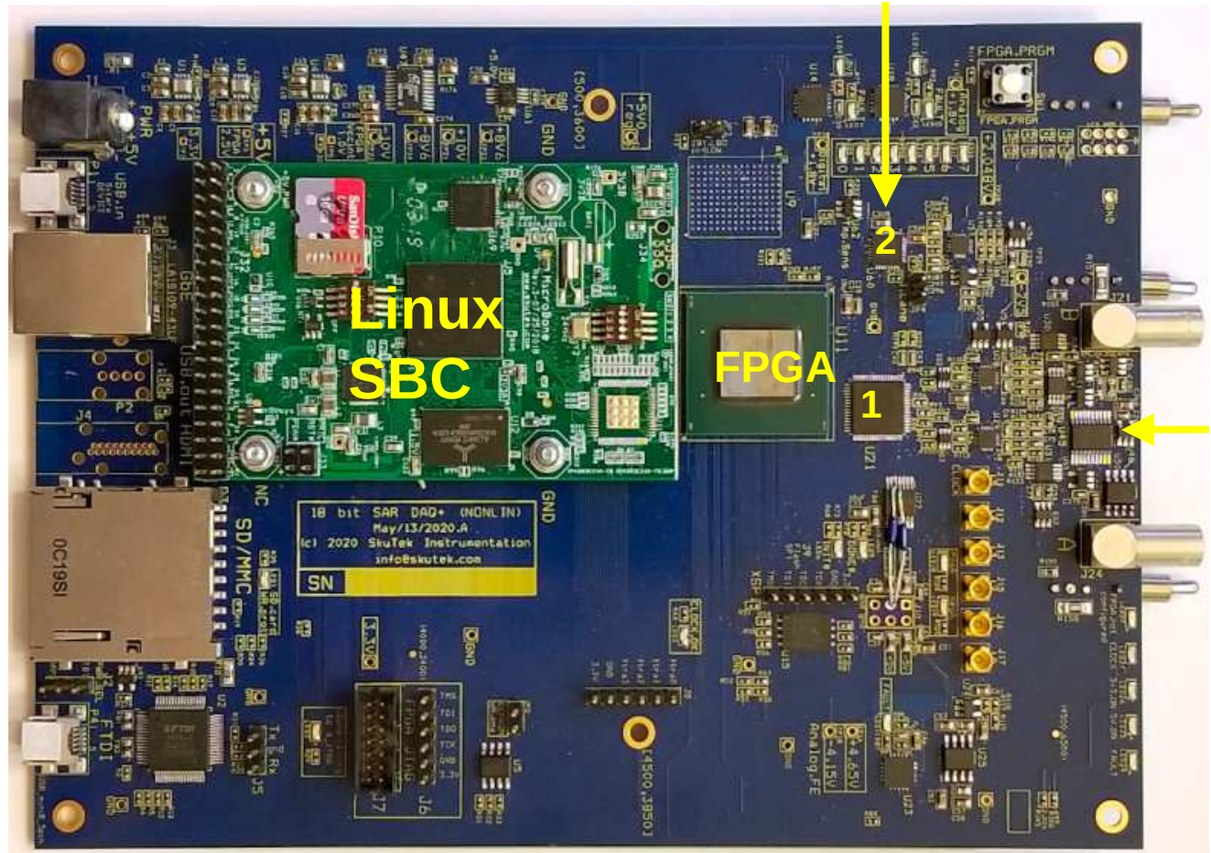


Figure 4
INL: integrate the measured DNL, subtract away overall slope.



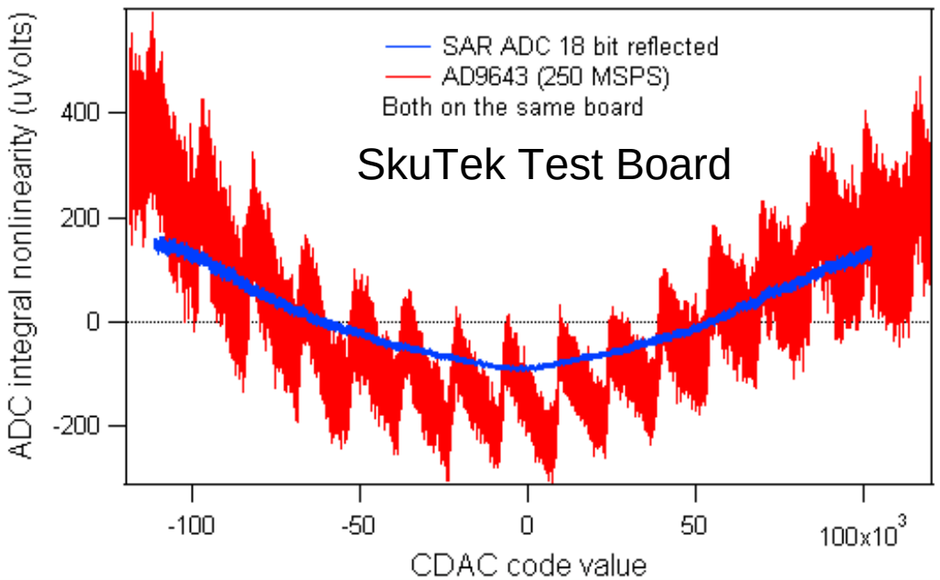
We Built a Test Digitizer With 18-bit ADC & DAC forming on-board nolinearity measurement circuit



In Situ Nonlinearity Measurement

Performed with our 18-bit Test Digitizer

- For every 18-bit DAC voltage we recorded two ADC waveforms with 32k samples.
  - A waveform from the fast pipelined 14-bit ADC.
  - A waveform from the slow SAR 18-bit ADC.
- We calculated the averages of both waveforms and plotted against the DAC code.
- The reference SAR ADC was free of local nonlinearities (no sawtooth pattern).
- The fast pipelined ADC showed the sawtooth, as expected.
- The overall horseshoe pattern was caused by the operational amplifier at input.

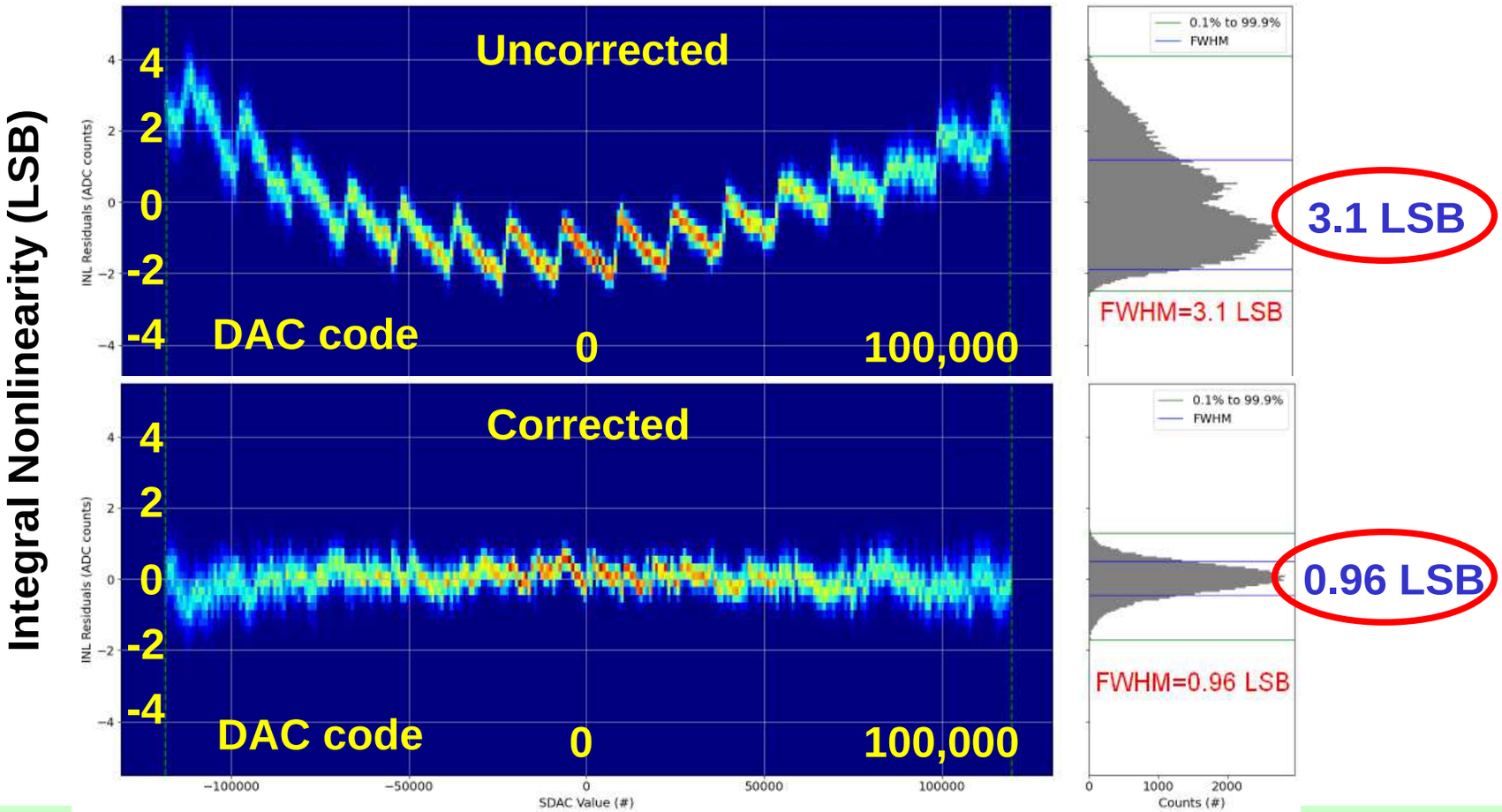


Blue: slow 18-bit ADC

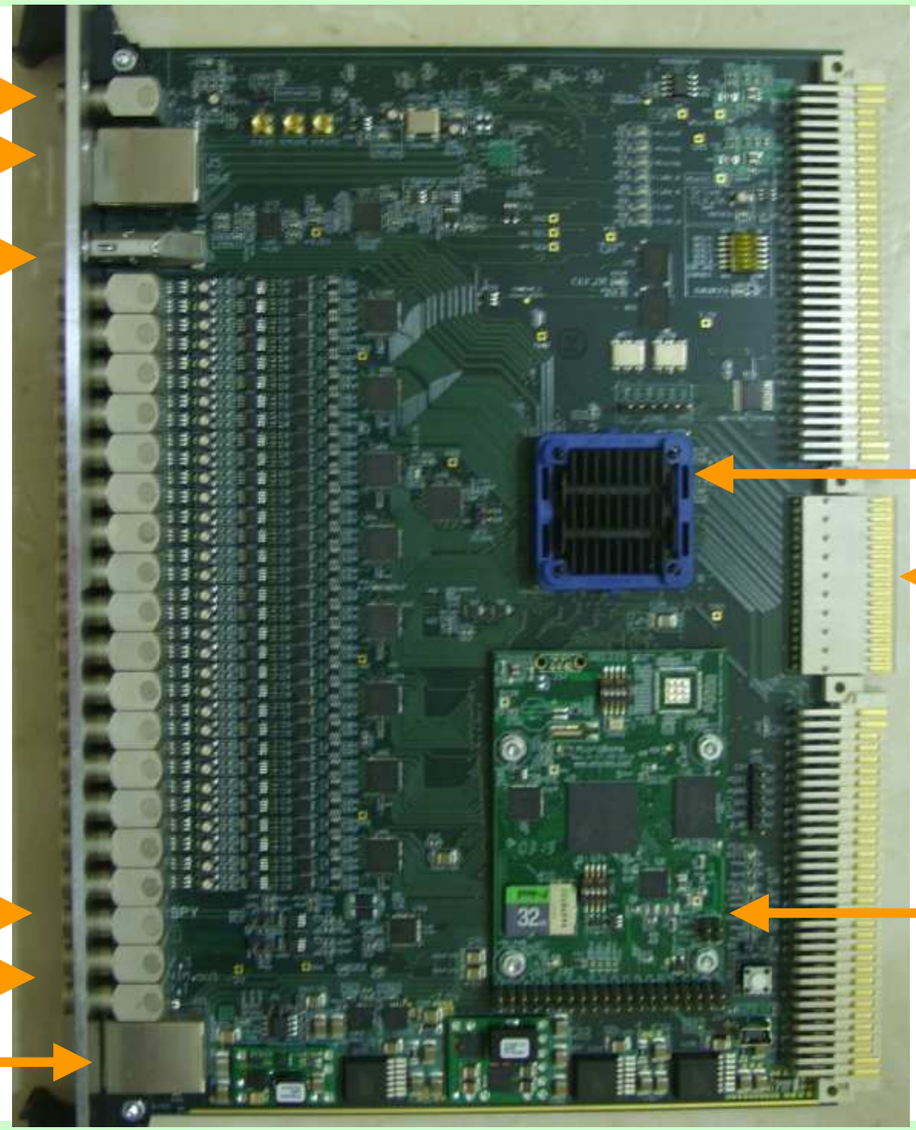
Red: pipelined 14-bit ADC

Our Nonlinearity Measurement and Correction

- We measured the INL, using the on-board 18-bit DAC to drive the known voltage to the input.
- The stimulus voltage was verified using the 18-bit ADC in parallel with the 14-bit main ADC.
- After applying the correction, the 14-bit ADC response is at the limit of the ADC Data Sheet.



32-Channel Digitizer for High Resolution Detectors



NIM in 0,1

1G Ethernet

Fast LVDS Link

Channels 0..31

High quality coax inputs

Analog out 0,1

NIM out 0..3

Linux Ethernet

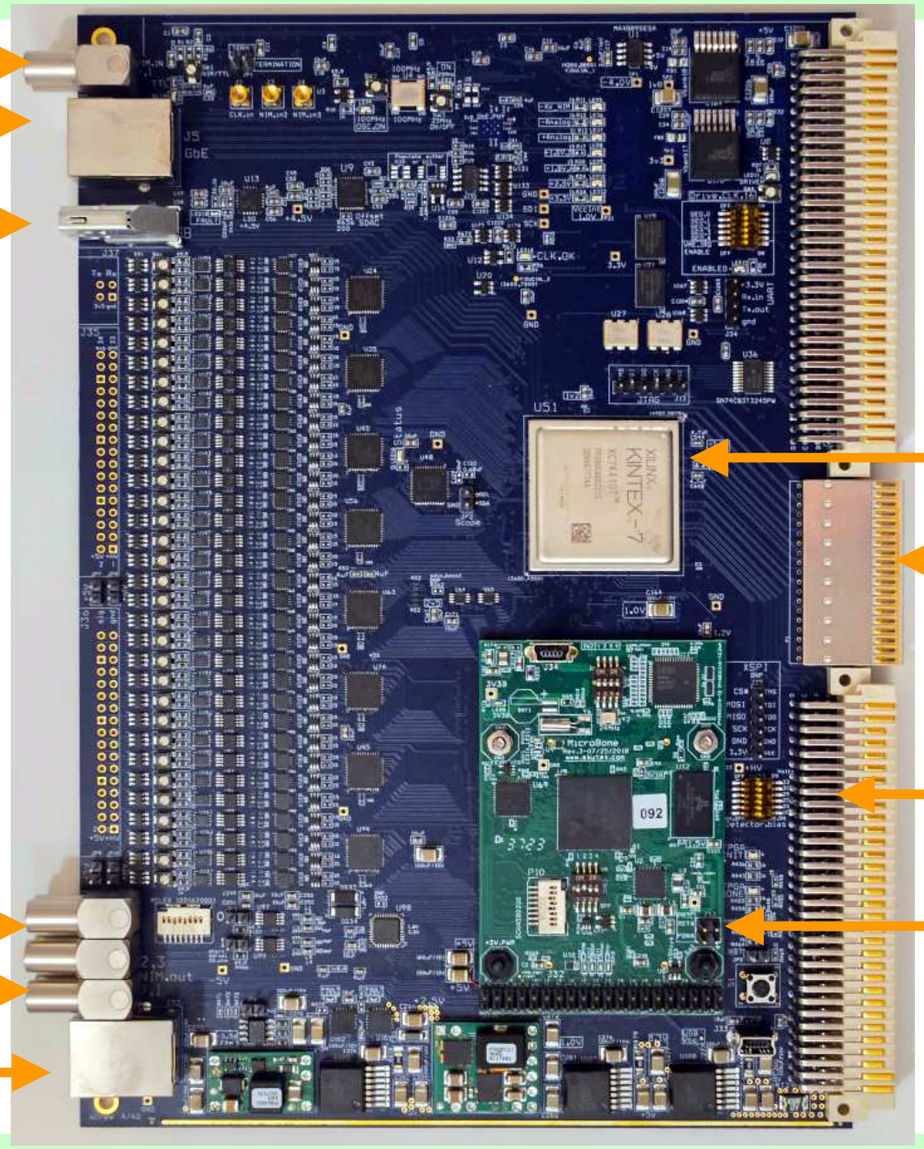
- On - board calibration with 16-bit voltage DAC

FPGA

Hard Metric P0

Linux SBC

32-Channel Digitizer for Low Resolution Detectors



NIM in 0,1

1G Ethernet

Fast LVDS Link

Channels 0..15

Bias voltage and +5V for channels 0..15

Channels 16..31

Bias voltage and +5V for channels 16..31

Analog out 0,1

NIM out 0..3

Linux Ethernet

- On - board calibration with 16-bit voltage DAC

FPGA

Hard Metric P0

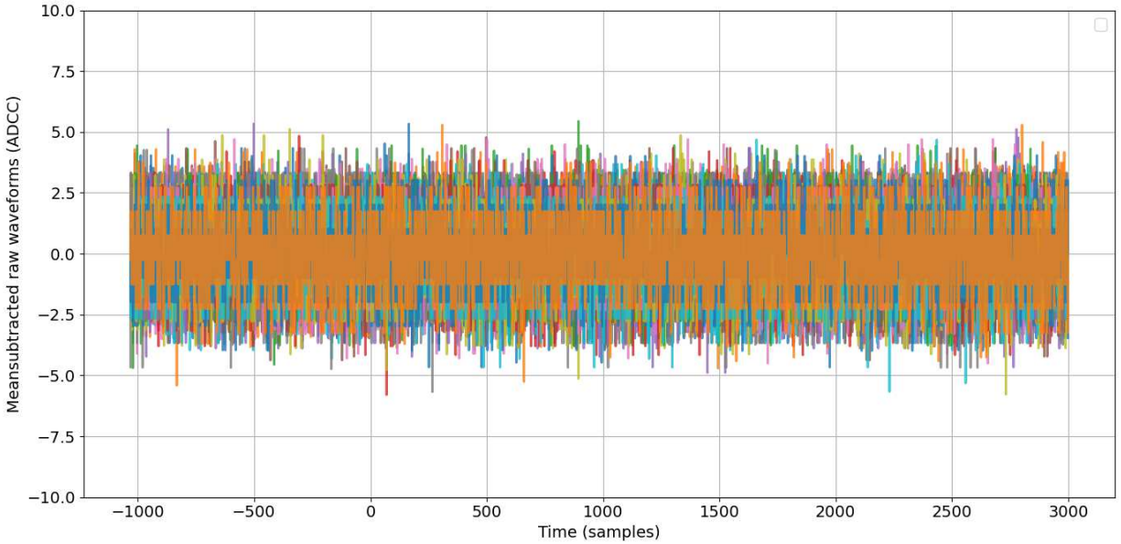
Bias voltage selection in 6 steps 10..32 volts

Linux SBC

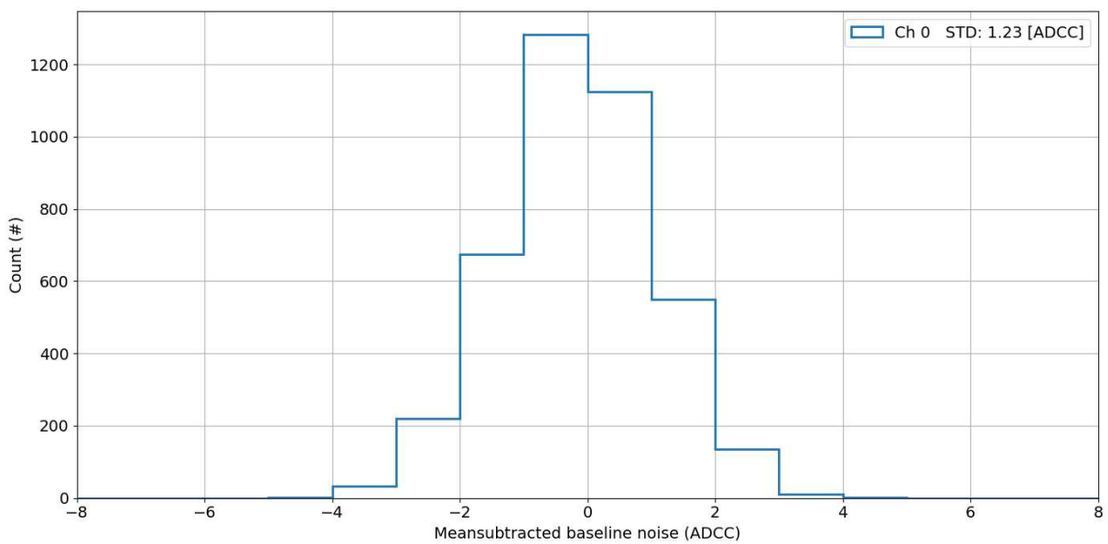
Analog to Digital: Very Low Noise

- Signal range = 2 volts, digitized with 14 bits @ 100 MSPS.
- 1 LSB = 2 V / 16k = 122 µV

Noise waveforms from all 32 channels



Noise RMS = 1.23 LSB = 150 µV



Digital to Analog: Very High Convenience

- Signal range = 2 volts, synthesized with 14 bits @ 100 MSPS. (“Inverse digitization”.)
- Any signal can be synthesized and examined with a scope: any input, any internal trigger, multiplicity, energy sum, etc.
- Logic Modules can synthesize any input from any slave digitizer, while the input stays connected.

Two analog reconstruction channels, 14 bits @ 100 MSPS

- In this figure, two SPY channels are outputting two internally generated sawtooth signals.
- SPY outputs were connected to a Tek scope.

Digitizer Ecosystem: Data Streaming and Management

Recording data

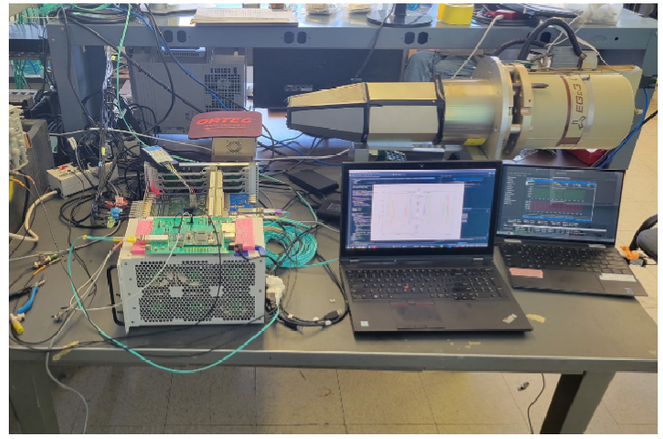
Each 32-Channel Digitizer can stream data at 10G

1 Digitizer = 10 G = 1.2 GB/s ~ **140K waveforms per second**

4 Digitizers = 40 G = 5 GB/s ~ **700K waveforms per second**

10 Digitizers = 100 G = 12 GB/s ~ **1.4M waveforms per second**

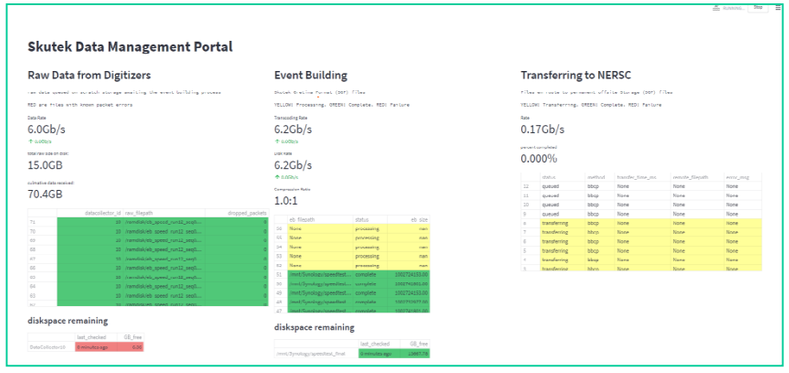
**Assuming 4096 Samples per waveform*



10G Data Collection Demonstration at ANL

Our Data Management Solutions will receive the streams and transfer your data to NERSC or another supercomputing center

Data Collector servers receive event streams and convert them to files



A Web-based Interface will let you monitor your data as it's collected, processed, and transferred to NERSC

Overview of the SkuTek DAQ

- High resolution appropriate for any detector, including HPGe.
- High linearity after applying INL / DNL corrections
- High throughput pipelined DSP firmware.
- Real time integration windows: energy, charge, pulse height, particle identification.
- Real time trigger and time stamp per channel.
- Time & Trigger Control Link (DGS / GRETINA TTCL): trigger, time stamp, sampling clock.
- White Rabbit clock input (under development).
- Board control and monitoring with Embedded Linux.
- Interface with EPICS, embedded web page, Jupyter, or SSH + Command Line.
- Event streaming, either 1 G or 10 G, in parallel from each digitizer.
- End-to-end data streaming and management, from the digitizers to NERSC.
    - Up to 100 G with hardware acceleration with commercial FPGA boards.

Remaining Tasks

- We have developed the solution of the nonlinearity problem.
- We built prototypes and demonstrated the nonlinearity measurement and correction.
- But we are not done yet.

- **The prototypes need to be turned into products desired by the NP community**.
  - Multi - digitizer DAQ system with multiple digitizers working together.
  - User - friendly setup, control, and monitoring.
  - Firmware and software customized to applications (we cannot avoid *some* customizations).
  - Add features requested by the community (e.g., integration with other DAQ systems).
  - Integrate with our own ecosystem: data collection, data storage, and data management.

- **It is difficult to commercialize products which are poorly known and perceived as risky.**
- We need to make the NP community aware of our products and solutions.
- We need to demonstrate how our products will benefit Nuclear Physics.

We plan to gain visibility through supporting research projects

A real-time DAQ trigger on the neutrino signal from galactic core-collapse supernovae (SN)

M. Elise McCarthy, Dept. of Physics and Astronomy, University of Rochester

Goal: Record the time sequence of LZ trigger pulses with zero dead-time to characterize the background events.

Requirement: Recording of the trigger time sequence must not require any modification or major interruption of the main LZ DAQ.

Approach: The digitizer will store sequences of trigger pulses in two PSRAM memory buffers (16 MB each). The recorded background trigger time sequences will allow for developing and evaluating different SN trigger approaches, that will be implemented and run on the LZ DAQ FPGA(s).

Tool: We **donated** the Vireo digitizer to this project.
The digitizer will be operated in parallel to the LZ DAQ.

We need to attend meetings and conferences

Low Energy Community Meeting, August 7-9, 2024

We need to show our products

Generate visibility and attention

Offer something tangible, valuable, and affordable

Our entry level 2-channel digitizer:

An introduction to Digital Data Acquisition

The LECM 2024 Free Digitizer Contest

- During LECM 2024 (last week) we organized a Free Digitizer Contest with a 2-channel Vireo awarded to the best R&D project involving students.
- The winner of the Free Digitizer Contest was announced on our behalf on Friday, August 9 2024 by Andrew Ratkiewicz, a Chair of FRIB Users Organization Executive Committee:
- We received two entries to our contest. Thomas Baumann of Mona Collaboration proposed to use our digitizer for development of a new neutron detector with SiPM arrays. Mustafa Rajabali of Tennessee Tech University proposed to study the natural rate of cosmogenic activation of materials on the Earth surface, using scintillation bars with photomultiplier readout.
- Since both entries involve undergraduate students and we see great educational value in both projects, we decided to award digitizers to *both* of them! We are hoping that both projects will be successful, will help educate students, and will have positive impact on the Low Energy Nuclear Physics community.

Future Plans

- Implement user - friendly control interface for the nonlinearity correction and DAQ.
- Add features requested by the community.
  - E.g., support for the White Rabbit clock was requested by FRIB. We are implementing it.
- Work out integration of multiple digitizers into a coherent DAQ.
- Unify GUI and user experience of the 2-channel, 10-channel, and larger units.
- Gain visibility and brand recognition in Nuclear Physics, HEP, and other branches of physics.
  - Support valuable research and educational projects with our devices.
  - Optimize the 2-channel digitizer hardware, firmware, and software for best user experience.
  - Decrease the cost of the entry-level units so they can be “profitably given away”.
  - Leverage the goodwill of the recipients.
- Keep adding expertise to the team.
- Keep working with interns.

Acknowledgements

Joanna Klima, Jackson Hebel, Jeffrey Maggio, Hugh Gallo, Edmond Tan, David Miller, James Vitkus, WS

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Special thanks to Manouchehr Farkhondeh, Michelle Shinn, and Brenda May

Component Boards of SkuTek Large Scale DAQ

Digitizer with 32 channels

Logic & Trigger Module Serving 320 Channels