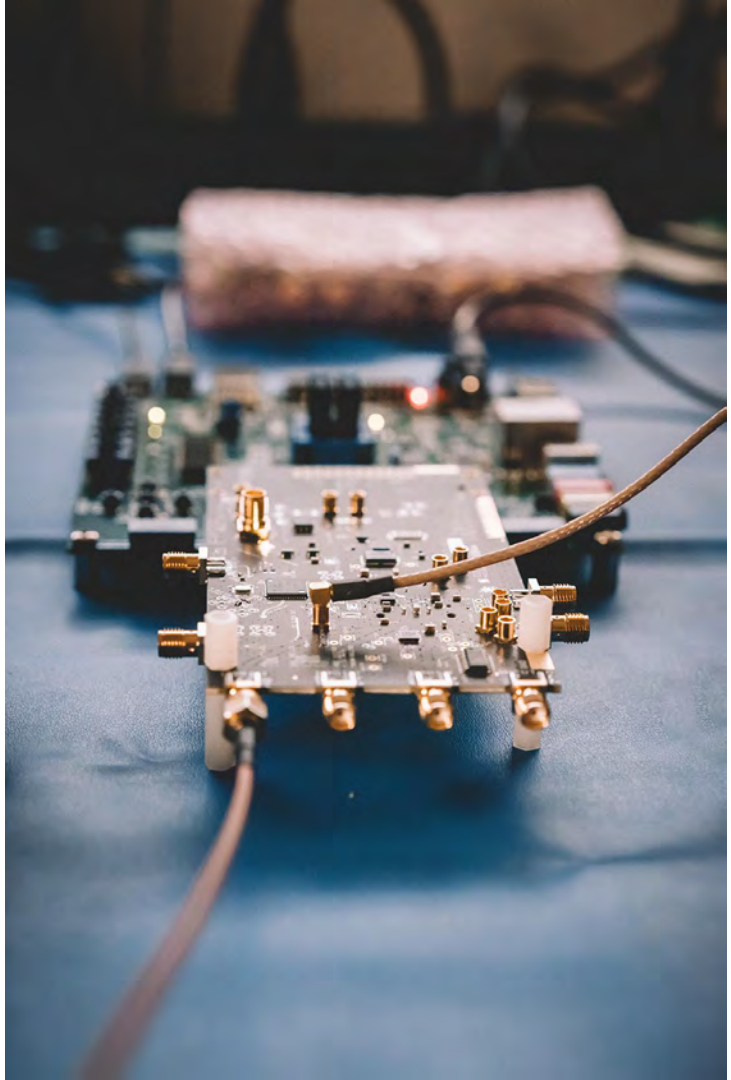


NALU SCIENTIFIC
ENABLING INNOVATION

Design and development of the All-in-One Digitizer System-on-chip "AODS"

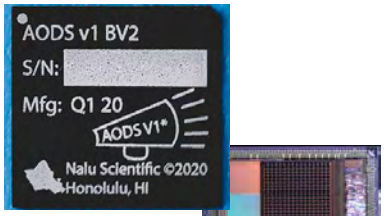
A low-cost, low power, low-noise and low channel-count Application Specific Integrated Circuit (ASIC) with a high dynamic range option.

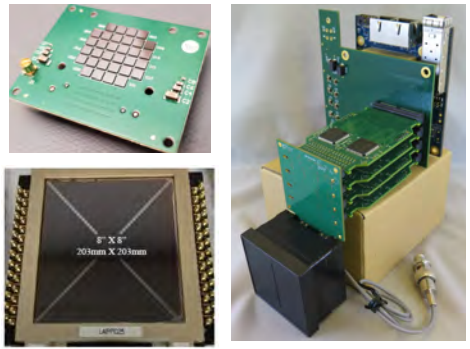
Aug 14, 2024
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

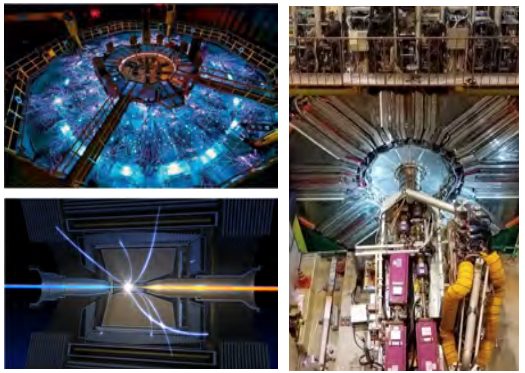
Work funded by DE-SC0019527

NCE: 8/31/24

Core Technology:
Data Acquisition Microchips







1. Front-end Chips:

- Event based digitizer+DSP
- 4-64 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

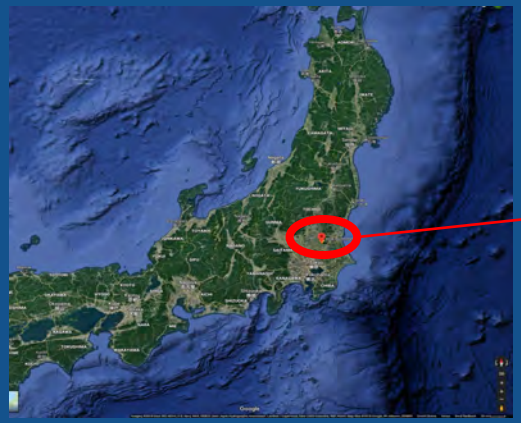
- SiPM
- PMT
- LAPPD
- Detector arrays

3. Applications:

- NP/HEP experiments
- Astro particle physics
- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging

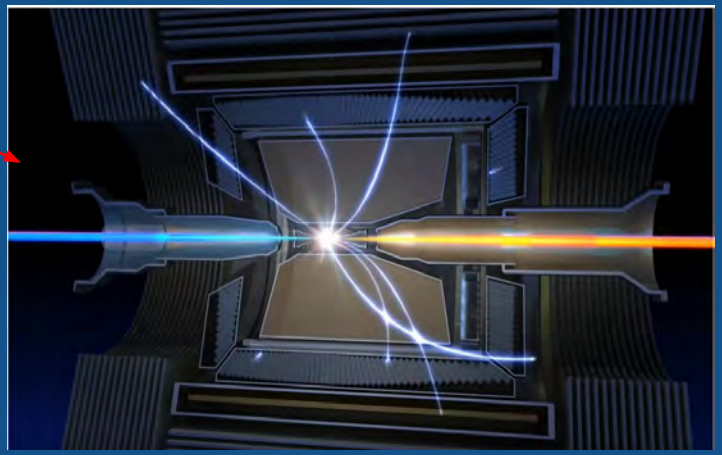
WHERE WE STARTED

A Search for New Physics – The Belle II Experiment

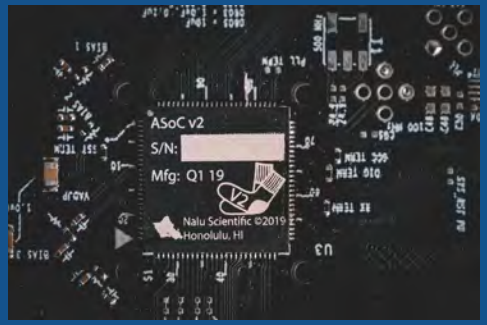


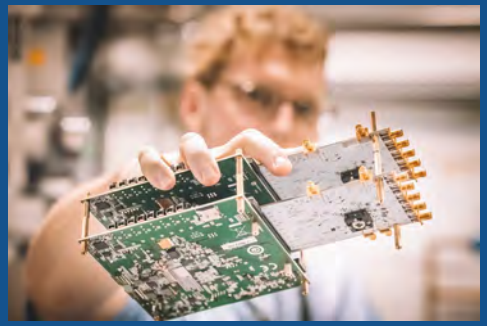
Tsukuba City
Located 60 mi north of Tokyo

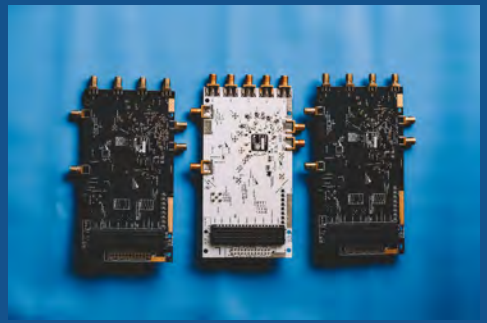
High Energy Accelerator Research Facility (KEK)
in Tsukuba



Interaction point inside the electron/positron collider
Source: KEK Youtube channel







ABOUT NALU SCIENTIFIC

Agile Small Business in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- Staff members with PhDs, MSc, and BSc
- Access to advanced design tools
- Rapid design, prototyping and testing

Vertically Integrated Team:

Microelectronics	Analog + digital System-on-Chip (SoC)
Hardware	Complex multi-layer PCBs
Firmware	FPGAs, CPUs, Embedded
Software	Data science, GUI, documentation
Scientific	Plasma, medical, physicists, space

Past Accomplishments:

- 5x Phase I/II SBIRs transitioned
- Developed microchip from R&D to COTS (available via CAEN)
- 3x US Patents Issued
- Over $3M in non-SBIR sales of products and services

CAEN Technologies Inc.

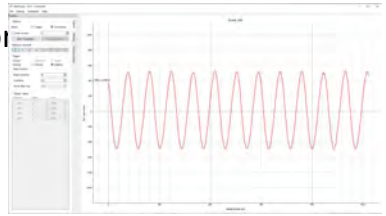
Nalu = 'wave' in native Hawaiian language

NALU SCIENTIFIC
ENABLING INNOVATION

Current ASIC Projects

Project	Sampling (GHz)	BW (GHz)	Buffer (Samples)	Number of Channels	Timing Res. (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-2	0.6	2k	32/64	80-120	Rev 2 avail
AARDVARC	8-14	2.2	16k	8	10	Rev 4 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5	4k	16	10	Rev 1 avail

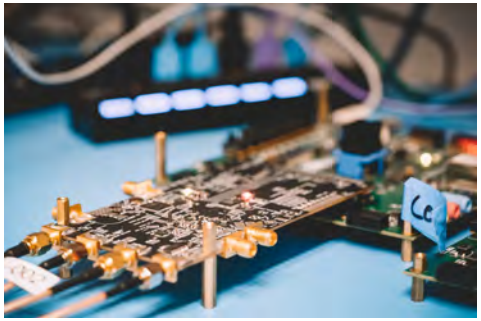
- DOE Phase I/II SBIRs
- Low SWaP-C specialty digitizers for
  - Radiation detection
  - Photonic sensors
  - Time of Flight (ToF)
  - Medical imaging
  - Space
  - Rad hard and harsh
- Evaluation PCBs available
- Extensive suite of software tools
- All microchips and tools available through CAEN Technologies USA



Software

Eval PCB

Microchips



AODS Project Highlights

Low channel count, low cost, digitizer with daisy chain and high dynamic range options.

Overall technical objective:

Functional AODS chip fabricated, tested, characterized and documented:

a. On-chip generated clocks and their associations
b. On-chip signal processing capabilities for Phase I (a simplified DSP)
c. On-chip calibration circuitry
d. Digital transceivers and failsafe mechanisms for daisy-chain operation

Parameter	Specification
Sample rate	1-2 GSa/s
Analog Bandwidth	500MHz
No. bits	12
Supply Voltage	2.5V
Dynamic Range	60 dB
Virtual dynamic Range	90 dB
Timing accuracy	<100ps
Gain Response	As low as 32 ns
Input noise	1mV
Gain stages	0dB,15dB, 30dB, (45dB)
Analog buffer	16k samples
Integration	SoC
Serial Rate	500Mbps

Phase II technical objectives:

1. AODS Design: it will be based on the experience gained from Phase I and will benefit from a top-down approach that will provide basis for further verification. Analog front end will guarantee programmable gain, termination and high dynamic range. Digital back end will provide dynamic range integration, digital signal processing and communication (daisy chaining) features.
2. AODS Verification: based on previously defined specifications will be separately performed on analog and digital portions and the overall chip
3. AODS Prototype Fabrication: will use well-tested 250 nm technology to reduce the risk
4. AODS Evaluation PCB Design: will emphasize extensive testing of all the novel AODS features
5. Firmware/Software and testing : design and development of firmware and software to allow extensive testing of all AODS features, as well as basis for standalone use of evaluation boards by potential users.

AODS V2 DESIGN DETAILS

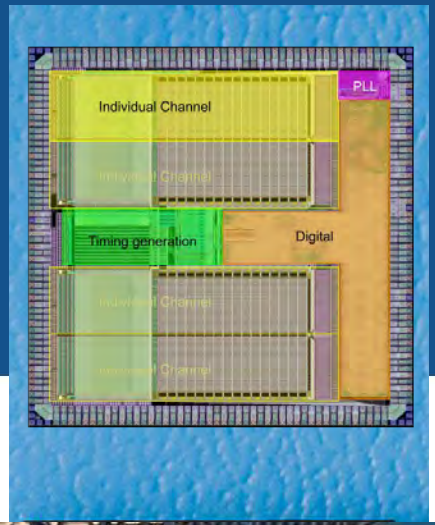
Compact, high performance waveform digitizer

- Mid performance digitizer: 1-2 Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

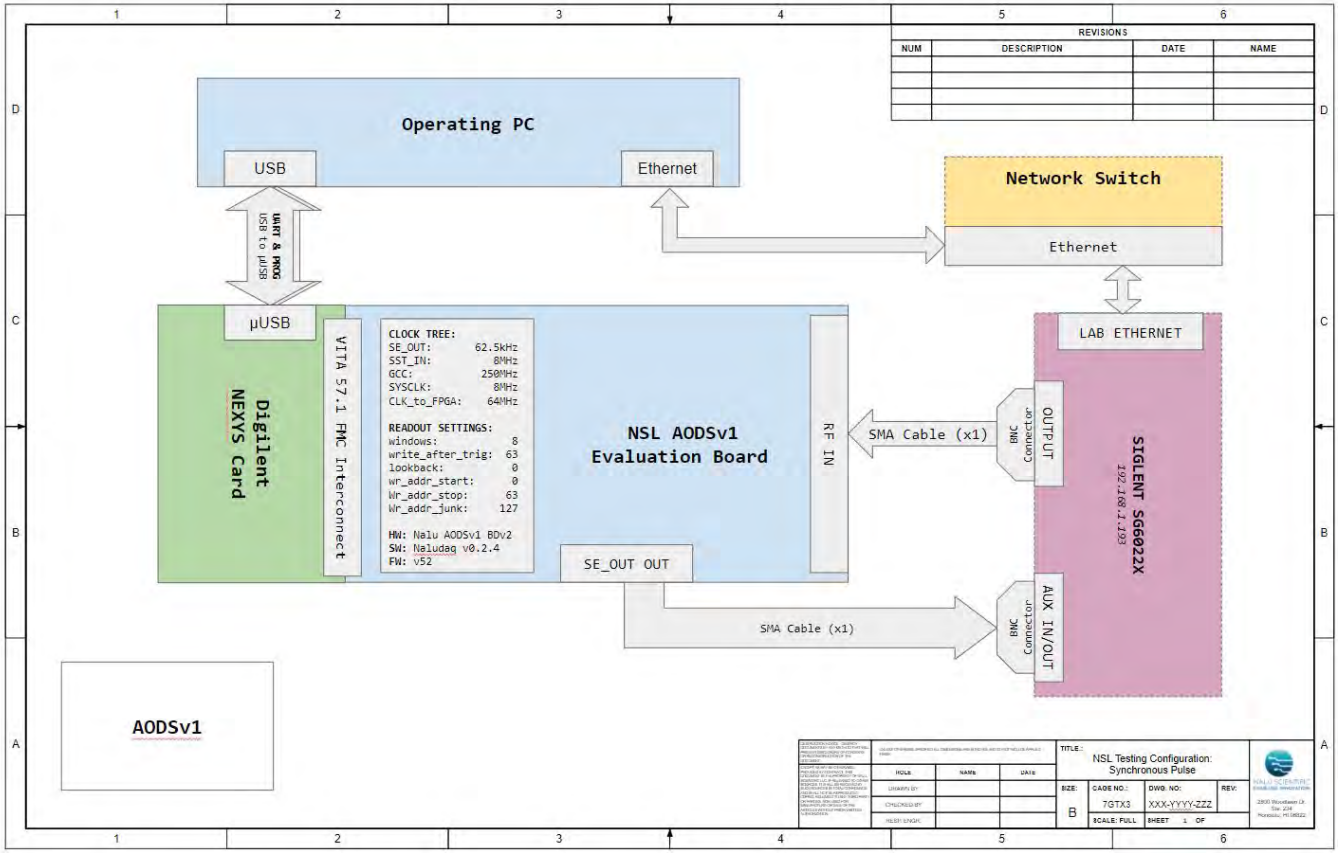
Parameter	Spec
Sample rate	1-1.5 GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	50-100ps
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- High dynamic range mode
- Self triggering
- Eval cards available
- Custom boards under dev

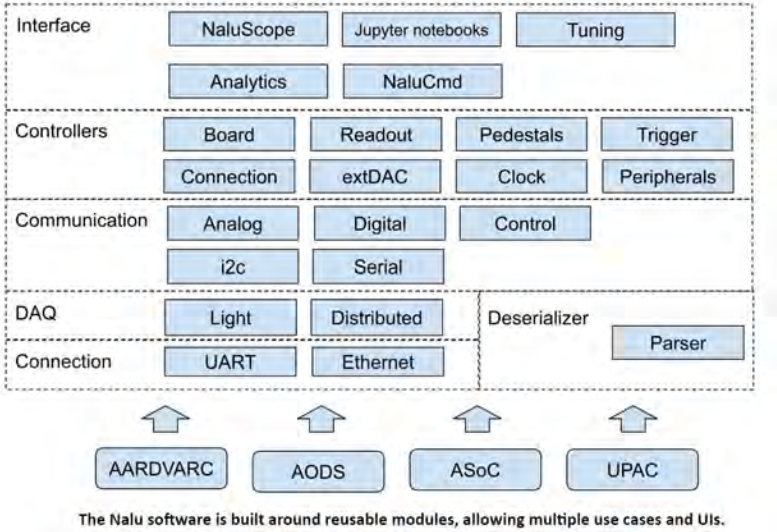
IEEE NSS 2020, 2022



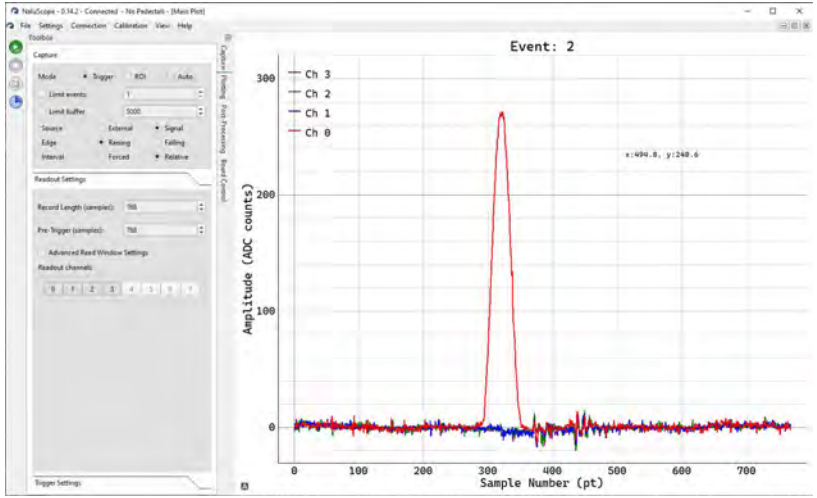
Test Setup



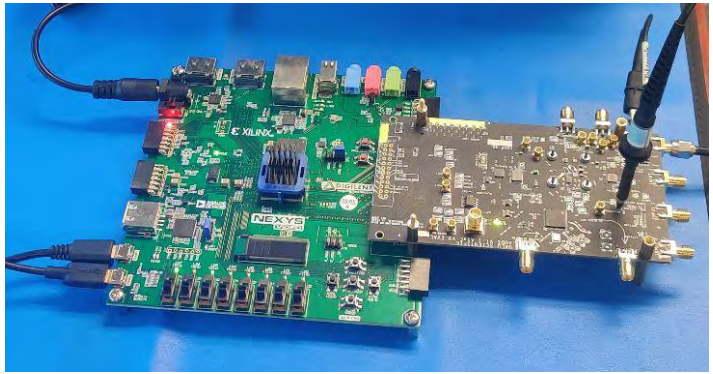
NaluScope Common Software and GUI



The Nalu software is built around reusable modules, allowing multiple use cases and UIs.



- Windows/Linux PC
- USB interface
- GUI, CLI interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage

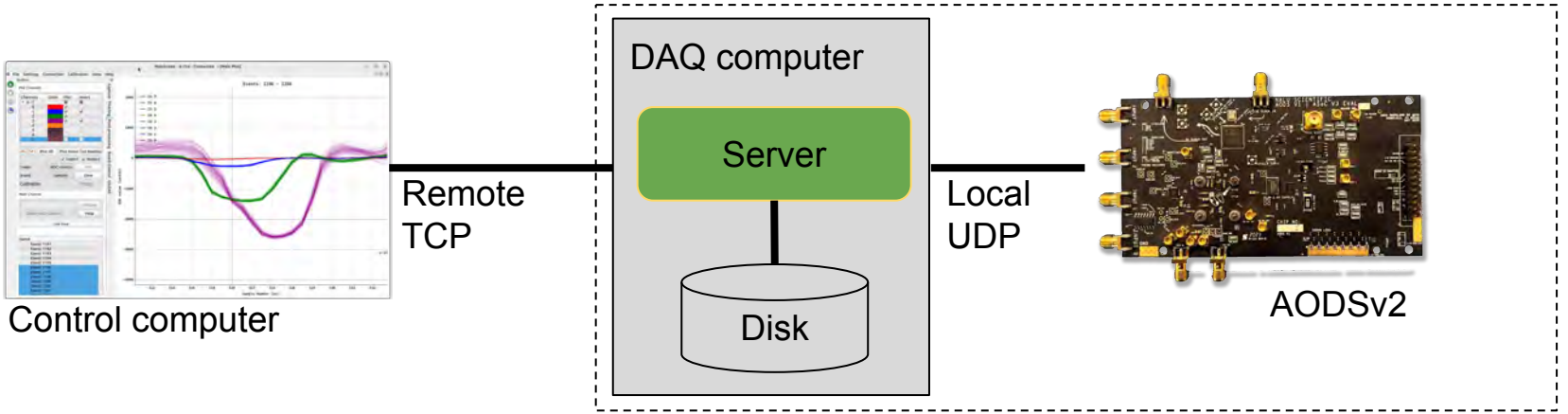


Software/Firmware Activities

- FW/SW development:
  - GbE Readout speed integrated in NaluScope
  - Standalone GbE server with remote control capabilities
  - Gigabit ethernet firmware for AODS evaluation platform
  - Gigabit ethernet firmware for DSA L platform
  - Calibration tool for gainstages implemented in GUI
- Multichip control API upgraded
- NaluScope AODS specific manual (commercialization)
- Port back-end from Python to Rust
- Support site added **support.naluscientific.com** (commercialization)

Gigabit ethernet

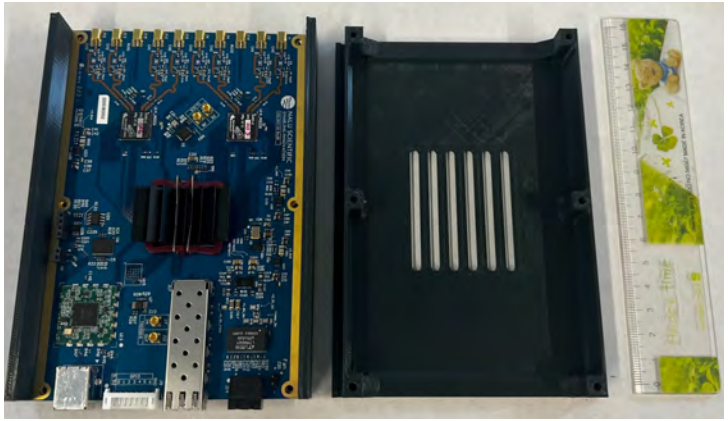
- New rust based backend for gigabit ethernet
- Rust language cut development time for production ready
- GbE backend server used in Naluscope
- Backend server can be run independently, allowing for interesting hardware configurations.
- Designed to run on most Embedded Linux, Linux
- Server can run on low end hardware such as raspberry pi.



Benchtop AODS Based Digitizer

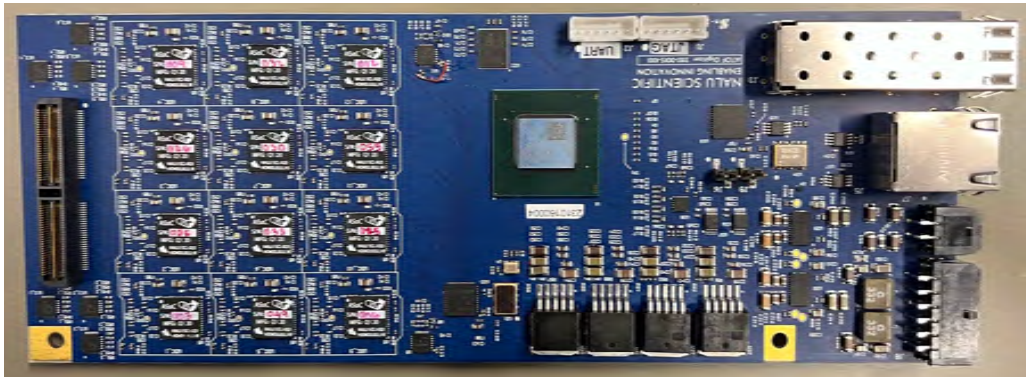
Product Name: DSA L3-8+
Product Description: 8 channel, 1-2 GSa/s digitizer with built-in amplifier
Dimensions: ~ 6” x 4” x 1”
Gain: 19.5dB, replaceable
Bandwidth: ~500 MHz
Digitizer Chip: AODS V2
Sample rate: 1-2 GSa/s
Power: USB
Data: USB/UART, GbE UDP
Integration: amps, chip, FPGA, clock, regulators, comm, FW, SW
Trigger: Internal, External, Software

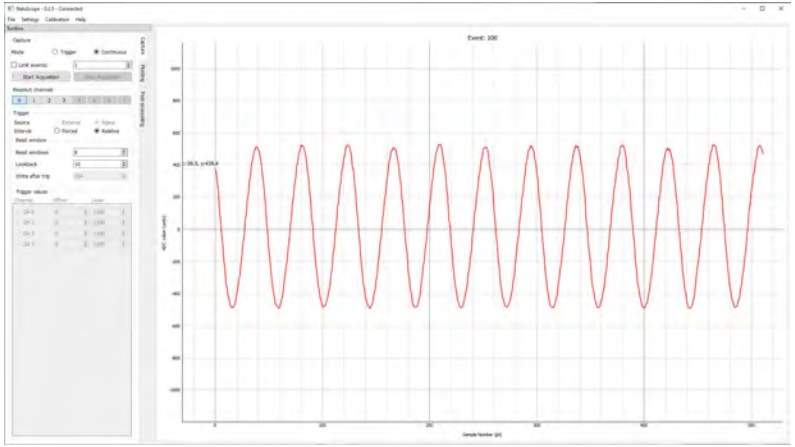
*DSA: Digitizer for Specific Applications



Product Description

Product Name: DSA A3-48
Product Description: 48 channels, 3.2 GSa/s
Dimensions: ~ 8” x 3” x 1”
Bandwidth: ~800 MHz
Trigger rate: Designed for up to 20 kHz
Digitizer Chip: ASoC V3
Sample rate: 2.4-3.2 GSa/s
Power: External
Data: USB/UART, GbE
Integration: chip, FPGA, clock, regulators, comm, FW, SW
Trigger: Internal, External, Software
Timing resolution: 30-50ps achievable



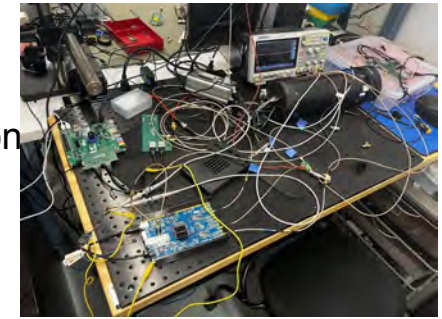


Prototype HW and preliminary FW/SW is available.
Funded by NP, under test at Argonne/JLAB

<u>ASoC based digitizer that is pin compatible with AODS.</u>

Summary of Activities

- Initially fell behind schedule:
  - Phase Started in April 2020 - pandemic onset
  - Extra time needed for extensive testing
  - Supply chain problems: FPGA, reg, clock chip
- Generally caught up on schedule given the NCE
- AODS V2 designed and fabricated in Feb 2022
- AODS V2 testing complete
- Synergistic project:
  - High Dynamic Range Lidar readout for Oceanography Application

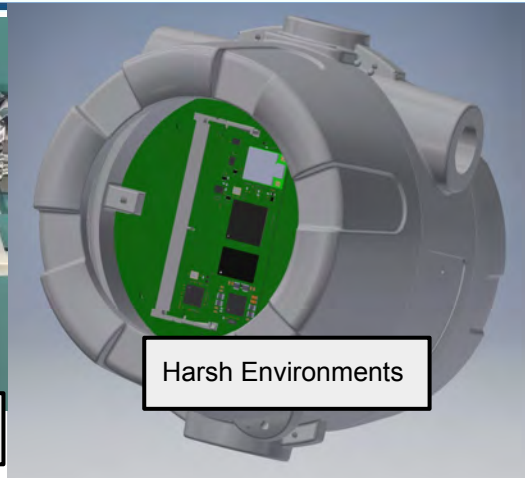


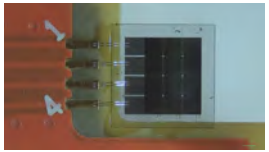
- Next steps:
  - TID - customers funded
  - Test board designed for high dynamic range mode
  - SW/FW for high dynamic range mode - prelim version available

Commercialization

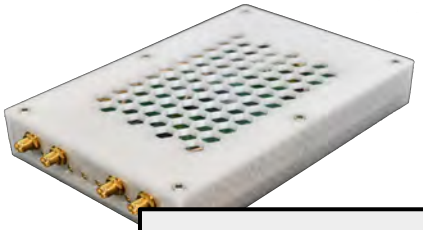
- Executing on distribution agreement w CAEN
- Supply chain is fully recovered
- Attended several trade shows/conferences (overhead funded)
- Increased sales activity
- Several integration NRE contracts from labs
- FFP product sales contracts from labs
- Users want a solution (box), than a chip:
  - Vertical integration (chip+HW+FW+SW+app note)
  - Focus on value-add engineering
  - Multi discipline knowledge of the user needs
- Product development contracts from commercial entities

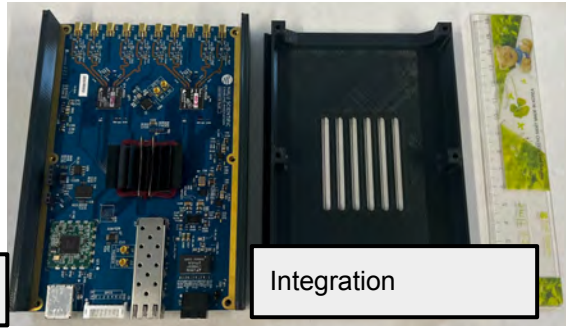

Products Shipped


Harsh Environments


Sensor Integration

EMI Shielding


Full Integration


Integration

Funding, Collaboration and Workforce Development

FY16-22

Funds Secured by Nalu

- ✔ 9x SBIR Phase I
- ✔ 6x SBIR Phase II
- ✔ Various matching grants
- ✔ Misc. contracts

FY16-22

Sponsored Research

- ✔ University of Hawaii
- ✔ National Labs
- ✔ 5x post docs
- ✔ 5x graduate students

FY23-26

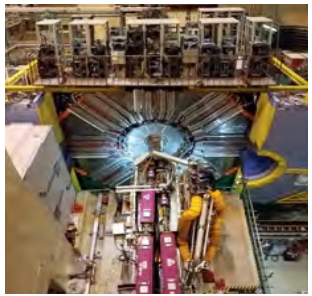
✔ **New possibilities:**

- ✔ New tech-dev based on capabilities
- ✔ Sensor integration: medical, space
- ✔ Custom design
- ✔ New partnerships

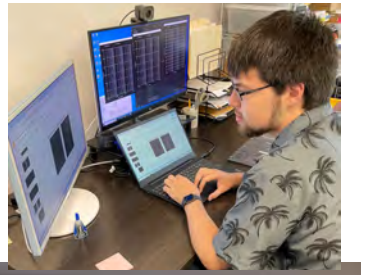
Why Hawaii?

- Strategic location - Asia <> US
- University of Hawaii
- Large impact on local economy
- "Hawaii Brand"
- Retain local expertise

2x MS and 2x PhDs had their first jobs at Nalu Scientific.



Conferences and Events



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NOAA