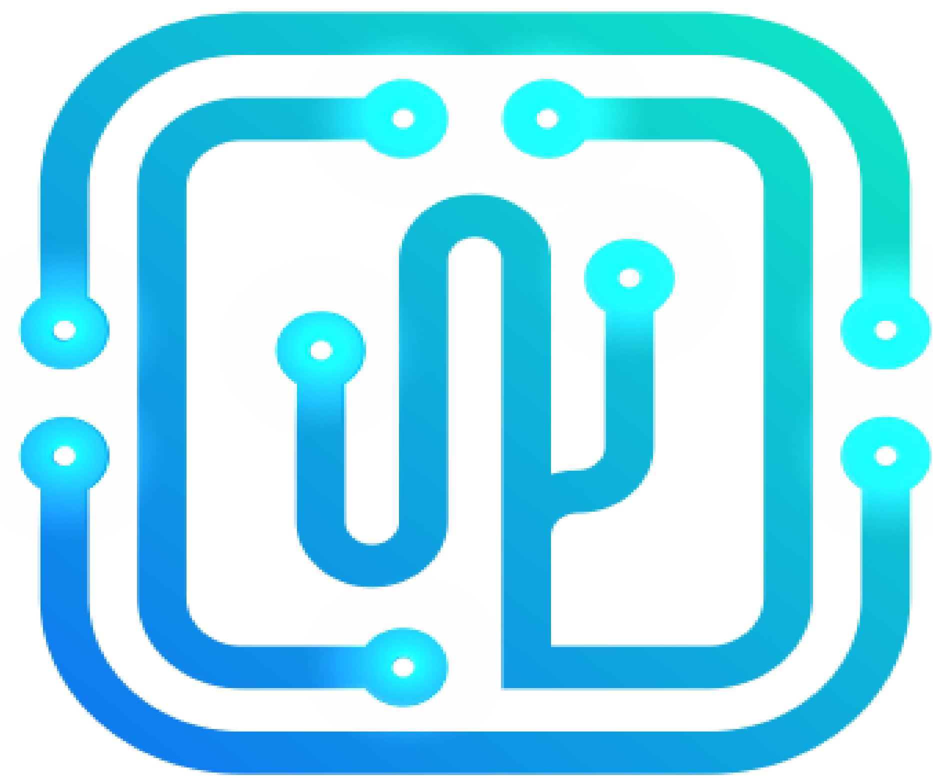


CACTUS MATERIALS

A compound semiconductor integrated device manufacturing company for AI Photonics and Power

September 3, 2024

LEADERSHIP TEAM

Rafi Islam, PhD
CEO/CTO

- PhD in Materials Engineering from ASU
- 13+ years in manufacturing at Intel
- 20 years of experience in the Semiconductor Industry
- Ironman Triathlete

Iqbal Ali, PhD
Director of Engr.

- PhD in Materials Science U of Arizona
- Worked for Intel, Applied Materials, Texas Instruments
- Spent two years building a FAB in Moscow

Roger Spencer, MBA
Director of Sales

- 30 years of semiconductor experience'
- Experience includes working in DEC and Intel

Marc Papageorge,
Director of operation & Business Dev.

- MS from U. Florida Materials Engineering
- 30+ patents, publications, and engineering awards
- Former COO of Sicamore Semiconductor

Ron Elwood, CPA
CFO

- 30 years of C-level experience in various accounting roles
- CFO role with Baer, Inc. and Bright International Corp.
- Lead on Audit Committee.

Andrew Schwinger
Business Development

- 7 years of experience in both consulting and business development
- 15 years of experience in banking and investment mgmt. in the USA, Tokyo, and Hong Kong
- Competitive Swimmer

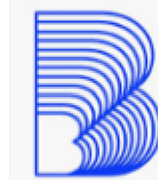
Previous Tech Firm

Previous Tech Firm

Previous Tech Firm

Previous Tech Firm

Business Background



Business Background

THE PRIVATE BANK

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CACTUS MATERIALS HISTORY

2016-2017	**Founded; Stealth Mode; R&D**
2023-PRESENT	*** To meet growth, we acquire larger state-of-the-art semiconductor fab to scale up our products** *** ITAR, ISO-9001 Cert, and DoD trusted Supply by Q4, 2024**
PATENTS	**100+ Patents**
US RESHORING	**National Defense Authorization Act *regulated* that 70% of defense semiconductors need to be Made in USA by 2031 + Dawn of AI Industry 100% reliant on "Compute".**

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TEMPE ARIZONA FACILITY

ITAR REGISTERED AND DEPARTMENT OF DEFENSE (DOD) TRUSTED SUPPLIER BY Q4, 2024

State of the art 40,000 sq ft.

Class 100 Clean Room

2 MBEs (Molecular Beam Epitaxy)

2 MOCVDs (Metal Organic Vapor Deposition)

100+ pieces of advanced Equipment & tools

Design, develop, & manufacture Compound, AI, and Power semiconductors

LINK

1.5 Minute Video Clip of the Fab

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A New Approach to Achieving High Granularity in Low-Gain Avalanche Detectors (Phase II-NCE)

Rafiqul Islam, PhD. Cactus Materials, Inc. (PI)

Collaborator:
Bruce A Schumm, PhD. UCSC, Santa Cruz Institute for Particle Physics
Gabriele Giacomini, PhD, Brookhaven National Lab

Acknowledging the support of the US Department of Energy

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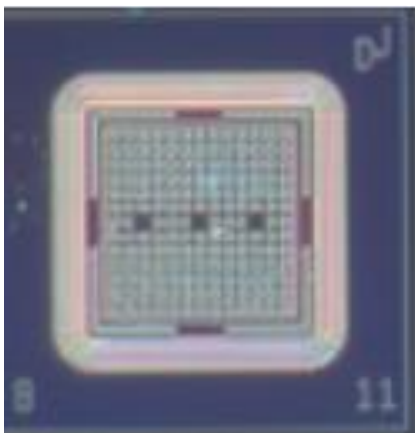
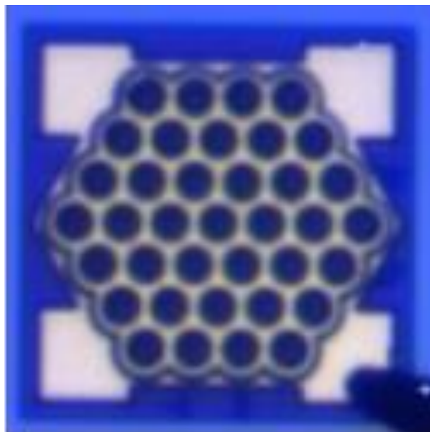
CURRENT PRODUCTS & SERVICES

AI Photonics

- ULTRA UFD and IRD Detectors Chip
- VICTORY VCSEL Laser Chip





Power

Silicon Carbide (SiC) MOSFET>3.3kV and Extreme Sensors

Strategic Services

- SiC Foundry Services (30% of the fab capacity)
- III-V Epitaxy Wafers Development
- Heterogenous 3D integration [W2W]
- Rad-hard Silicon Engineered Substrate

**Current capacity of the fab 50,000 wafers production/year*

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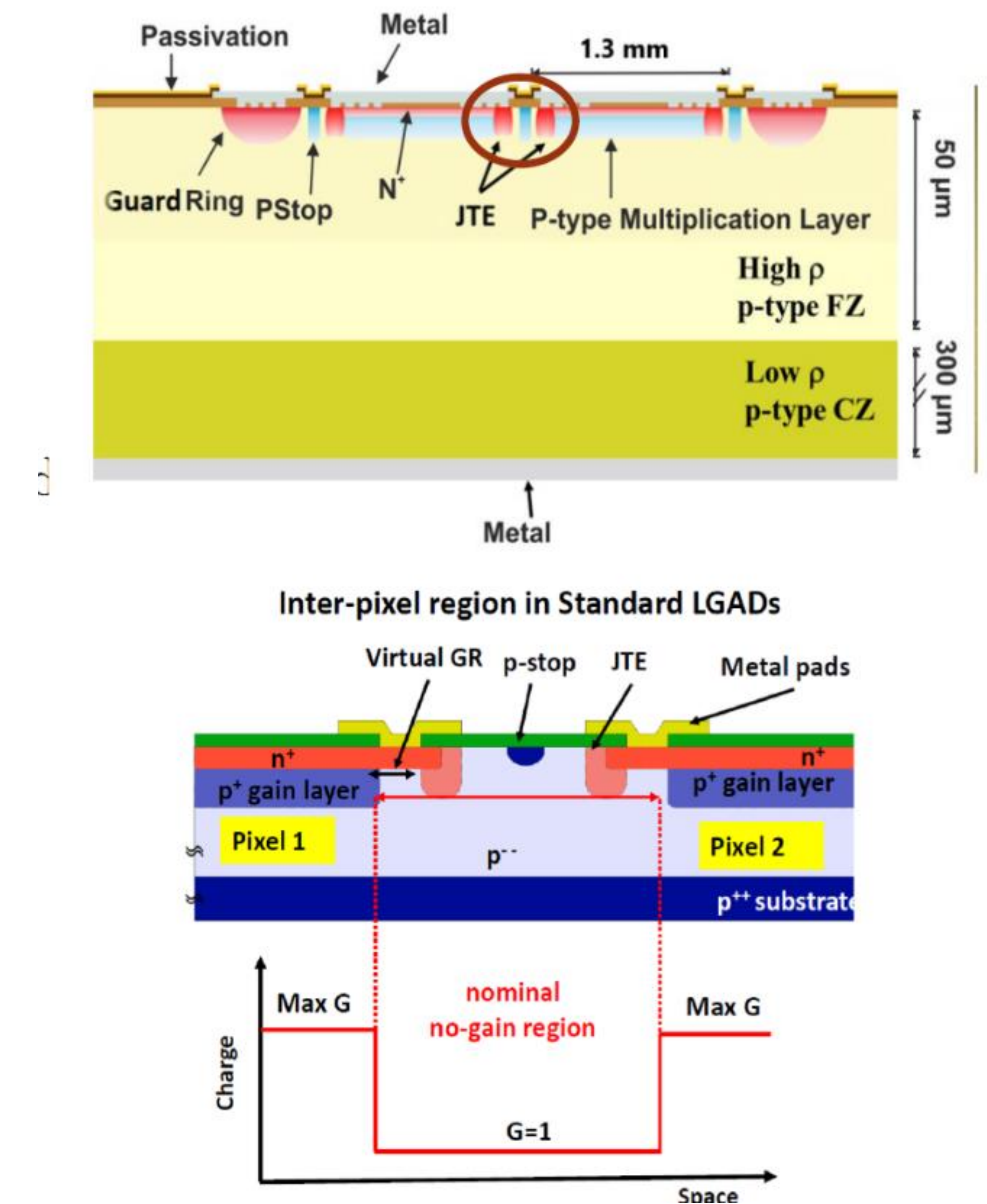
LGAD Arrays

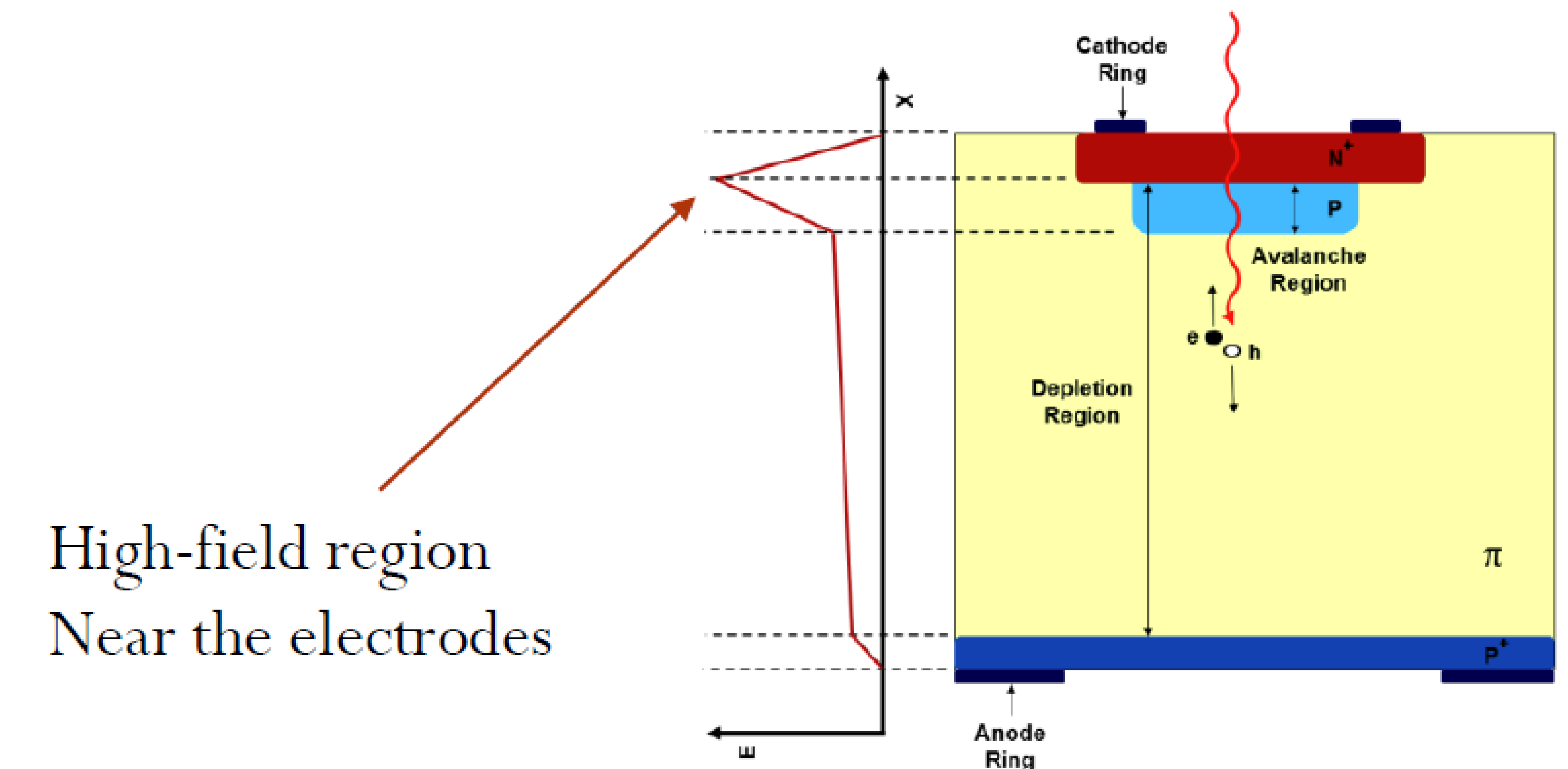
- Granularity is a current limitation for LGADs
- Due to high fields in the multiplication layer the pads needs electrical insulation
  - Protection structure: Junction Termination Extension (JTE)
  - Causes inter pad (IP) gap to 50-150 um, also changes with applied bias voltage
  - Limits LGAD granularity to mm scale
- However, 50 um pitch (and lower) is required for next generation colliders and 4D tracking
  - At least some level as the ATLAS new inner tracker (ITK)
- **Several possible solutions are being investigated at Cactus Materials, Inc.**
  - Deep Junction LGADs (Current Phase II-NCE)
  - Radiation Hardened AC LGADs
  - Trench Isolated LGADs
  - Double sided inverted LGADs
  - Focal Plane Detector

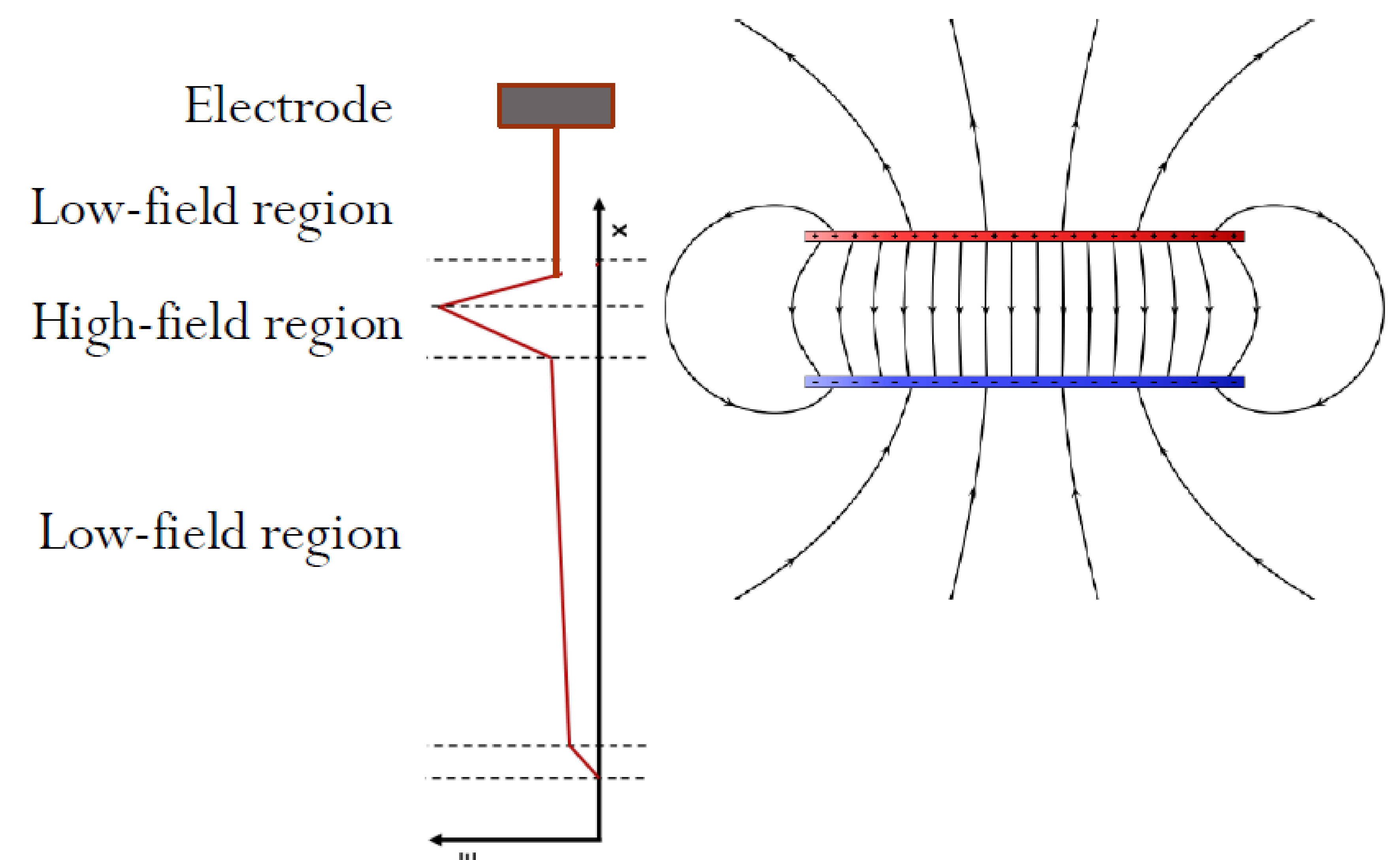


Picture Credit: FBK, Trento, Italy

A new approach: Deep Junction

- Granularity limit caused by high field near the electrode
  - What if the field is kept low while maintaining gain?
- Basic inspiration is that of the capacitive field
  - Large between plates, but surrounded by low field regions beyond the plates
- Use symmetric P-N junction to act as an effective capacitor
- Localized high field in junction region creates impact ionization
- Bury the P-N junction so that fields are low at the surface allowing conventional granularity

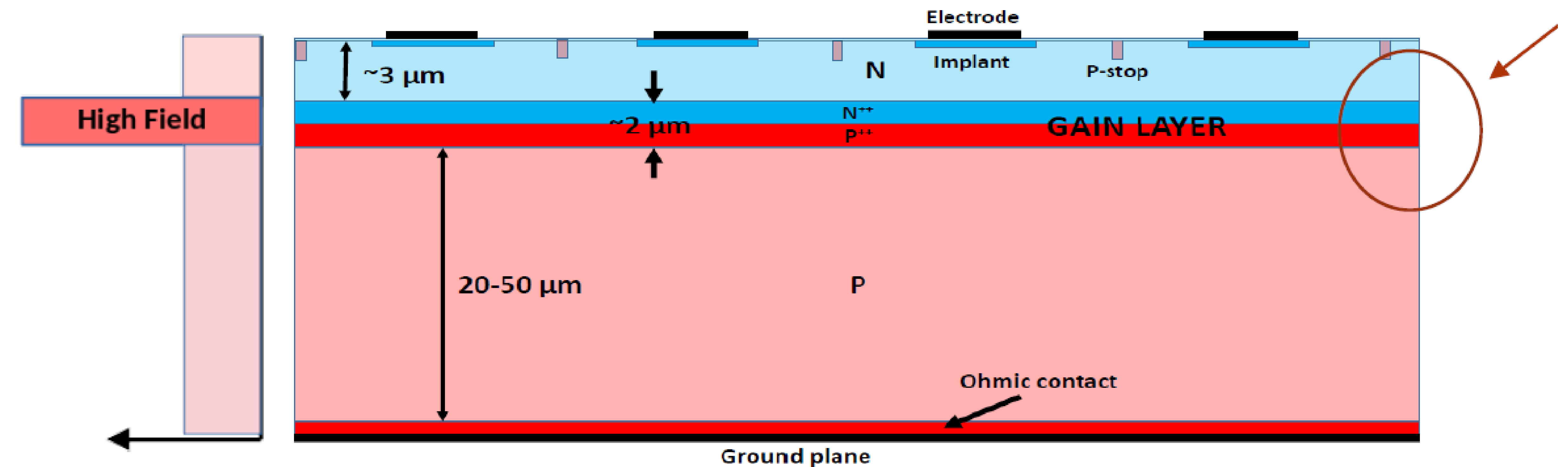


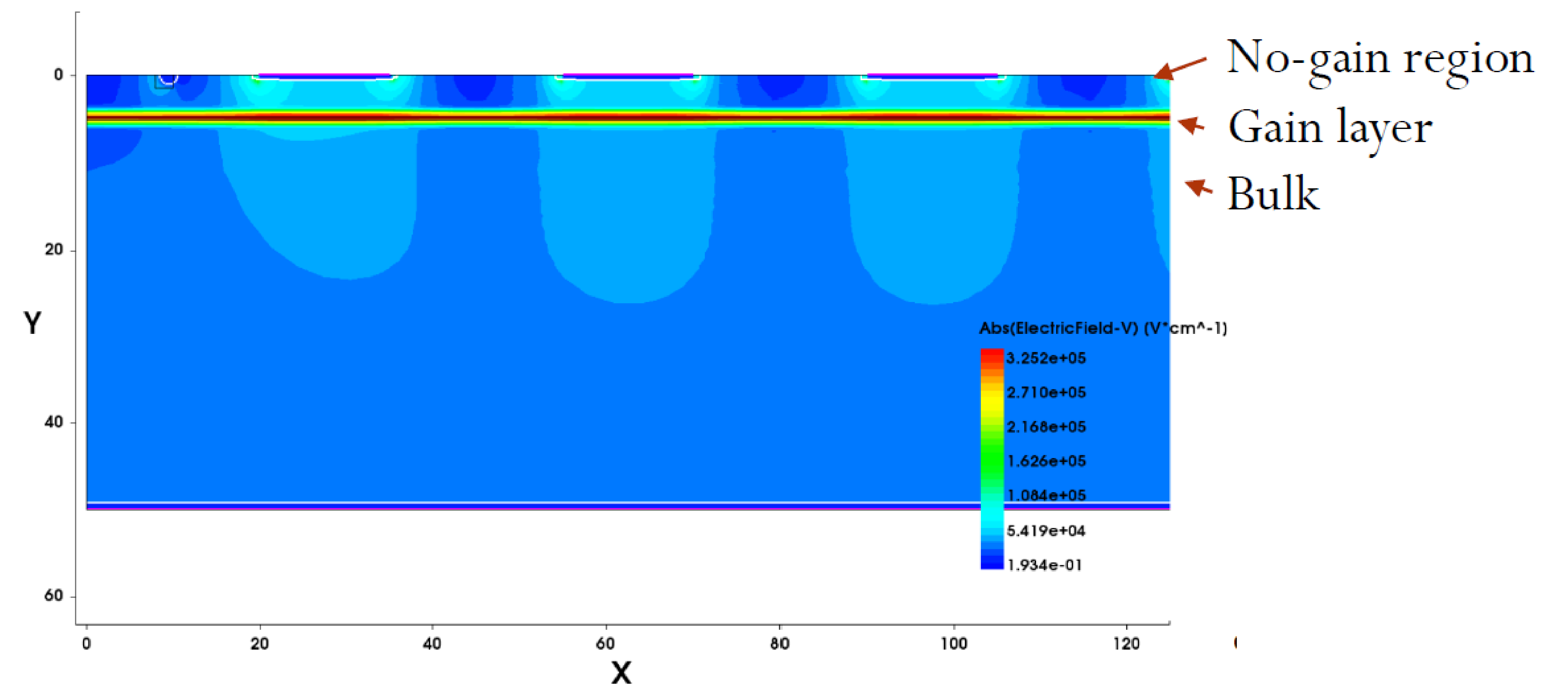


A new approach: Deep Junction

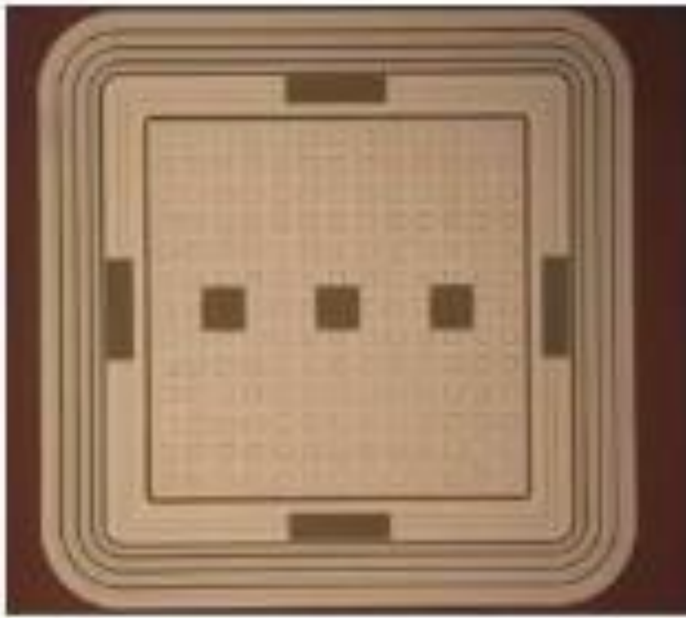
- P++ gain layer paired with a N++ layer that lowers the field
  - Junction is buried ~5 um inside the detector
- Tuning of N+ and P+ parameters important
  - Low field outside of the electrodes while maintaining sufficient gain
  - No need for a JTE
  - Different termination of the gain layer designed
- DJ-LGAD design studied with TCAD Sentaurus
- Production is ready to deploy at Cactus

Termination of the gain layer





Application Ecosystems



Cactus Materials Device

Nuclear Physics & HEP

Electron-Ion Collider (EIC)

X-ray imaging with high frame rate

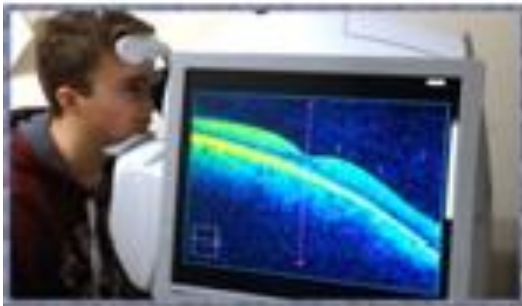
4D tracking

Medical Imaging (ex. PET)

CMS

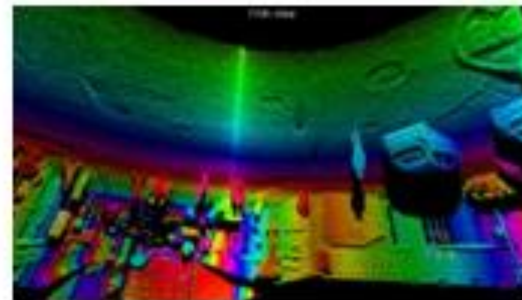
ATLAS

Potential Consumer



Medical / Cosmetic

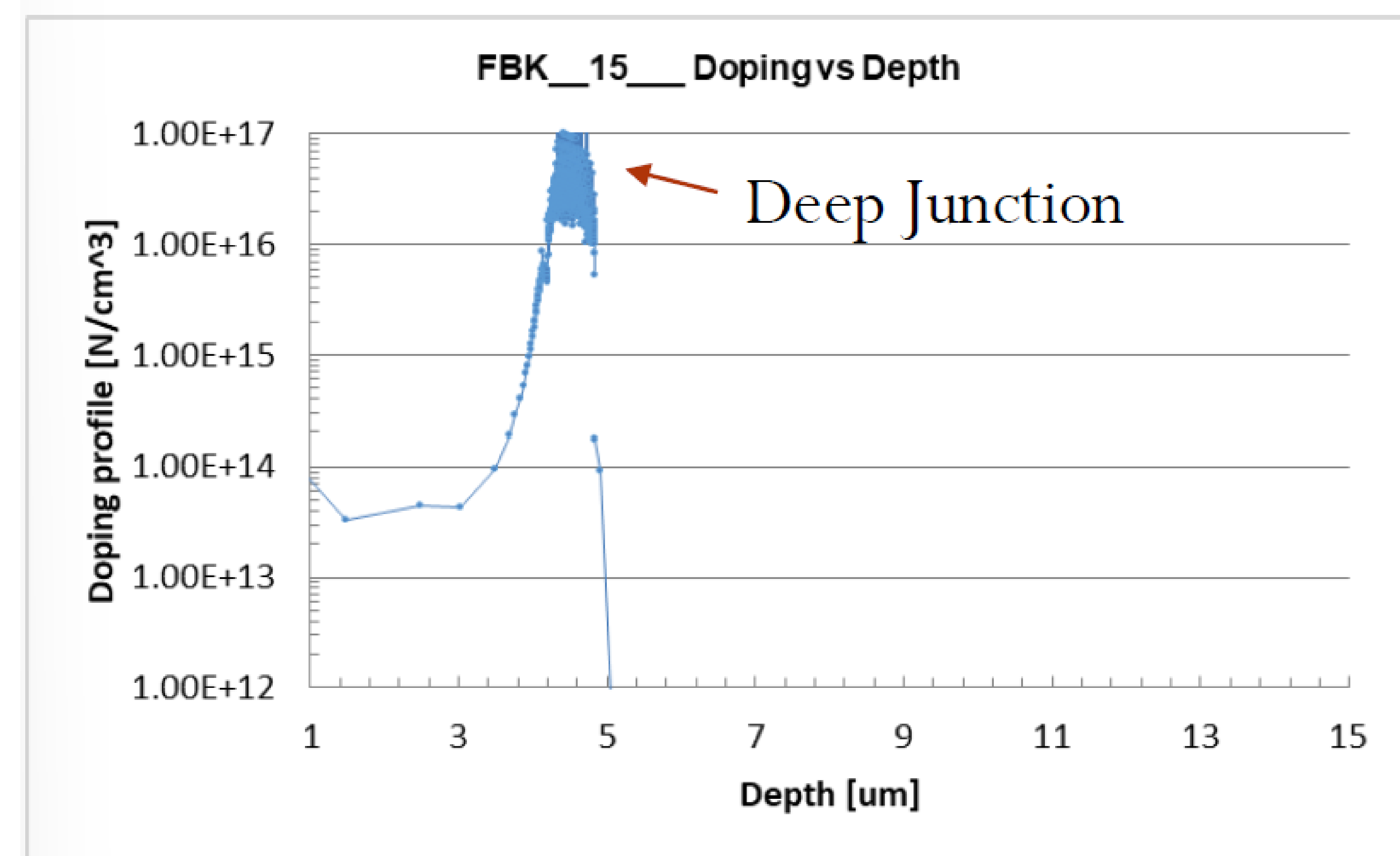
Optical Comm.
Data Centers



Defense

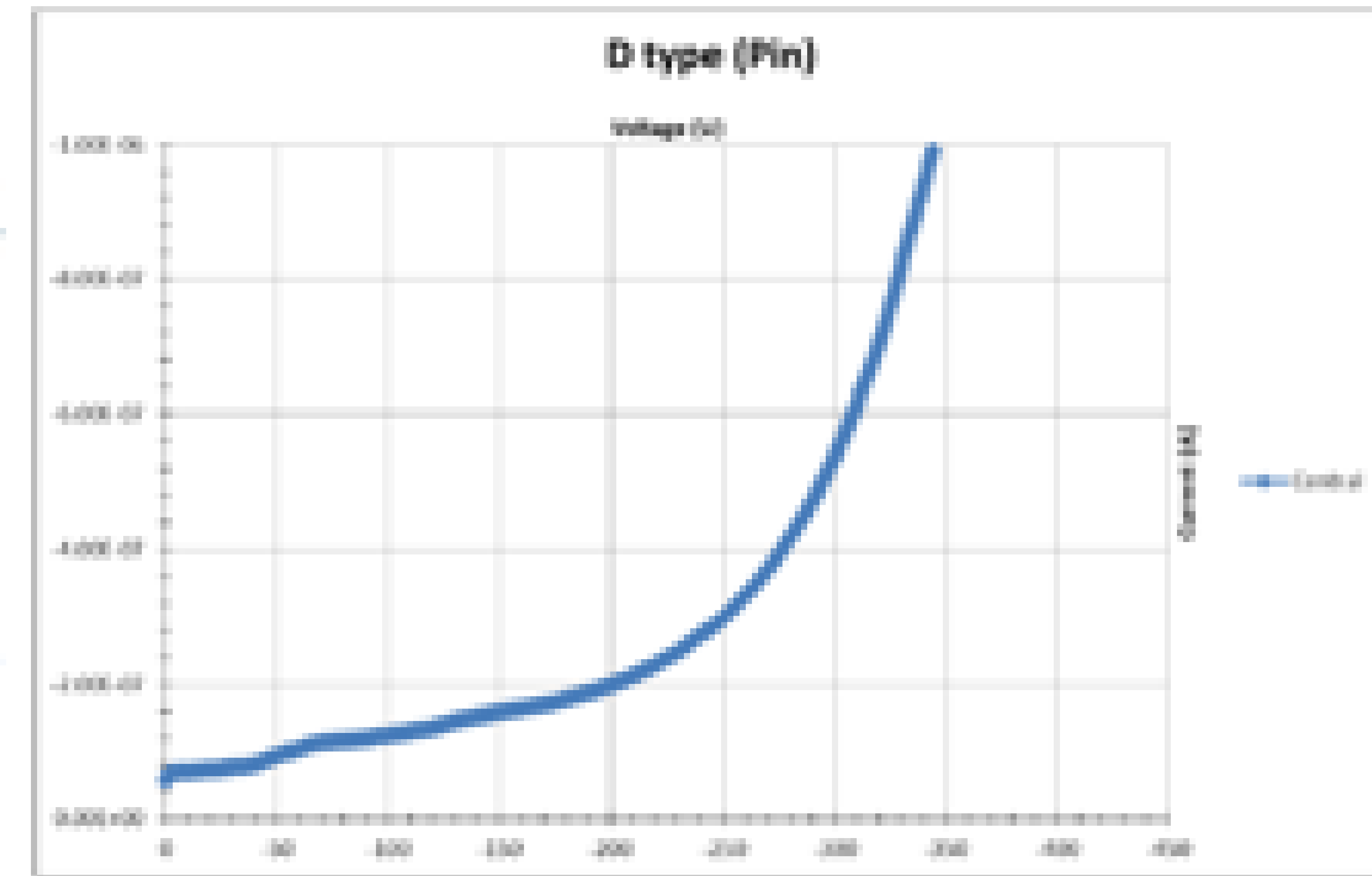
A new approach: Deep Junction

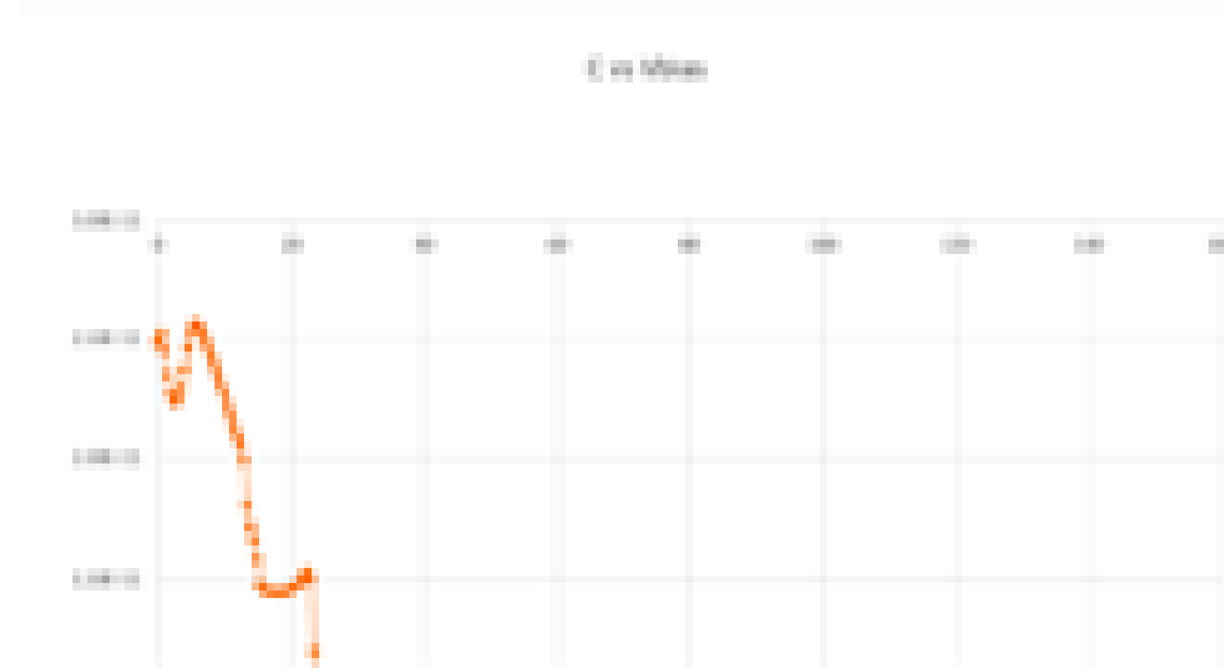
- Prototypes were performed in both epitaxy and wafer bonding(w2w) approaches:
- Prototypes can fully deplete and show gain
- 2x1 arrays were produced and show minimal IP gaps
    -

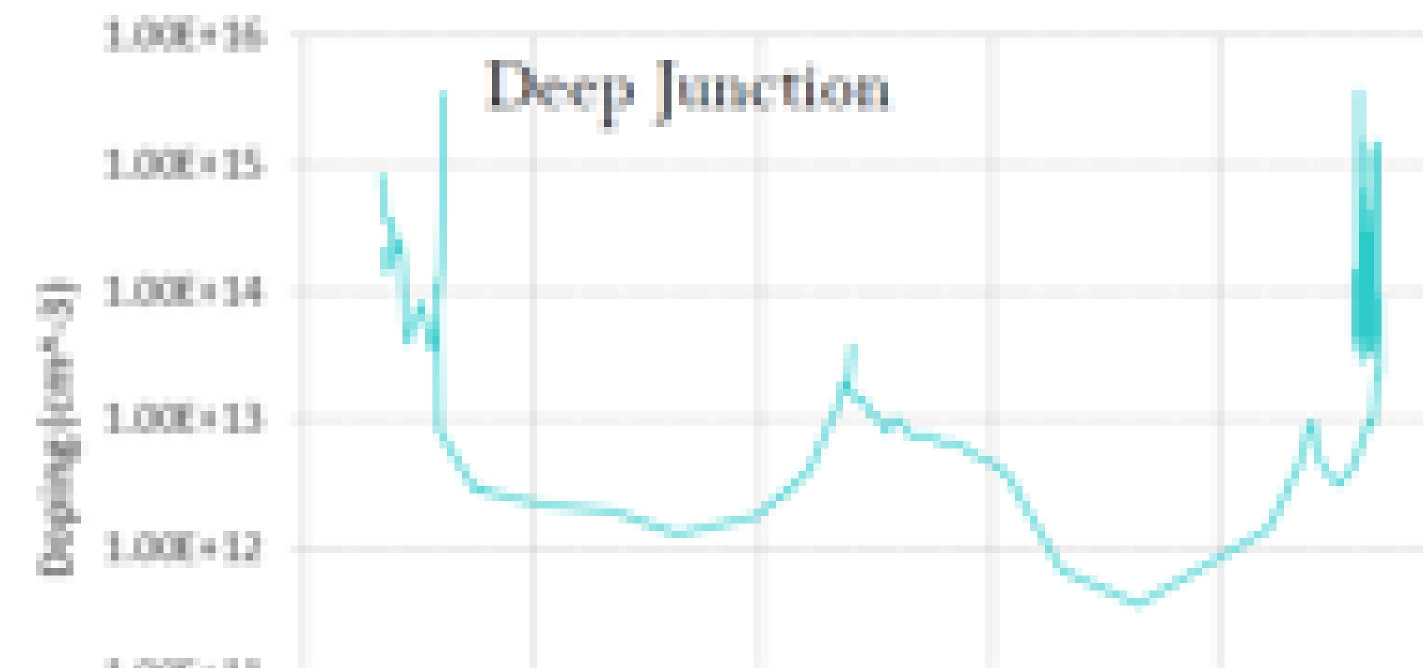


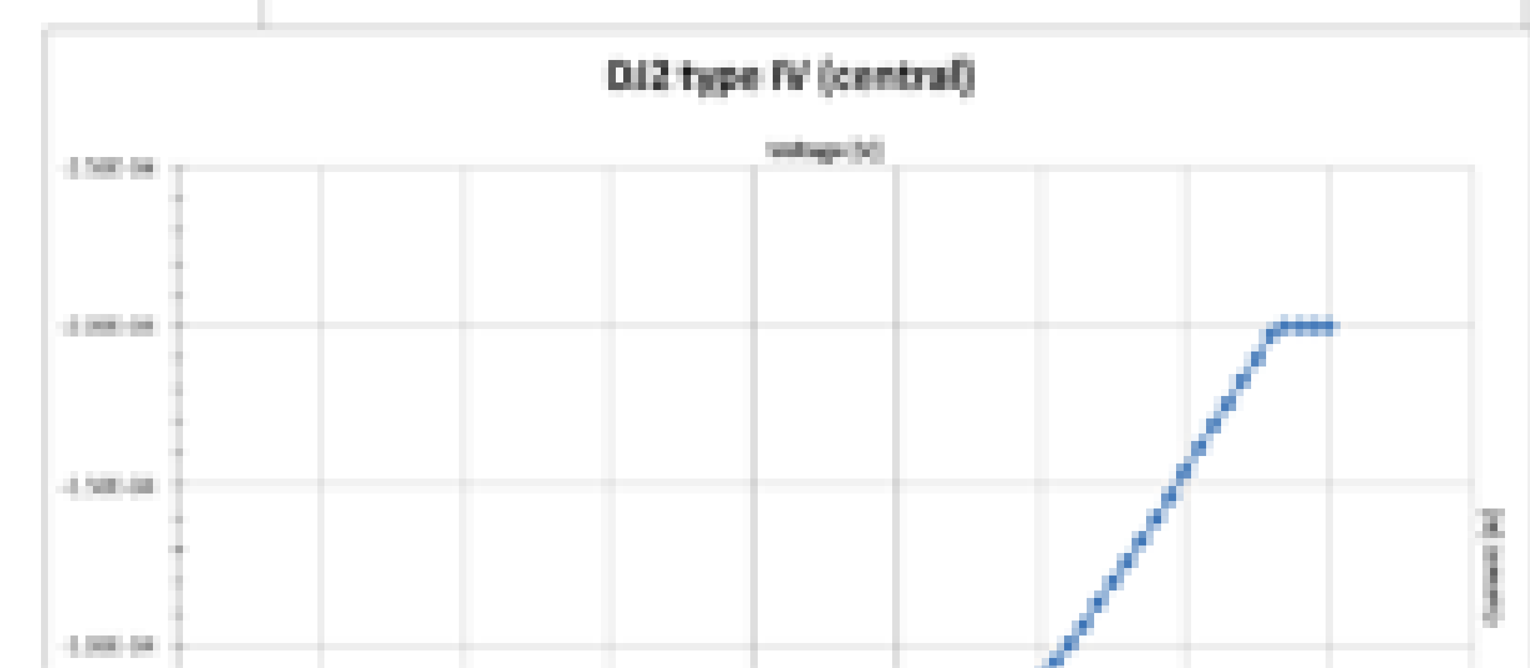
DJ-LGAD: Results

- D-type, standard PiN with deep junction, Current <1uA
- DJ-type, deep junction ending below the active area, High current (100s uA
  - The sensor is also very noisy, not usable
- DJ2-type, deep junction ending under the Guard ring,
  - Manageable current (10s uA), BV seems to be very high
  - CV shows deep junction structure, thickness seems higher than expected
- DJ3-type, 2x1 array, termination as DJ2, Manageable current (10s uA)



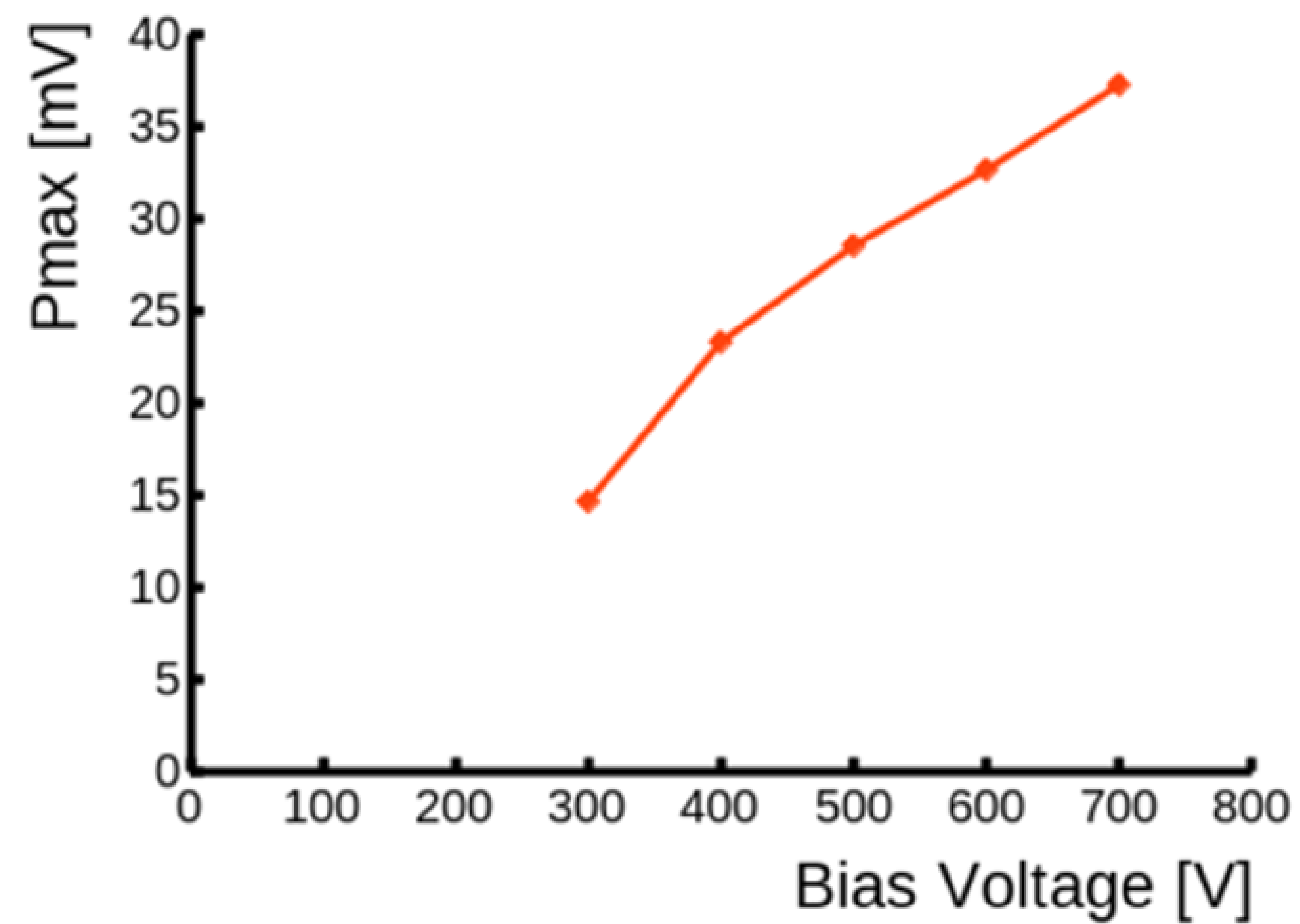


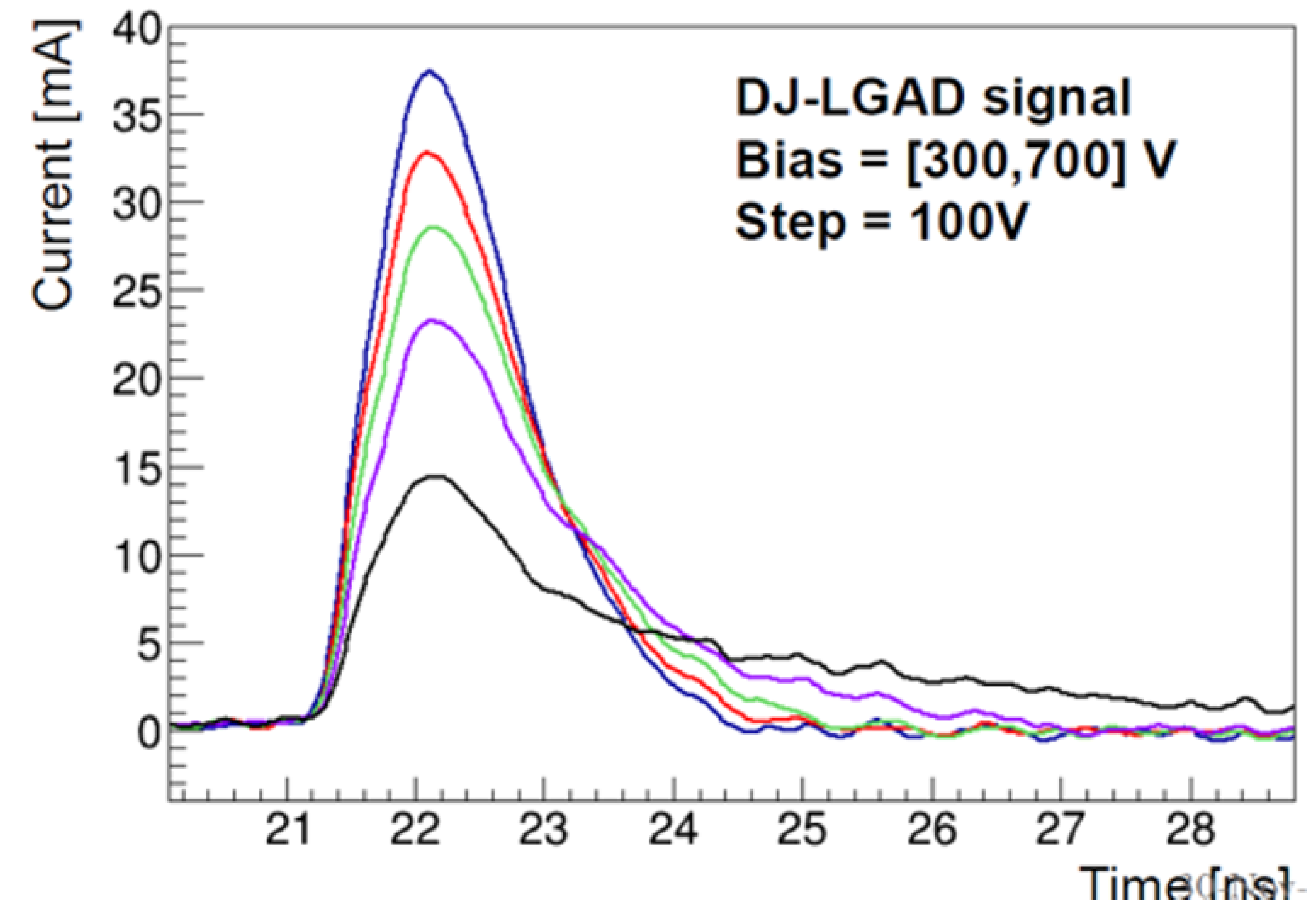




DJ-LGAD: Charge Collection Studies

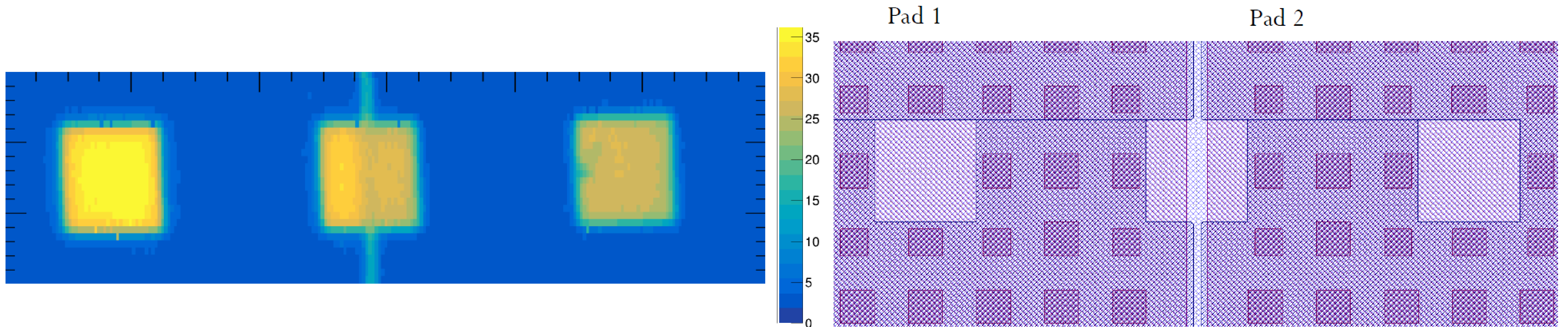
- Sensor mounted on UCSC 1ch and 4ch board, test with Sr90 source with know trigger sensor to study MiP response
  - Read out by fast oscilloscope, trigger on the trigger sensor
- **Rise time ~ 580 ps, similar to a typical 50-60um LGAD,** Breakdown >700V
- **Measured gain of ~ 3 to 5**
  - Lower than conventional LGAD
  - Optimization of the gain layer doping is required for future prototype





DJ-LGAD: Laser Studies

- **DJ-LGAD 2x1 array prototype is studied with IR Laser scan**
  - Digitized by fast scope, laser spot size is 10-20 um
- Pmax values in terms of the laser beam location are shown for sum of channels
  - Sensors have 3 open areas in the metal, one in each pad and in between pads
  - In the scan the blue low signal region corresponds to the metal
  - The sum of the two signals is more or less constant on the sensor (no gain loss in between pads)



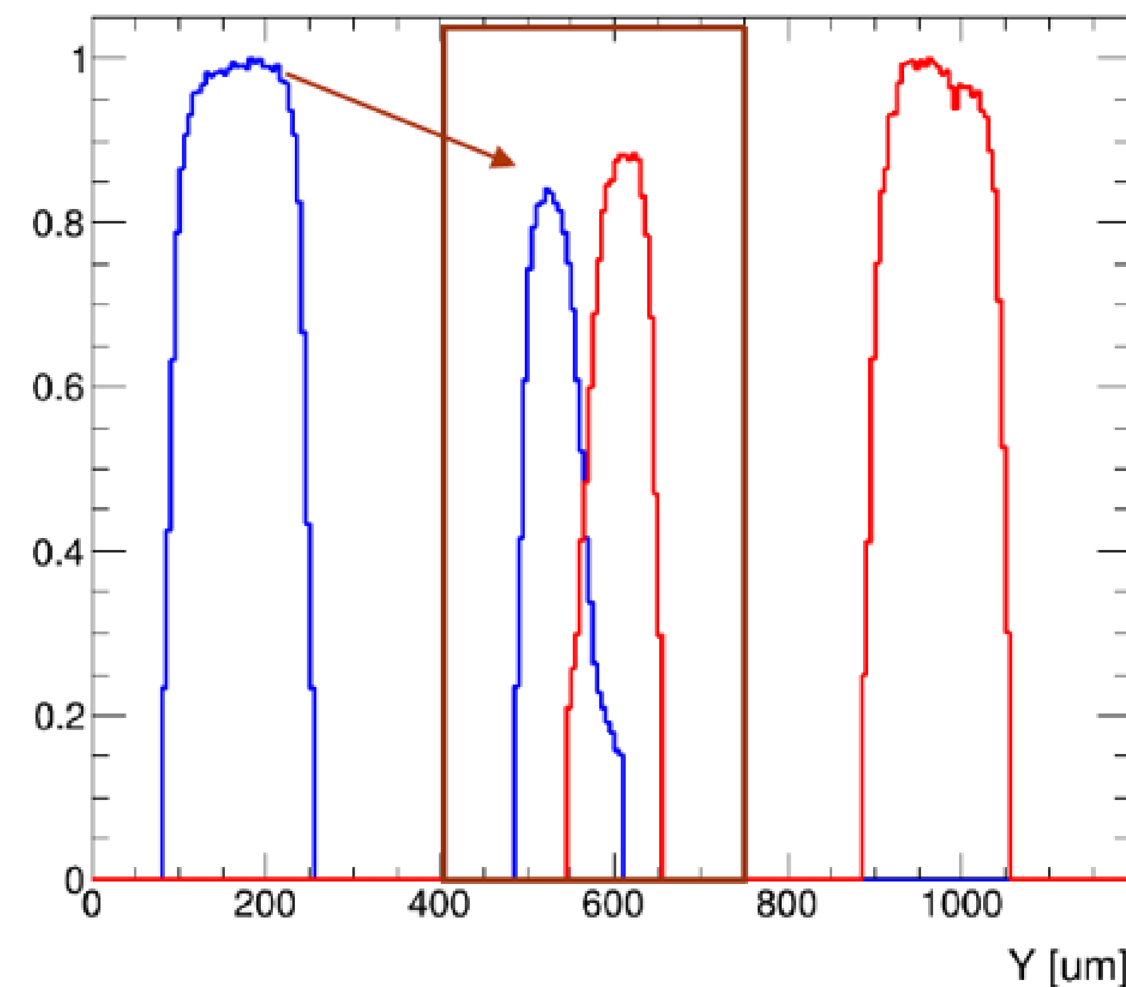
DJ-LGAD: Laser Studies

- **1D profile fractions shows a slightly lower signal next to the gap**
  - 2D simulation shows the field in the gain layer is reduced in the inter pad region
- Zoom in the inter pad region (nominal electrode gap is 30um)
  - Sum of signal show almost no reduction in the gain
  - Minor cross talk in a 50 um region between pads

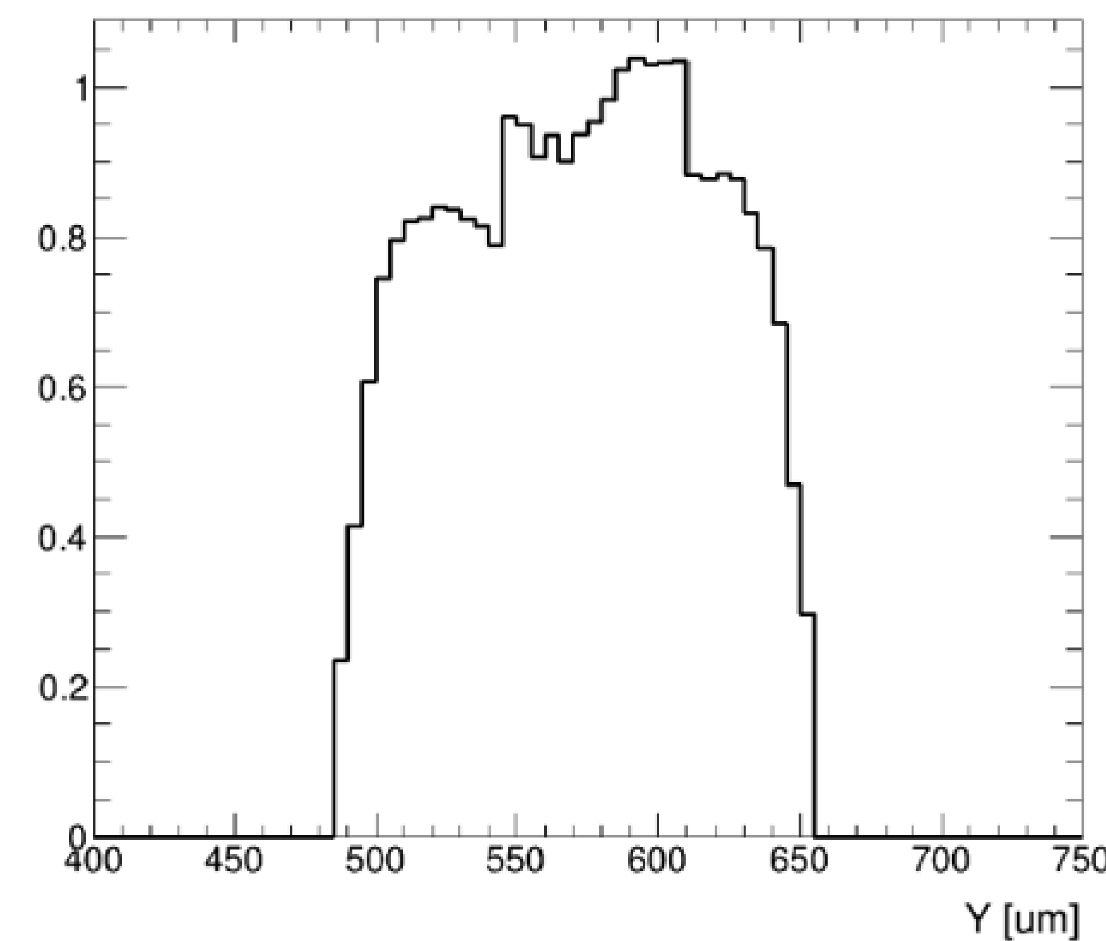
The pmax fraction of an individual strip is defined as:

$$pmax\ fraction\ (channel) = \frac{pmax\ (channel)}{\sum pmax}$$

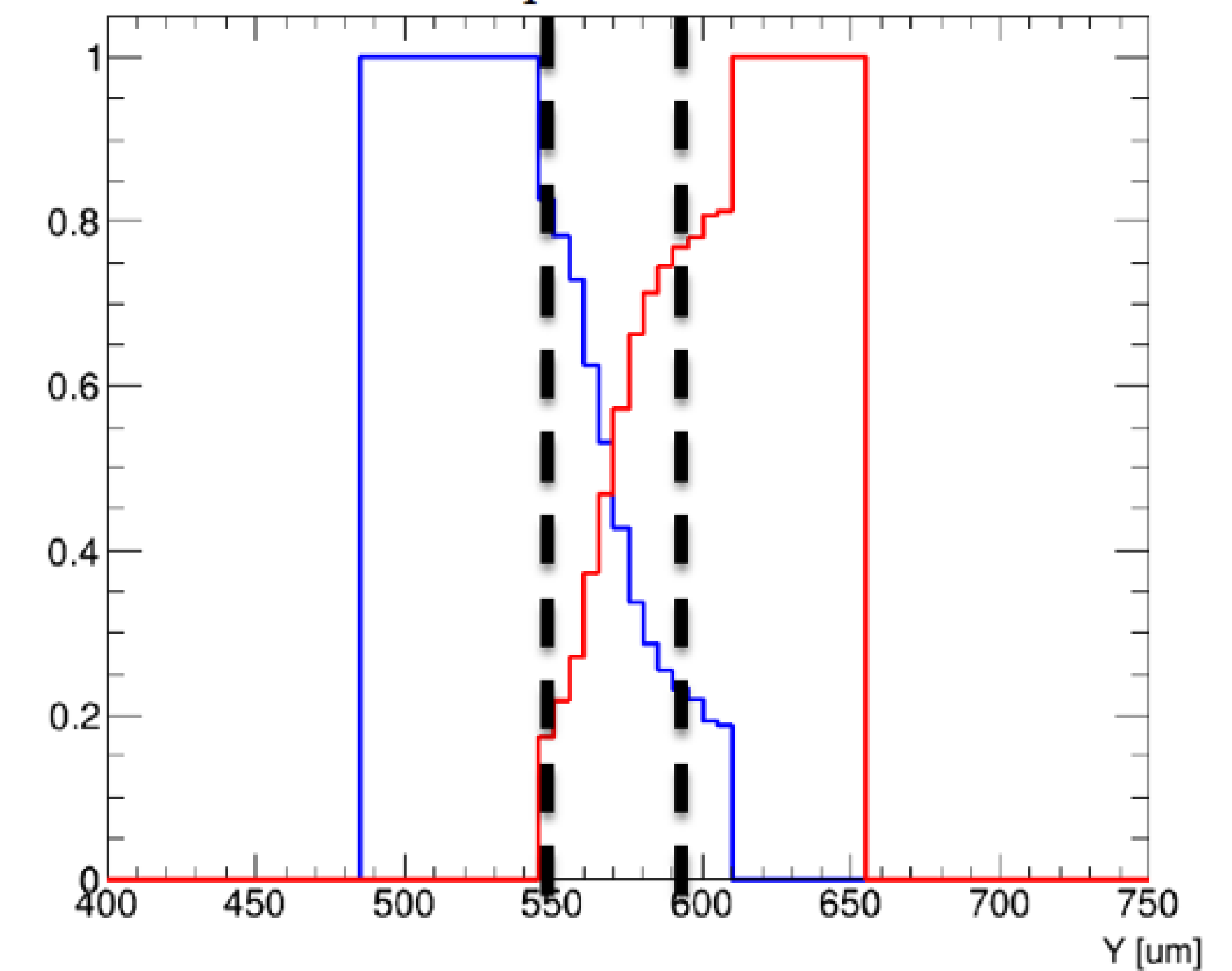
Normalized profile for Pad 1 and 2



Normalized sum of Pad 1 and 2



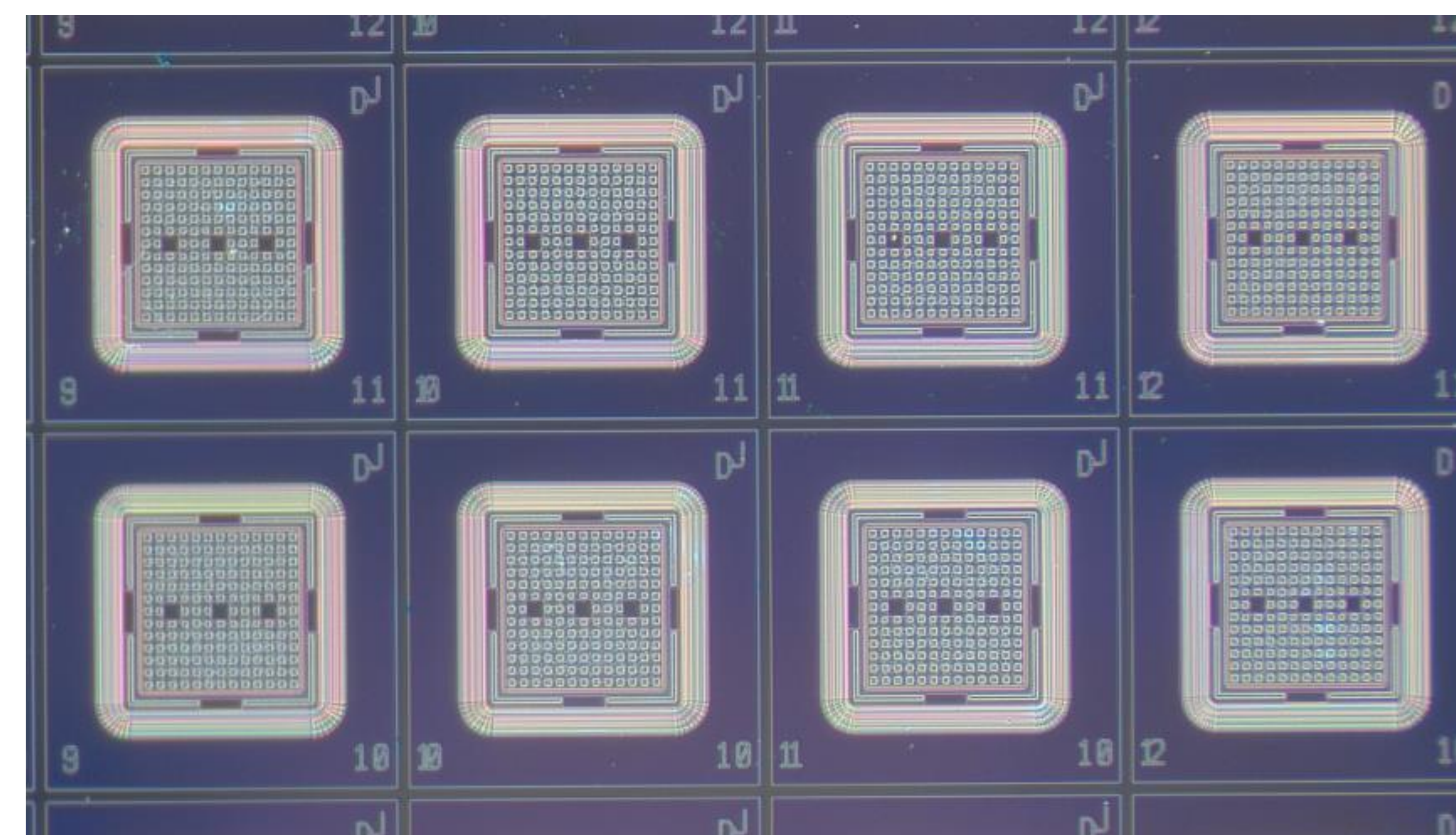
Fractional Pmax profile between Pad 1 and 2



Electrode gap (30um)

Conclusions

- DJ-LGAD: a device with deep gain layer
  - Avoid high field near the electrodes while maintaining gain
- Demonstrated that the deep-junction can be fabricated with epitaxial growth and w2w wafer bonding
  - Shows very good signal/charge uniformity across the channels
  - Almost no IP-gap is present between pads, small cross talk
- Future production will address
  - Very large leakage current -> reduce the current to level of conventional LGADs
  - The gain is lower than conventional LGADs -> optimize the doping
- This transformational technology can be used for many types of devices
  - Cactus's Materials Inc. wafer bonding capability can be extended to other absorber High-Z materials (III-V materials; GaSb, GaAs, InP)



THANK YOU

Cactus Materials, Inc.

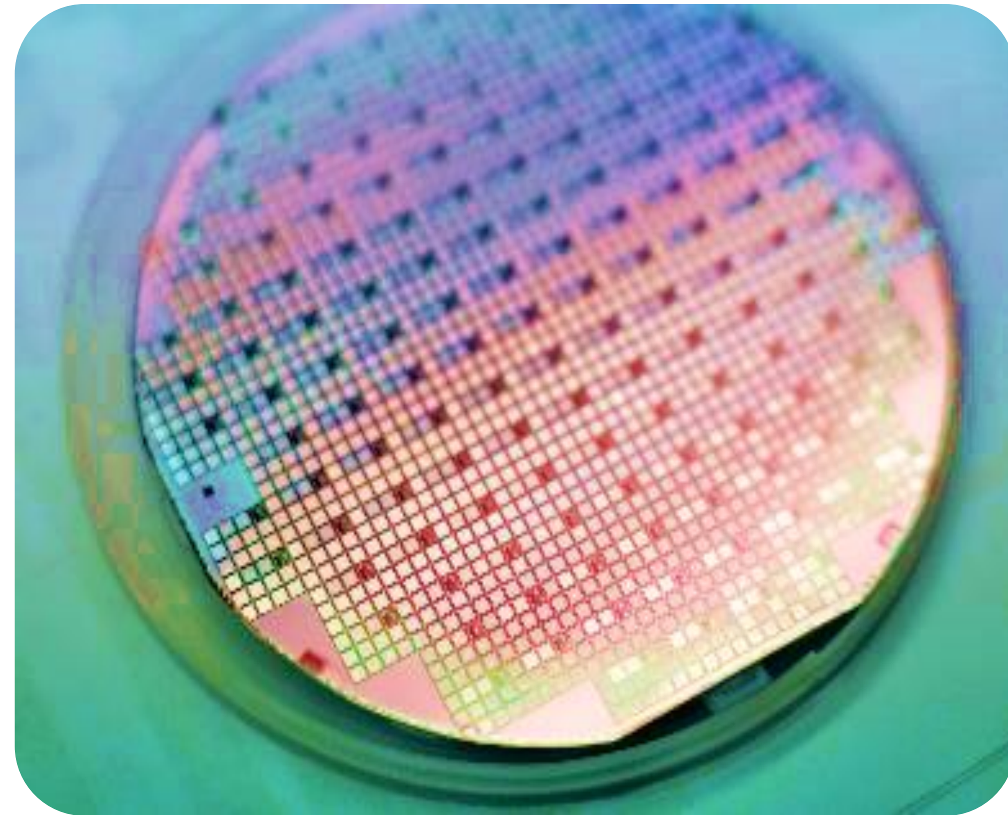
www.cactusmaterials.com

Rafi Islam. CEO

480-213-4704

Rafiqul.Islam@cactusmaterials.com

Power: SiC Products Roadmap and Key Milestone



Core SiC products & PDK
Planar 1.2kV, 1.7kV, 3.3 kV
JFET, and MOSFET

3D Integrated high density Packaging

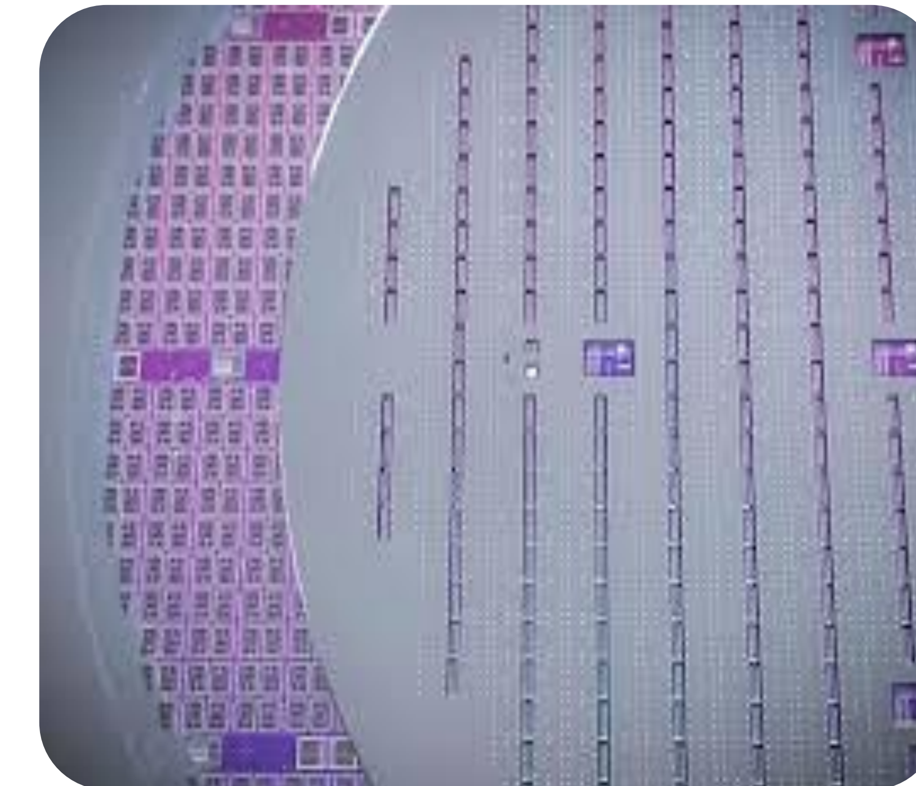
***R&D:** Extreme Environment*
High voltage and high temperature

HV HOT SiC Products
3.3kV, 10kV +
MOSFET – IGBT
Optical Detector
Key Technologies:

- Thick epitaxy > 60 um
- Trench Design/Processing
- Gold Ohmic Contacts
- Low RDSon
- Detector – RAD Hard
- High Temp > 500C

AI Power Semiconductor
High volume 1.2kV/1.7kV
Product delivery to AI & Automotive suppliers

SiC SMART-AI
Wafer to Wafer Integration
SMART Power Devices - AI
CMOS



Industrial and mobility
High volume 3.3 kV product delivery to Trains, Solar Inverters and others

Evolving Technology

HV HOT SiC Products
15kV – 20KV
MOSFET – IGBT Product delivery to Electric Trains, Wind Converters and power grids

2024 | 2025 | 2026 | 2027

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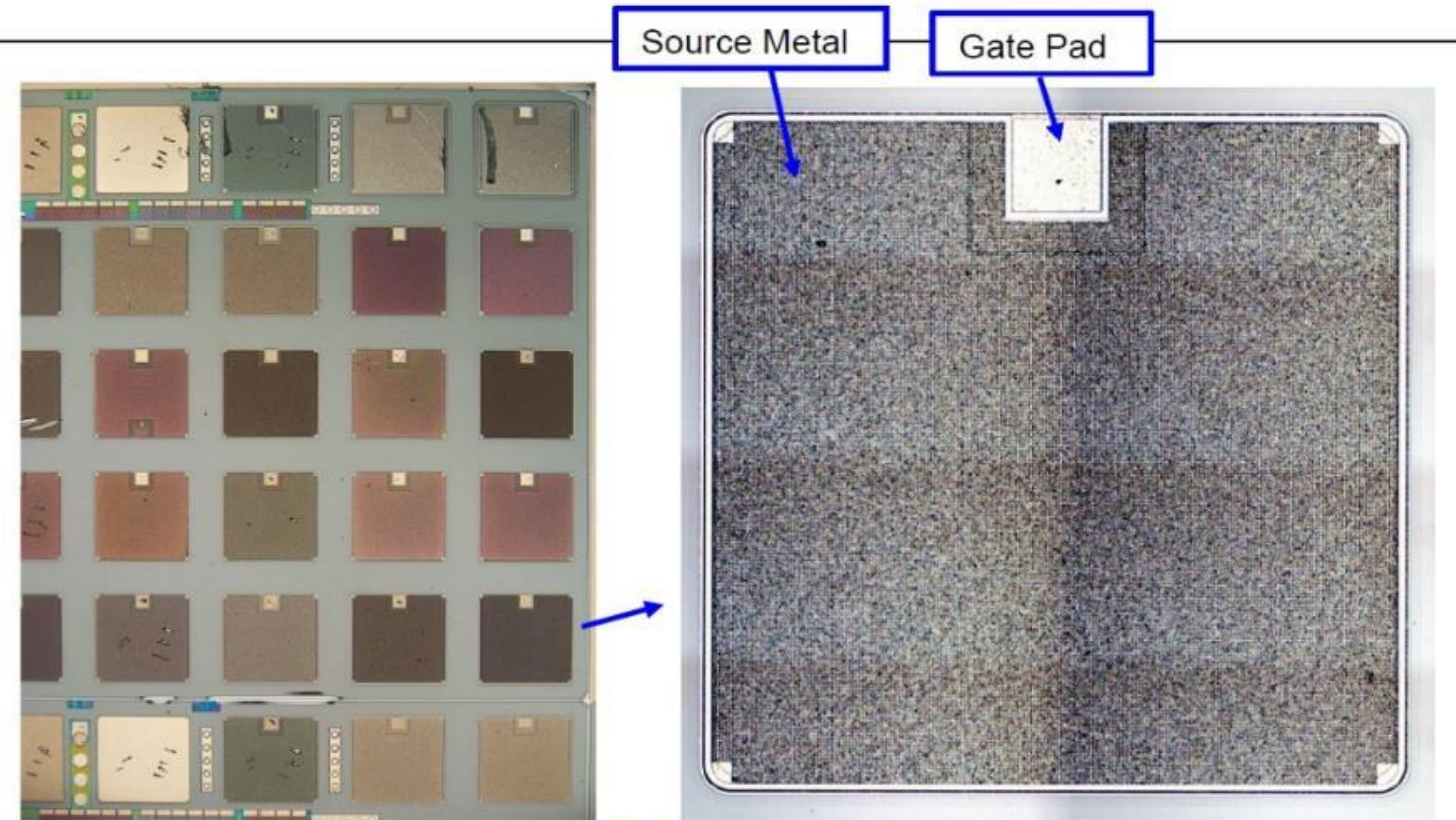
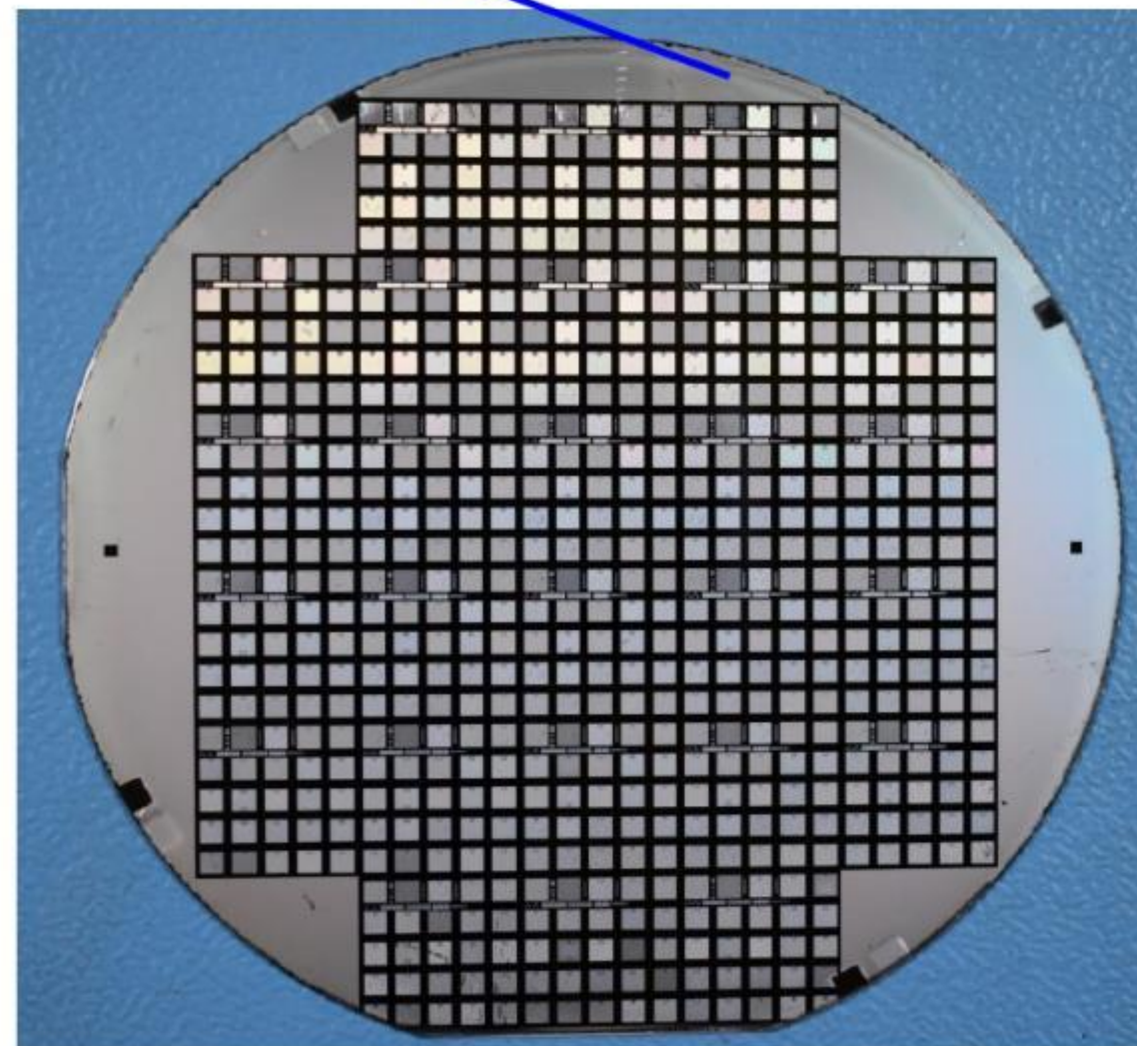
3.3KV MOSFET we have Fabricated

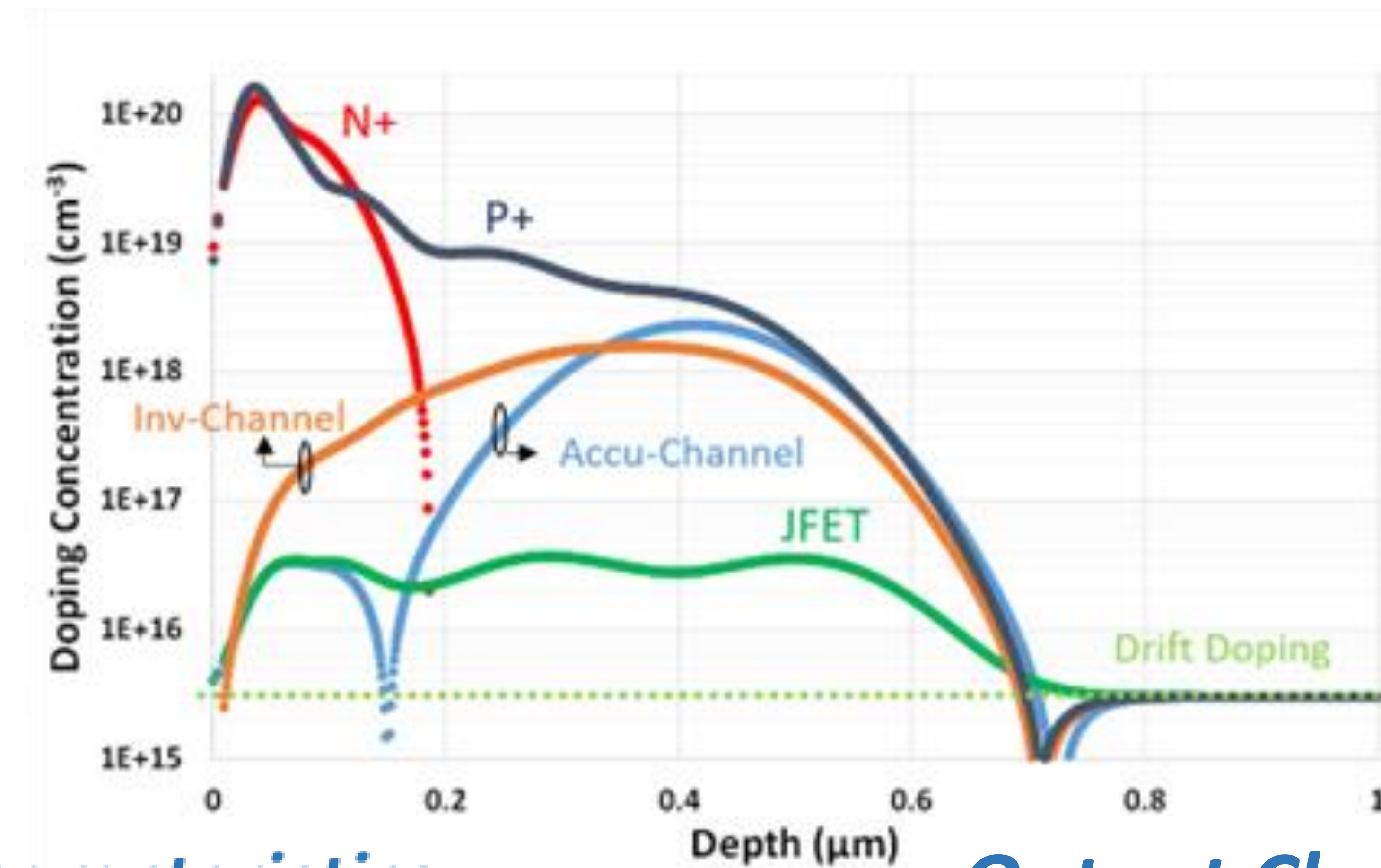
Pictures of Dies after fabrication



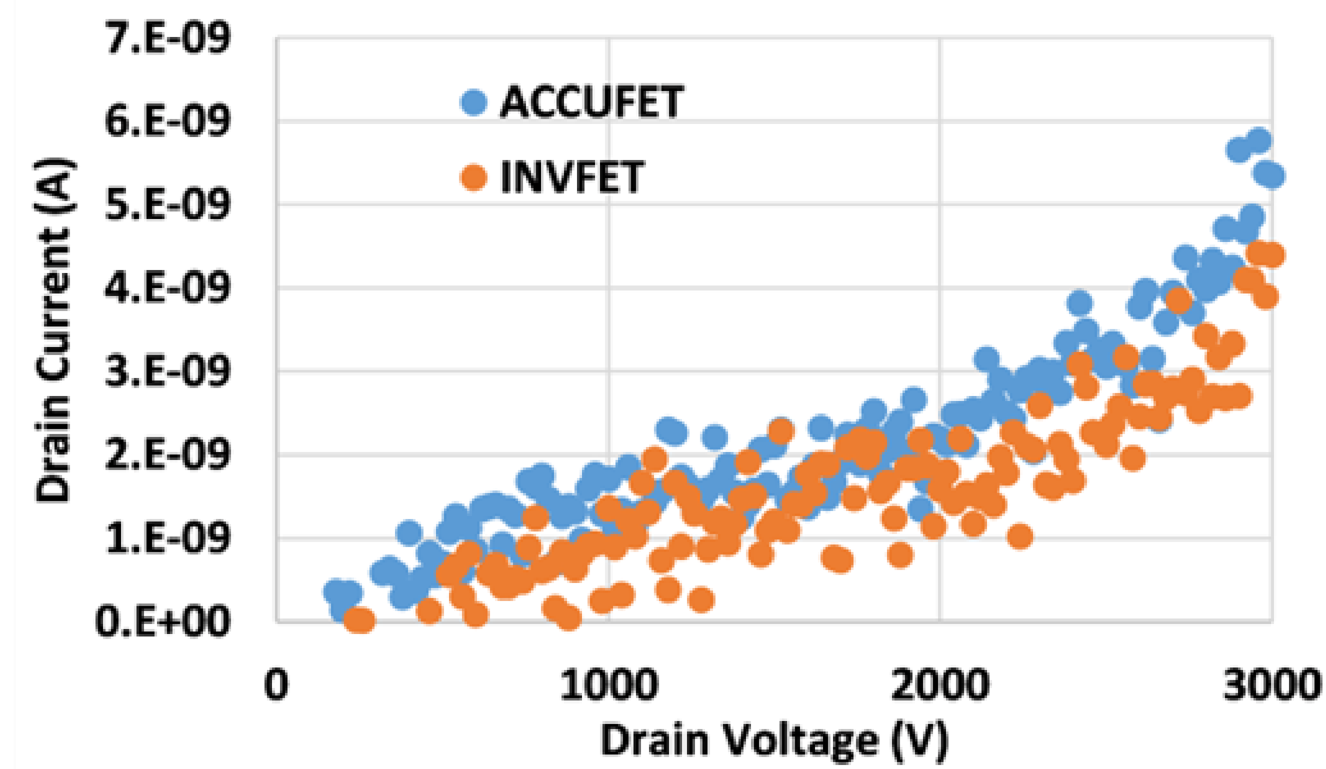


Wafer-level Measurements

<Doping Profile in vertical direction>

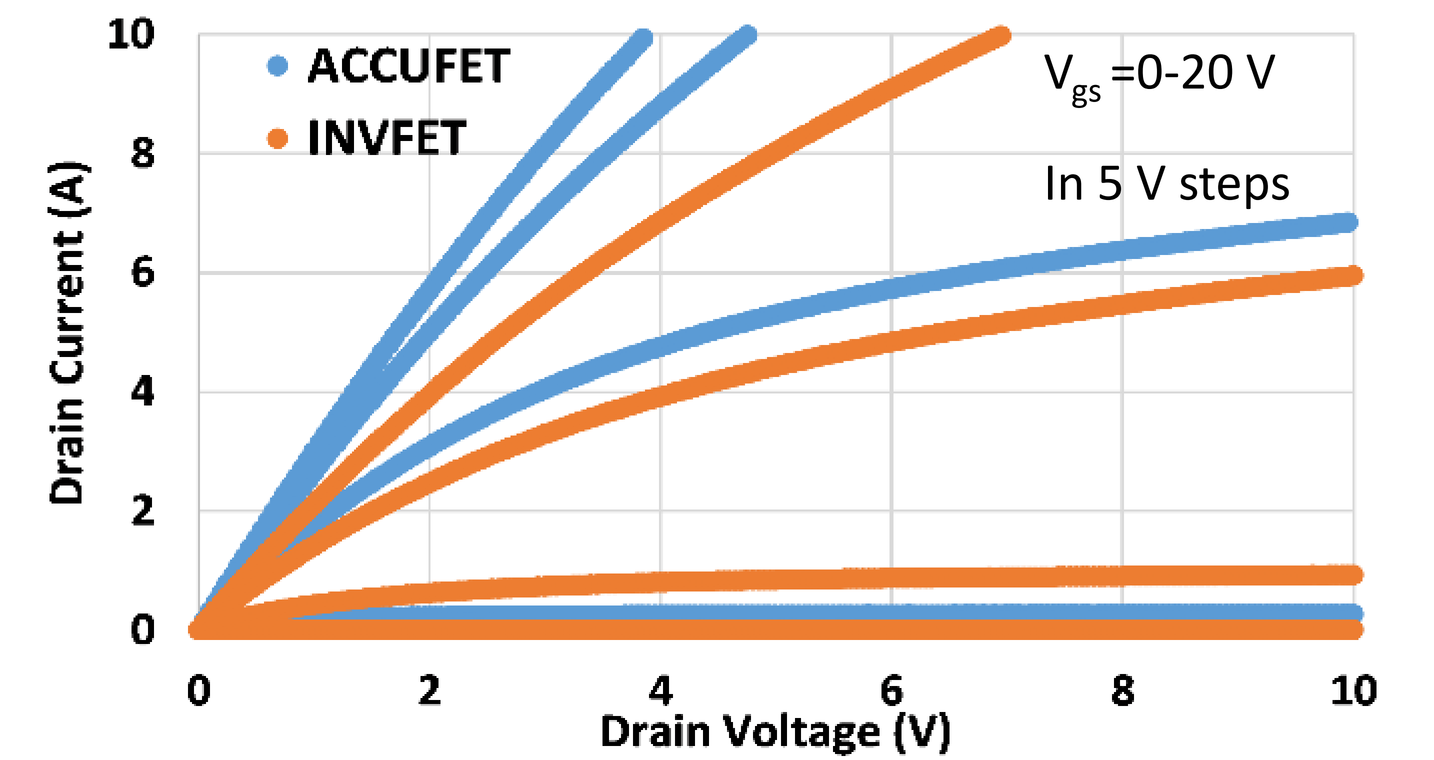


Blocking Characteristics



- Both MOSFETs have very low leakage current < 10 nA up to 3 kV.

Output Characteristics



ACCUFETs have better output characteristics and $R_{on,sp}$ compared to INVFET due to higher channel mobility and lower V_{th}.

1.2 KV SiC Diodes and MOSFETs