Nalu Scientific

Data Acquisition Systems

How to reduce costs and power usage in front-end electronics by implementing a system-on-chip approach for data acquisition.

Isar Mostafanezhad, Ph.D.

Founder and CEO, Nalu Scientific, LLC

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DOE Phase II SBIR Exchange Meeting

DE-SC0015231

Funded by DOE Office of NP

About Nalu Scientific

Nalu Scientific
Data Acquisition Systems

Mission statement:

Design house for DOE electronics needs with commercial grade support

Personnel:

6 engineers and experimental physicists

40+ years combined experience

Tools:

Commercial grade ASIC and electronic design tools

Funding:

DOE SBIRs and contracts

ASIC Design

- Mixed signal System-on-Chip
- Power optimization
- Full suite commercial grade Cadence license and server + design kits

Hardware Design

- FPGA, VHDL development
- Implementation
- Bring up and debugging
- Complex multi-layer boards

Expertise in:

- Fast time of flight measurements
- Readout electronics for HEP/NP

Mano Innovation Center

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2800 Woodlawn Dr. Ste #240
Honolulu, HI 96822
info@naluscientific.com
+1 (888) 717-6484

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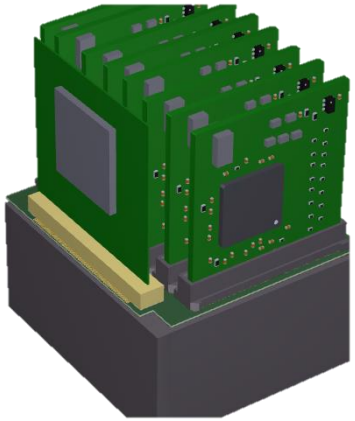
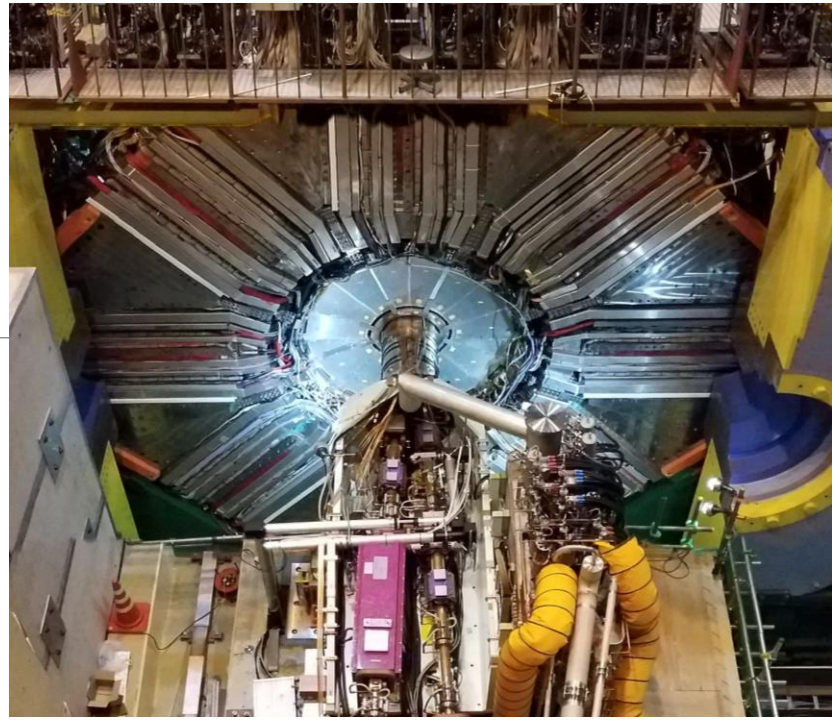
Waveform Digitizer SoCs for Single Photon Time of Fight Detection: Compact, Low Cost, Low Power





Main application: Particle collider experiments

1. Various Chips:
- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-10 Gsa/s, 12 bit res.
- Low SWaP
- Low cost
- User friendly

2. Integration:
- Detectors:
  - SiPM
  - PMT

3. Other applications:
- Low light detection
- Picosecond timing

Design and Fabrication of the ASoC:
A System-on-Chip Data Acquisition System

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Problem:

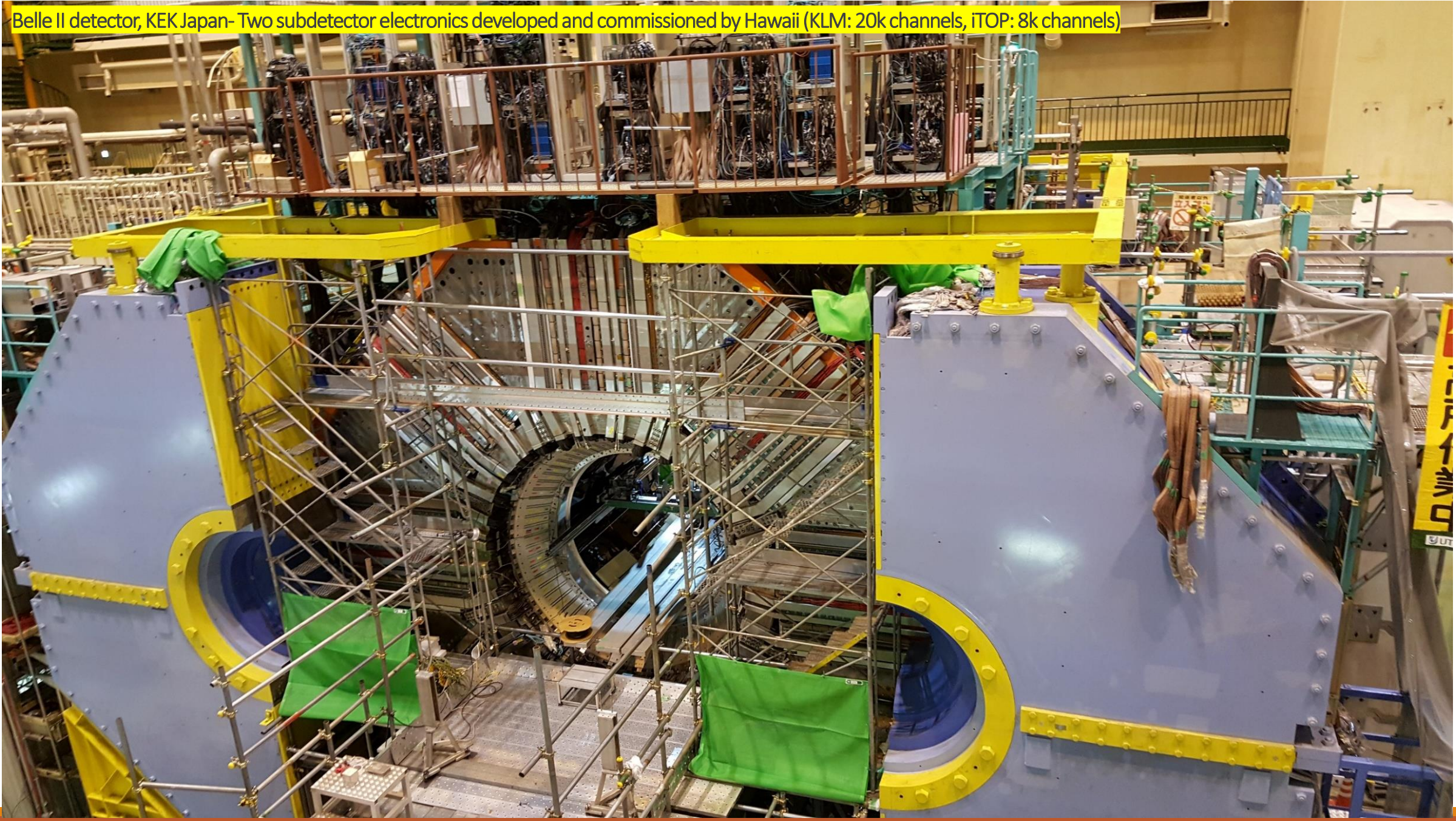
- We need new developments in instrumentation electronics with significantly improved energy, position, **timing resolution**, sensitivity, rate capability, stability, dynamic range, **durability**, **pulse-shape discrimination capability**, and **background suppression**.

Proposed Solution:

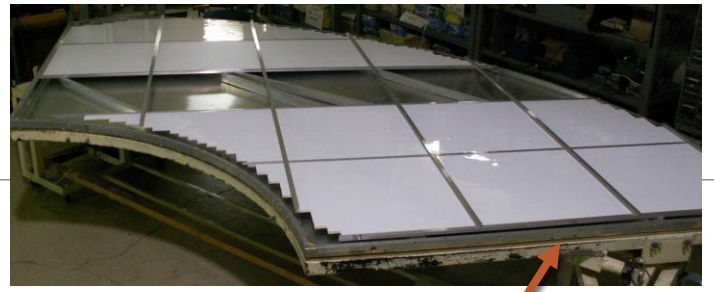
- Analog to digital converter System-on-Chip (ASoC)

Benefits:

- High integration
- Analog and digital processing on a single chip
- High resolution waveforms at low cost and low power
- Feature extraction and background suppression in the front-end


Belle II detector, KEK Japan- Two subdetector electronics developed and commissioned by Hawaii (KLM: 20k channels, iTOP: 8k channels)

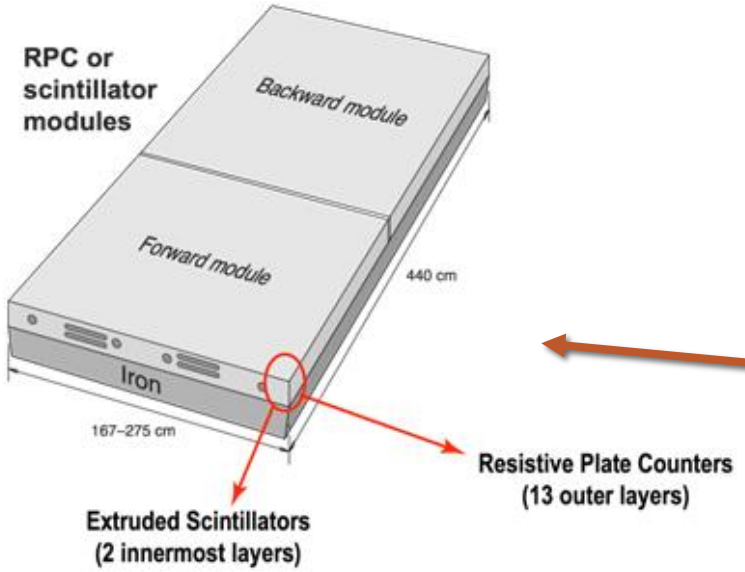
Belle II: KLM Scintillator Upgrade
20k+ channels at 1 GSa/s ea.

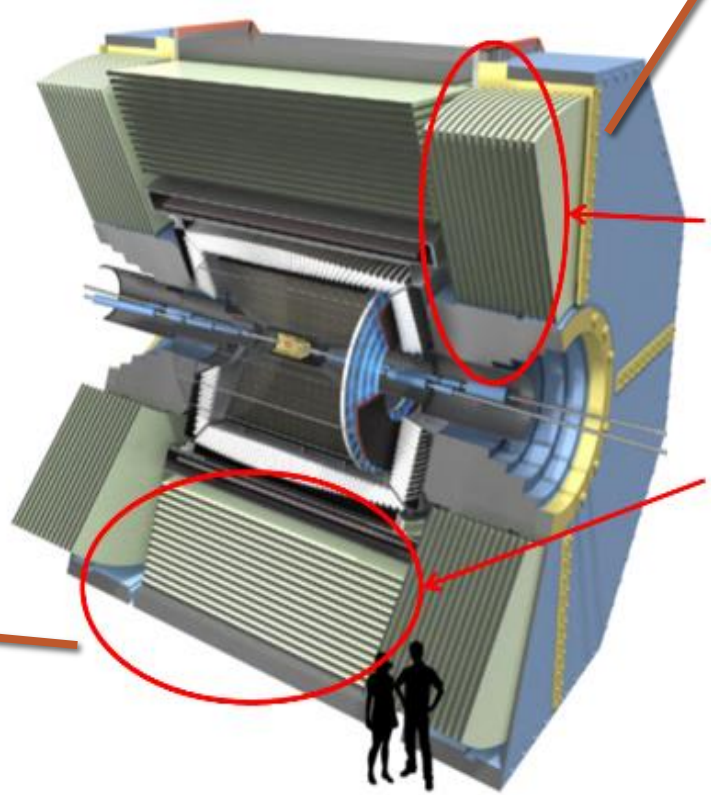


KLM detectors:

- Endcap: scintillators
- Barrel: scintillators +RPCs

Located outside the magnet





Lesson learned 1: Classical HEP/NP Experiment

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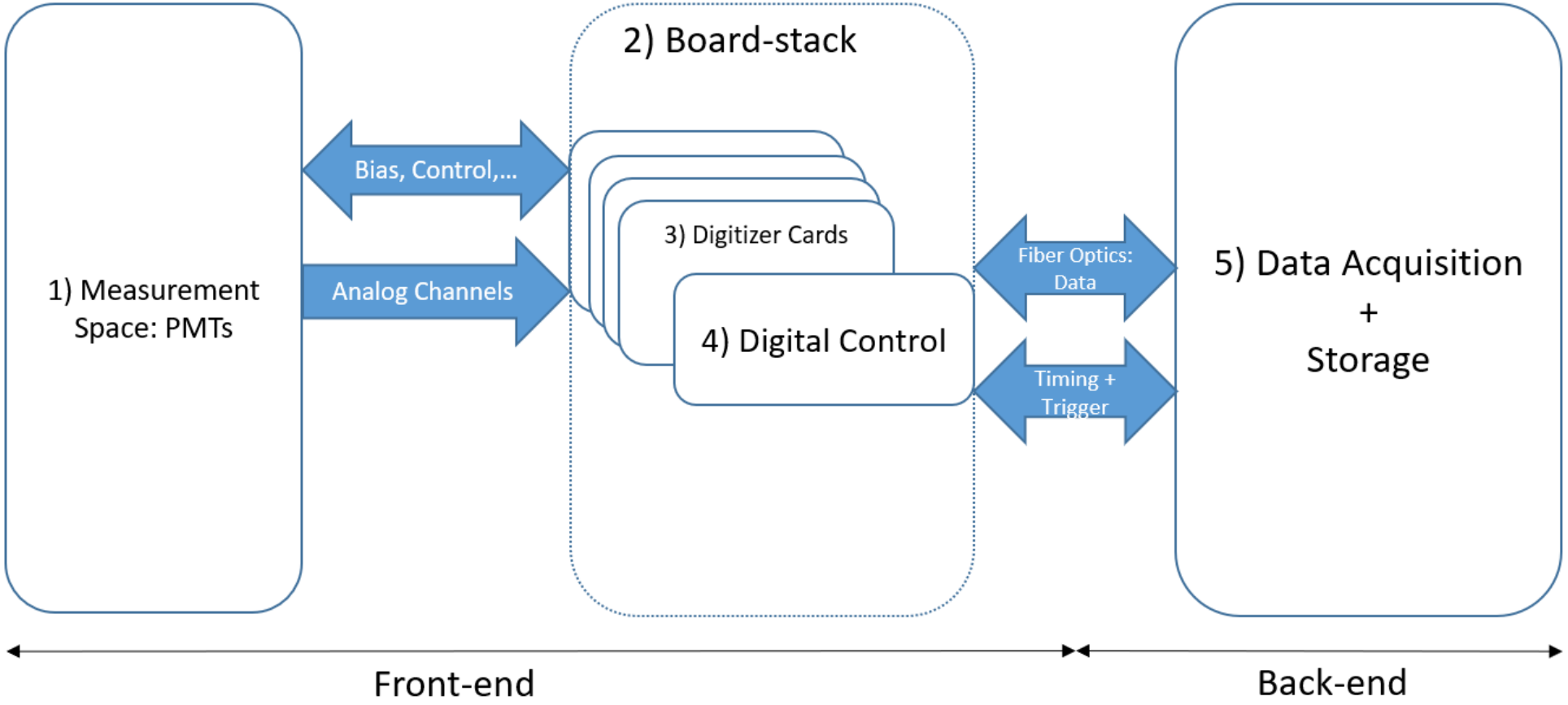

Lessons learned 2: Opportunities

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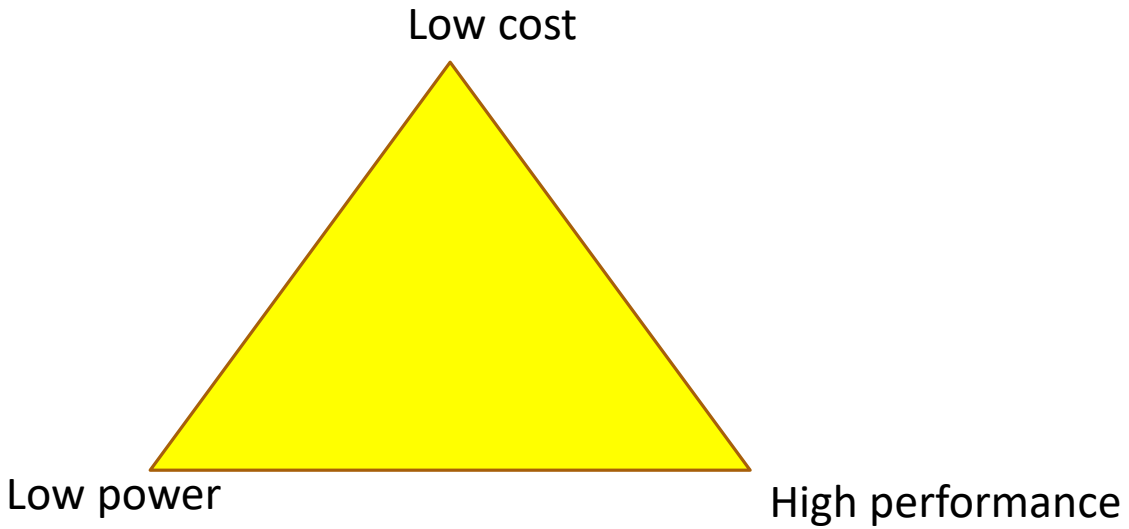
HEP/NP electronics need to be:

- Rad hard
- High performance
- Low cost
- Low power
- Highly integrated
- User friendly

Optimize to get to sweet spot = 2-3x gain

Solution: new design/SoC integration = 10 x gain



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Benefits of Higher Integration - SoC

- **Analog memory:**
  - Sampling always on (1-10 Gsa/s), but at low power
  - Digitize only Region of Interest (ROI)
  - Long analog buffer -> suitable for large experiments
- **Digital processing:**
  - Per channel cost reduction by a factor of 4
  - Relax thermal design by 40% reduction in power dissipation
  - Trigger time-stamping at the front-end
  - Eliminating the need for costly high-end FPGAs
  - User friendly: substantially reducing the FPGA firmware development labor
  - Reduced complexity and design and cabling effort/cost for the front-end boards

Analog/Mixed signal design

+

Digital/Synthesized logic

=

System-on-Chip (SoC)

SBIR Project: ASoC- System on Chip

Compact, high performance waveform sampling- Funded Phase II

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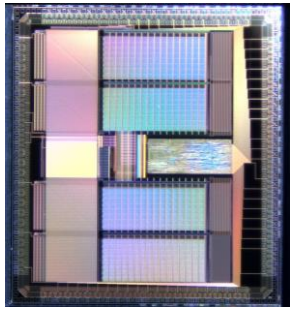

Fabricated ASoC Rev 1 die.

Spec	
Sampling rate	2-4 Gsa/s
ABW	0.9-1.5GHz
Depth	32k Sa
N channels:	8-32
Fab	250nm CMOS

Key Contribution:

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available
- 5mm x 5mm die size

Funded DOE Phase II Project

All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

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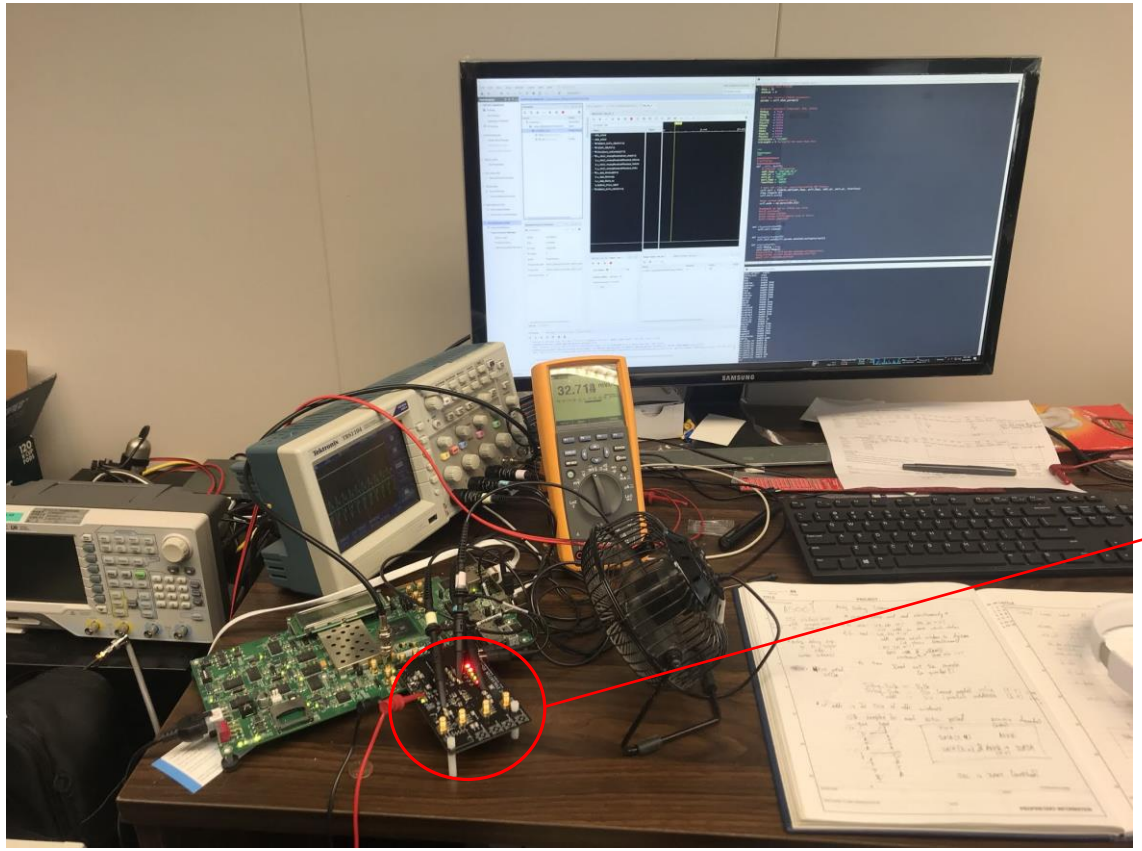
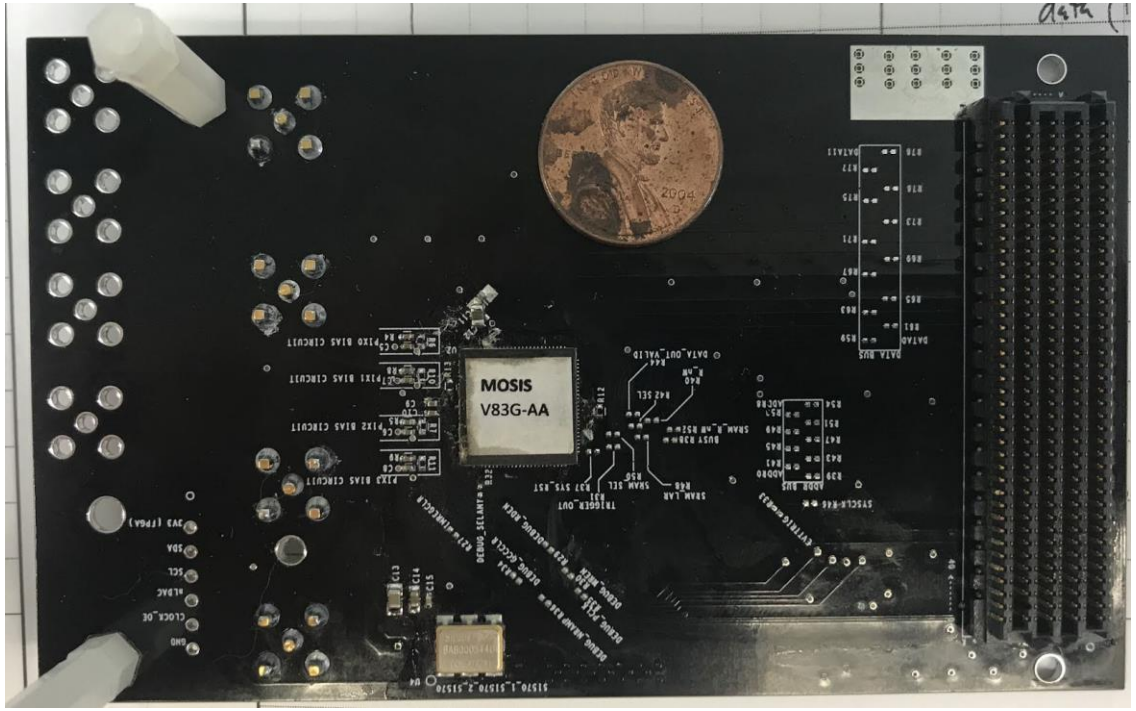
ASoC Under test!

Results to be published at conferences and journals in the next 2-3 months.





ASoC Evaluation FMC Card

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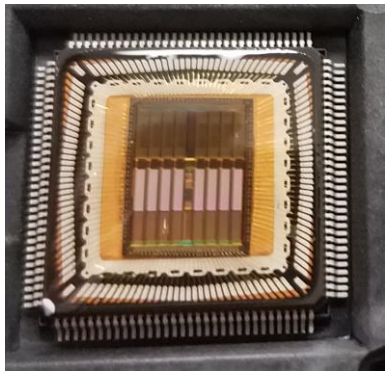
Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Integration	Built-in	Readout	Available Date
ASoC	3-5	0.8	32k	4-8	35	SoC	Pre amps	Parallel	Aug 2018
SiREAD	1-3	0.7	4k	64	80-120	SoC	Amp, bias	Fast serial	May 2018
AARDVARC	6-10	2.5	32k	4-8	4-8	SoC	Pre amps	Fast serial	Sep 2018

- **ASoC**: Analog to digital converter System-on-Chip
  - Rev 1 under test – **Eval card available**
- **SiREAD**: SiPM specialized readout chip with bias and control
  - Rev 1 under test
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
  - Rev 1 under test – Phase II



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Acknowledgements

- DOE Office of Science
- DOE SBIR/STTR Program
- DOE Office of NP
- From the team at Nalu Scientific: Thank you!