Telluric Labs LLC

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IP Access Gateway

The core of next generation software defined data acquisition systems

Presented to

DOE SBIR Phase II Meeting

By Michael Ivanciu and Codrut Radu Radulescu

Telluric Labs Team

- **Established**
  - **NJ LLC founded in August 2016 by Radu Radulescu and Michael Ivanciu**

- **Radu Radulescu**
  - **Vice President and technology lead**
  - **Thirteen years of entrepreneurial experience in the network timing synchronization**
  - **Over thirty-six years experience designing and manufacturing network equipment**
  - **Intellectual Property Attorney, and MEE in Telecommunications.**

- **Michael Ivanciu**
  - **President and business lead**
  - **Attorney practicing in New York and New Jersey**
  - **Major (Branched Military Intelligence) New York Army National Guard for 20 years**
  - **US Federal Trademarks at the USPTO**
  - **Contracts and Commercial Litigation**

Introduction

Telluric Labs Capabilities:

- **Special Data Networks – development and systems integration**
  - **Precision timing synchronization over commercial networks**
    - **Timing synchronization protocols**
    - **Time to Digital Converters (TDC)**
    - **Time sources – smart oscillator arrays**
    - **Data synchronization and consensus**
  - **Optical Networks,**
    - **Remote laser modulators**
    - **Multiplexing technologies**

- **Simulation of Detector and general Data Acquisition Networks**

Strategy: partnership with technology movers, grow intellectual property portfolio.

Phase II project: IP Access Gateway – the electronic gateway between detector network and SW defined DAQ

Relevance to the NP program: develop a reference platform for SW defined DAQ, enabling SW trigger, embedded timing synchronization, and seamless integration of data from multiple detectors.

Schedule and deliverables: 2020 – IPAG board and numeric timing synchronization

Future plans: Intelligent DAQ and transport networks, entangled photons, power over fiber, free space optics

Questions for the NP community

- **Interested in partnering and share expertise for new facilities**
- **Timing synchronization, trigger, and data readout requirements for future systems**
- **Other challenging constraints for future DAQ and timing synchronization**
- **Interest in remote laser modulation, PON, and massive bandwidth transport**

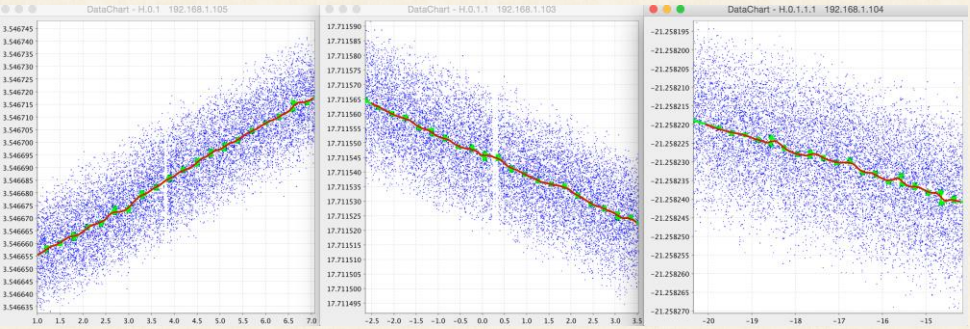
Problem / Solution

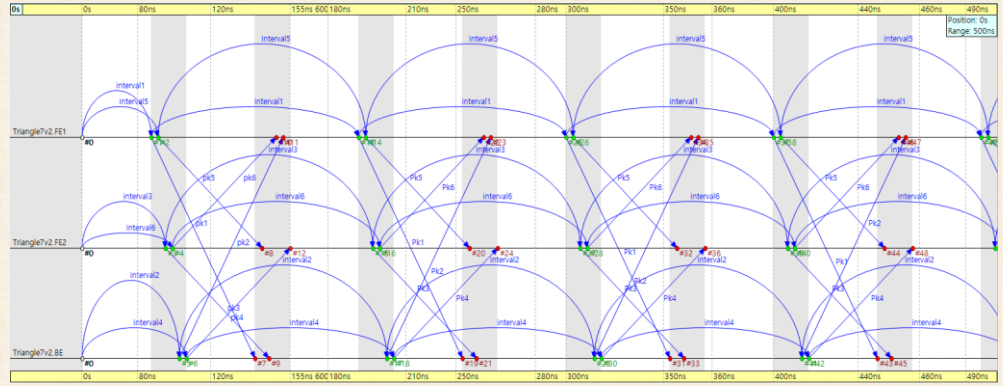
PROBLEM	IP ACCESS GATEWAY SOLUTION
Need for higher timing accuracy for data acquisition systems, covering longer distances	Full optical transport Numerical General Timing Synchronization over LAN Continuous acquisition, pS TDC
High bandwidth transport network for Nuclear Detectors readout data	Passive Optical Networks (PON) Remote laser modulators Concurrent optical multiplexing types
Lower costs	COTS HW: network, numerical timing, SW trigger, remote laser modulators
Highly scalable systems	Commercial LAN, standard interfaces, SW trigger, numerical timing
Reduce the volume, mass, complexity, and power of front-end electronics	Move functionality to backend, continuous readout, massive bandwidth network
Fast computer interconnectivity	Fast embedded switching

IP Access Gateway
Product Highlights

- **PCIe gen 4.0 COTS, FPGA NIC, modular board assembly;**
- **10E2 TDCs with pS timing accuracy, and continuous acquisition;**
- **1.5 Tbps aggregated LAN Bandwidth over more than 60 optic ports;**
- **In band General Timing Synchronization (“GTS”) for the entire facility: Frontend, Backend, Trigger, DAQ, and accelerator;**
- **Functionality implemented in the latest generation FPGA ;**
- **Provides both Synchronous and Asynchronous, standard and proprietary Interfaces (Ex: Ethernet / LpGBT) for linking to existing, and future frontend electronics;**
- **Configurable as a stand alone NIC for HPC and other commercial applications.**

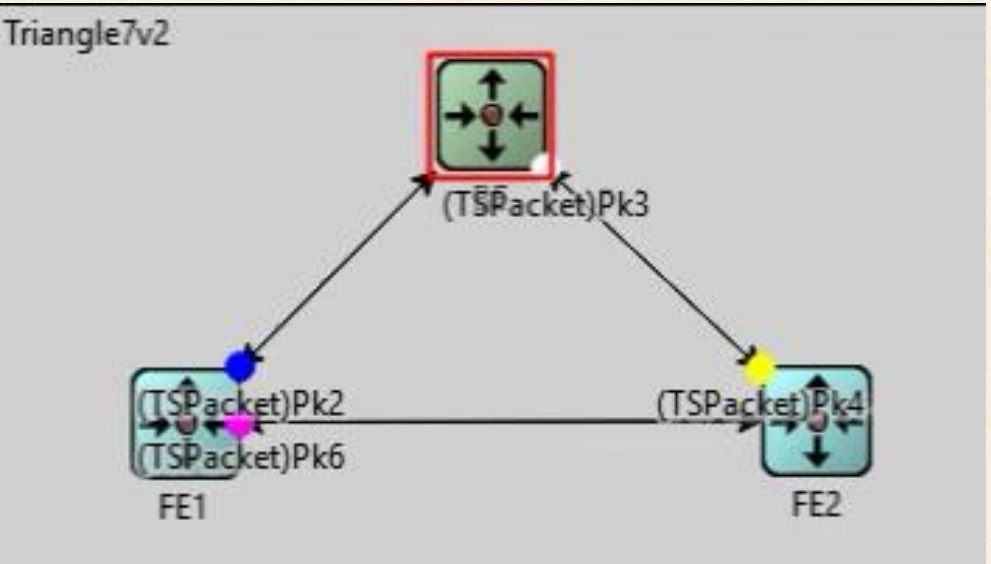
Readout Network and Timing Synchronization Simulator

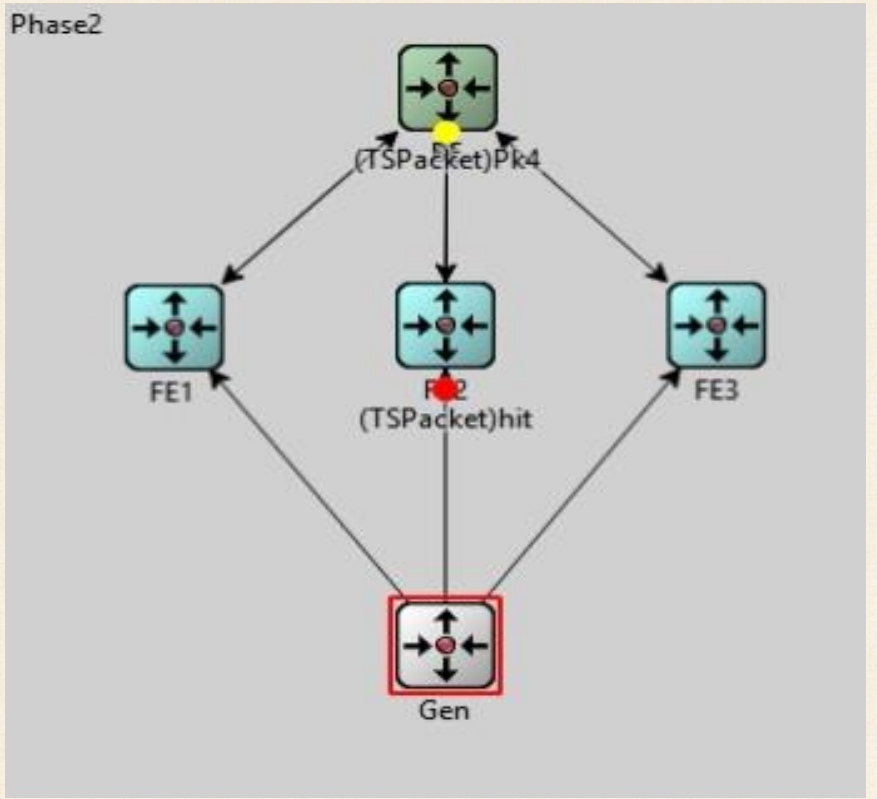




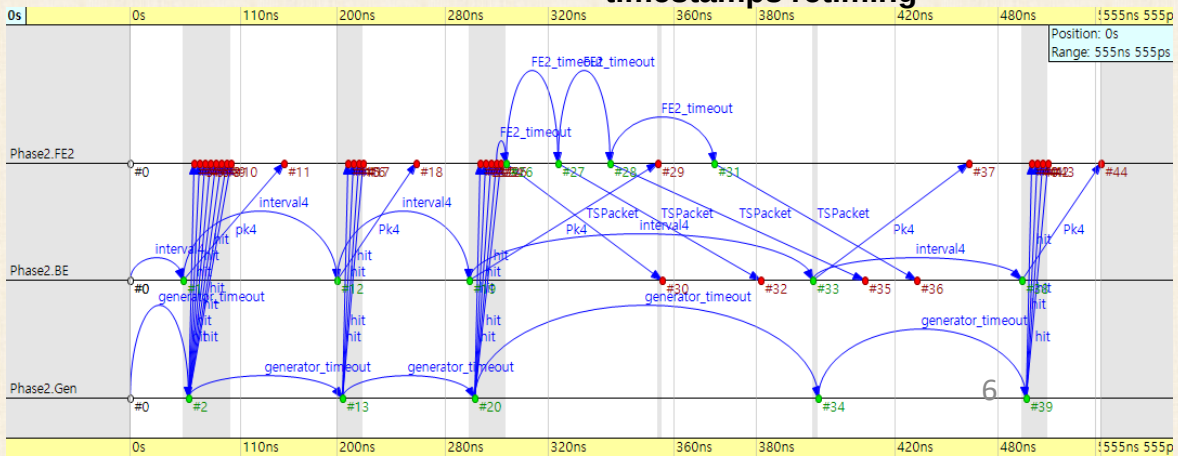
Closed loop network path - validation of GTS performance

Simulation validates the performance of our algorithms
Allows evaluation of the technology for specific customers systems
Evaluates independent timing sources and patterns of perturbation of the local free running clocks.
Unique self calibration capabilities of GTS running over ring topology (not possible for HW synchronization)





Time simulation from beam crossing to backend timestamps retiming



FPGA CODE

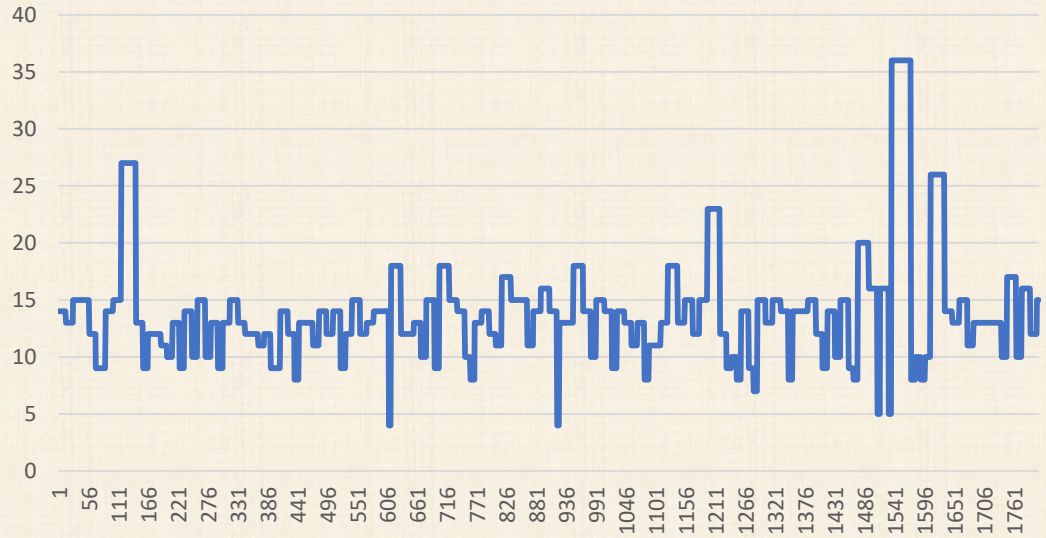
Time to Digital Converter (TDC)
Implementation with commercial programmable logic

Identified mutual interest and collaborated with FPGA manufacturer to leverage unexplored capabilities of the device. Partial implementation achieves pS performance

Automatic self configuration, calibration, optimization, through intelligent numerical algorithms.

Inherent high resilience of Single Event Upset, and jitter tolerance.

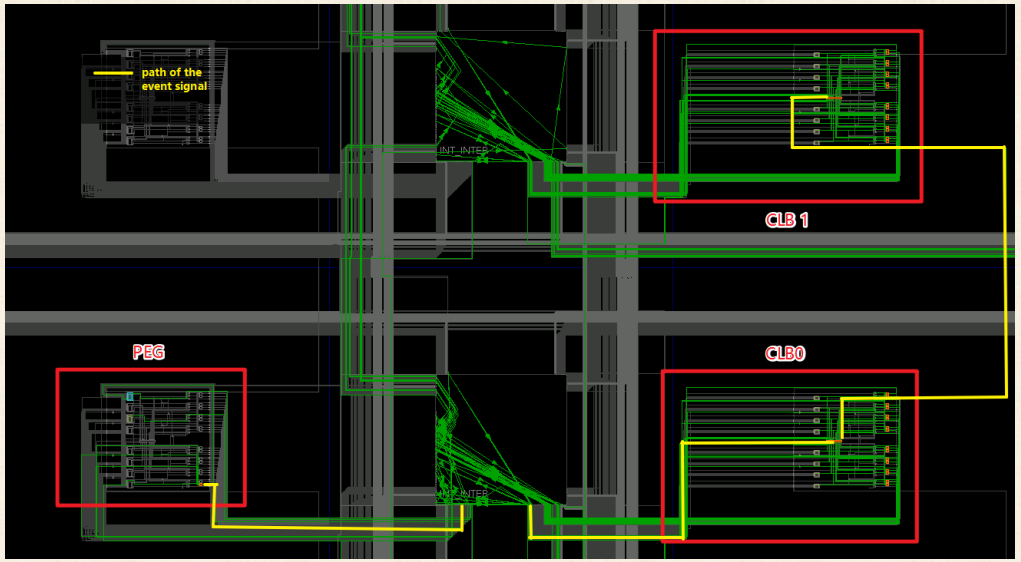
Simulation of final numerical processing shows fS accuracy.



SW defined TDC. Delay taps (vertical unit <0.5 pS), RMS < 8pS
First data collected on the boards - work in progress.

MIXED ETHERNET AND DETECTOR SERIAL TRANSPORT CONFIGURABLE INTERFACES

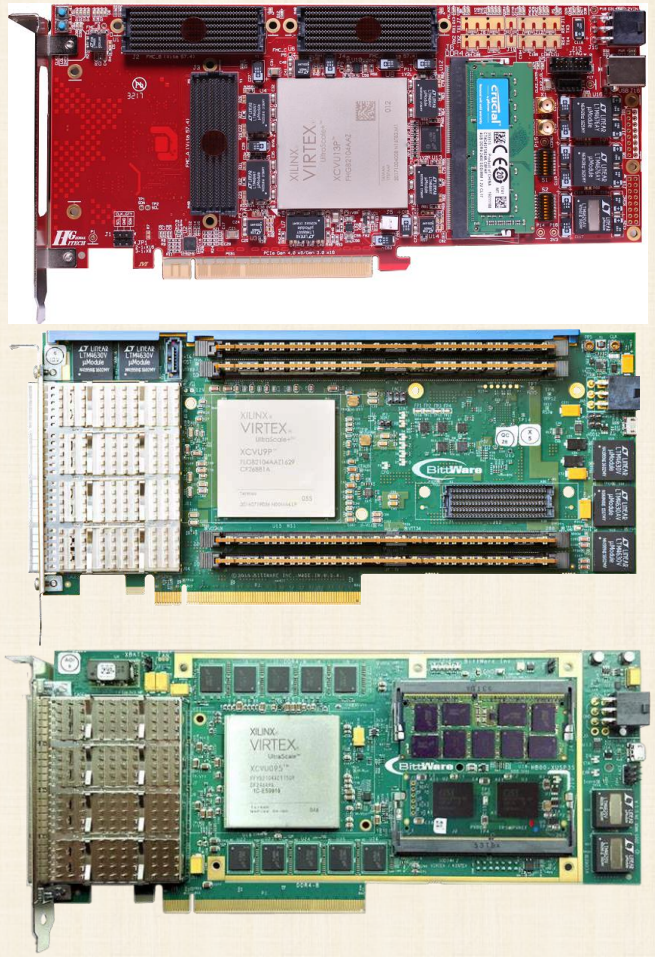
Supports concurrently the Detector digital connectivity and Ethernet ports in proportion tailored for each application.



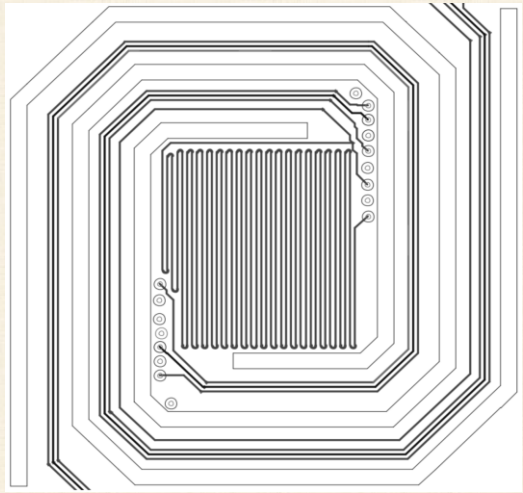
FPGA architecture provides the flexibility necessary for a software defined functionality

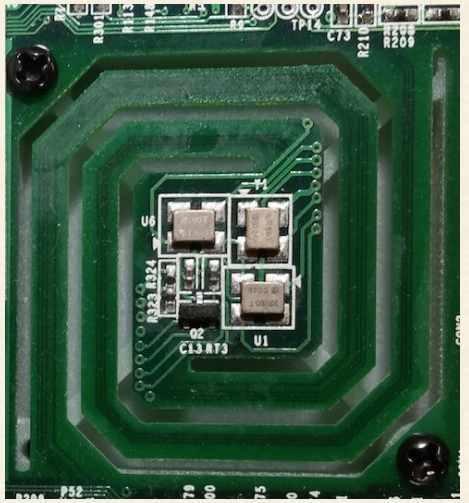
IP Access Gateway Hardware

MIGRATION FROM COTS NIC FPGA BOARDS TO HIGHER BANDWIDTH IPAG BOARD

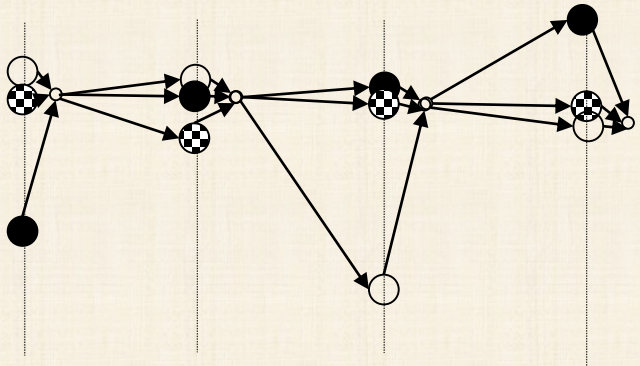


REDUNDANT FREE RUNNING TIME REFERENCE





Ideal for radiation environment. Free running oscillators have low jitter and higher short term stability. Lower speed of temperature variations by design.



Numerical Clock – Virtually determined by algorithms monitoring the free running oscillators

Full Optical Transport

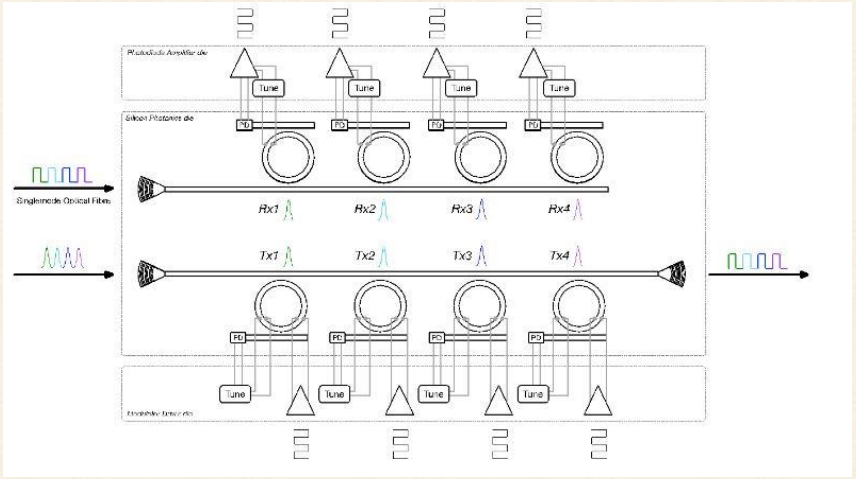
Strategy :

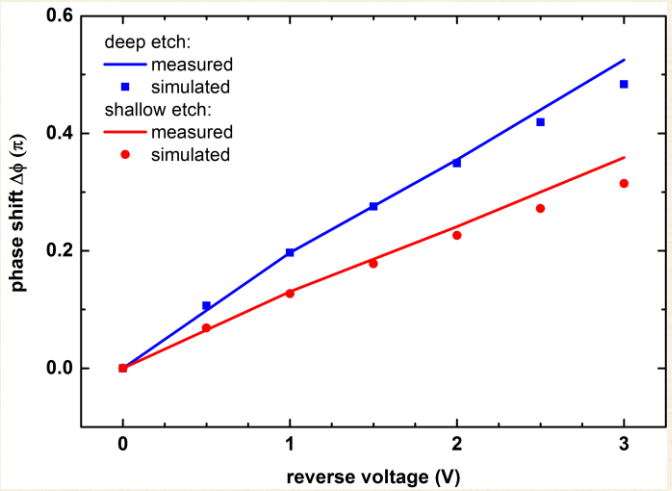
- **Collaboration with developers of low power, inherently rad hard silicon photonics modulators**
- **Remote laser illumination**
- **Concurrent types of multiplexing**

Benefits of massive optical bandwidth:

- **Simplifies Frontend electronics**
- **Reduces heat dissipation on detector**
- **Reduces interference from the mass and volume of Cu cables and electronics**
- **Eliminates HW trigger for many detectors**
- **Lower costs – use of COTS HW for backend**

Available modulator technologies with low power and voltage.
Currently under evaluation





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