12-bit 32 Channel 500MSps Low Latency ADC

Award Number: DE-SC0017213

Summary of year 1 progress, Ph II project

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Presentation Outline

Pacific MicroCHIP Corp.

- The Company, its Specialization/Expertise
- A List of Successful Projects
- Used IC Fabrication Technologies
- Current Project - 12-bit 32 Channel 500MSps Low Latency ADC:
  - Relevance to the NP Program
  - Project Goals
  - Chip Description
  - Project Schedules and Milestones
- Plans for the Future

The Company

- **Pacific MicroCHIP Corp. was incorporated in 2006.**
- **It is headquartered in Culver City, California.**
- **Main focus of the company – providing IC/ASIC design services and turnkey solutions.**

Office in Culver City, CA

Our Offerings

Pacific MicroCHIP Corp.

IC/ASIC Design Services:

- **Circuit Design (analog, RF/mixed, digital)**
- **Simulation**
- **Physical Design**
- **Chip Assembly**

Turnkey Solutions:

- **IC Design**
- **Chip Fabrication Logistics**
- **Package Development (involving a 3rd party)**
- **Chip Packaging (involving a 3rd party)**
- **PCB Development for Testing/Eval. (involving a 3rd party)**
- **Testing/Characterization (an in-house lab)**
- **Delivery of Chips, Parts and Board Level Solutions**

Core Expertise

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- **Analog (ADC/DAC, CTF, VGA, BG, LDO)**
- **Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)**
- **RF (LNA, Mixer/Modulator, PA)**
- **Digital (Verilog, RTL, P&R, Timing Closure, DFT, Verifications)**
- **Layout (SiGe/CMOS) down to 7nm**

A List of Successful Projects

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- 12-bit 32 Channel 500MSps Low Latency ADC ← Being presented.
- A spectrometer ASIC 4GHz BW, 6-bit@8GSps, 8K frequency bins.
- A correlation radiometer ASIC 2xI/Q inputs, 2-bit@20GSps, cross-correlation within 16 bands.
- 20GS/s 6-bit ADC ASIC.
- An 8-bit up to 56GS/s ADC.
- A fiber-optic TRx ASIC for 200Gbps. Includes 4xADC/DAC (8-bit@56GSps).
- An 8-bit up to 64GS/s DAC for fiber optic >400Gb/s Tx.
- A laser controller ASIC for 100-400Gbps fiber optic modules. Includes 12-14-bit DACs, ADCs, TIAs, PIDs, PWM, etc.
- A low power RF TRx ASIC for medical pill endoscopes. Tx 433.8MHz (1mA), Rx 13.56MHz (2mA).
- A low Power Rx front end (TIA) for up to 4x28Gb/s NRZ realized in 130nm SiGe.
- A low power up to 4x32Gb/s NRZ MZ modulator driver realized in 180nm SiGe.
- A low power up to 2x56Gb/s PAM4 MZ modulator driver realized? in 180nm SiGe.
- A cross-correlator ASIC including 128 2-bit 1GSps ADCs and a 64x64 cross-correlator matrix.
- A dual transceiver ASIC with eFEC/FEC (5M gates) for 8.5Gb/s to 11.3Gb/s fiber optic networks.
- An EDC receiver with an analog Viterbi for fiber optic networks from 8Gb/s up to 11.3Gb/s.
- A UWB transceiver in 180nm SiGe.

IC Technologies Used – down to 7nm node

★- indicates previously used node

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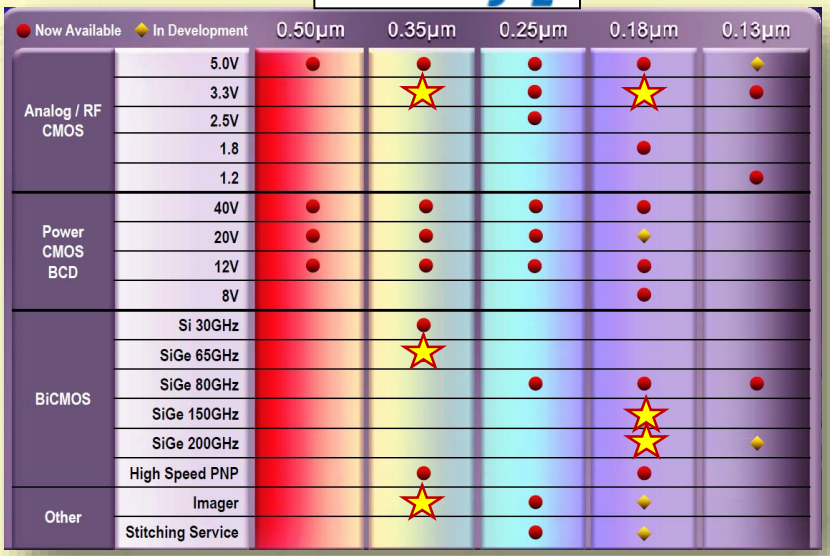

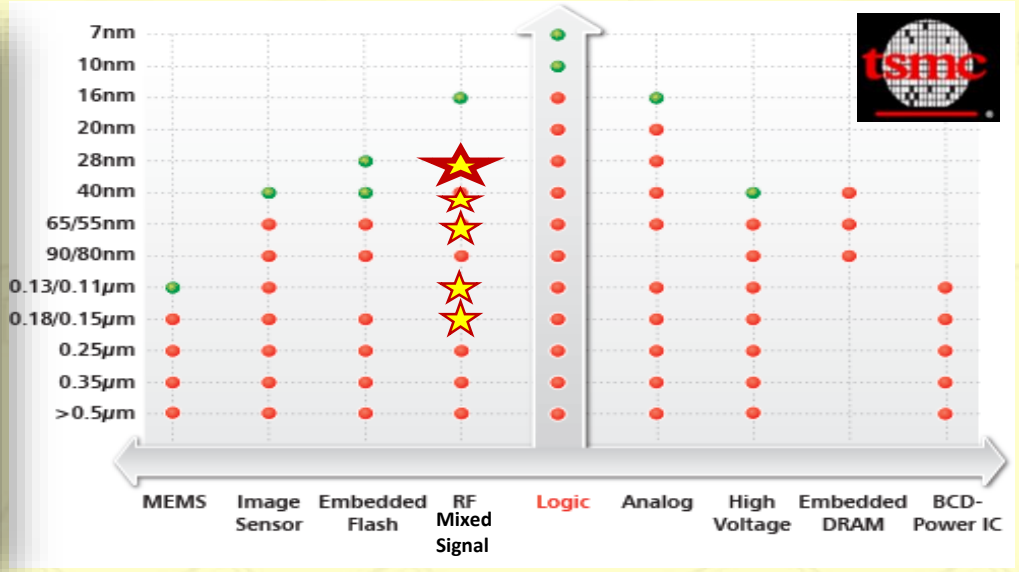

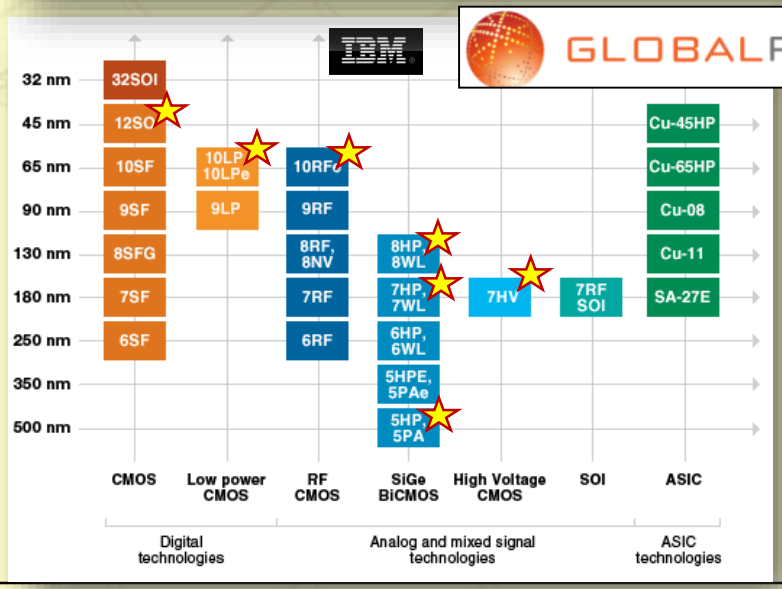

Relevance to the NP Program

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NP detectors require thousands of signal processing channels => need for digitizers to:

- **Shrink in size - our ASIC combines independent 32 ADCs per chip.**
- **Reduce power consumption - we offer 25mW per ADC.**

Upgrades in these systems demand for:

- **Digitizing accuracy - our ADC features 12-bit resolution.**
- **Adequate sampling speed - our ADC features 0.5GS/s.**
- **Low conversion latency - we offer 8ns.**

Targeted specific applications:

- **Low latency particle beams control systems.**
- **Imaging and spectroscopy systems for gamma-ray detectors.**
- **Multichannel detectors based on tube and silicon photo multipliers.**

Project Goals for Phase II

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Within this project we will:

- **Design circuits and layout for the ADC ASIC.**
- **Fabricate the chip.**
- **Develop a special chip carrier.**
- **Package the chips.**
- **Develop a test PCB and a DUT socket.**
- **Develop a GUI and a test bench.**
- **Test and characterize the ADC ASIC.**
- **Prepare a datasheet for marketing.**
- **Submit deliverables to the DoE.**

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Specifications Include:

- 32 independently operated ADC channels
- 500 MS/s sampling rate
- 0.6Vpp differential input swing
- 10-bit ENOB
- 250MHz Input signal bandwidth
- -40C..+125C temperature range
- 25mW/channel power consumption (with interface)
- JESD204B output data interface
- 8ns latency (direct ADC data output mode)
- 32x8Gb/s output data rate
- I2C interface for ASIC control
- 8.7mm^2 estimated ASIC layout footprint
- Solder bumped die in a BGA package
- 28nm CMOS technology

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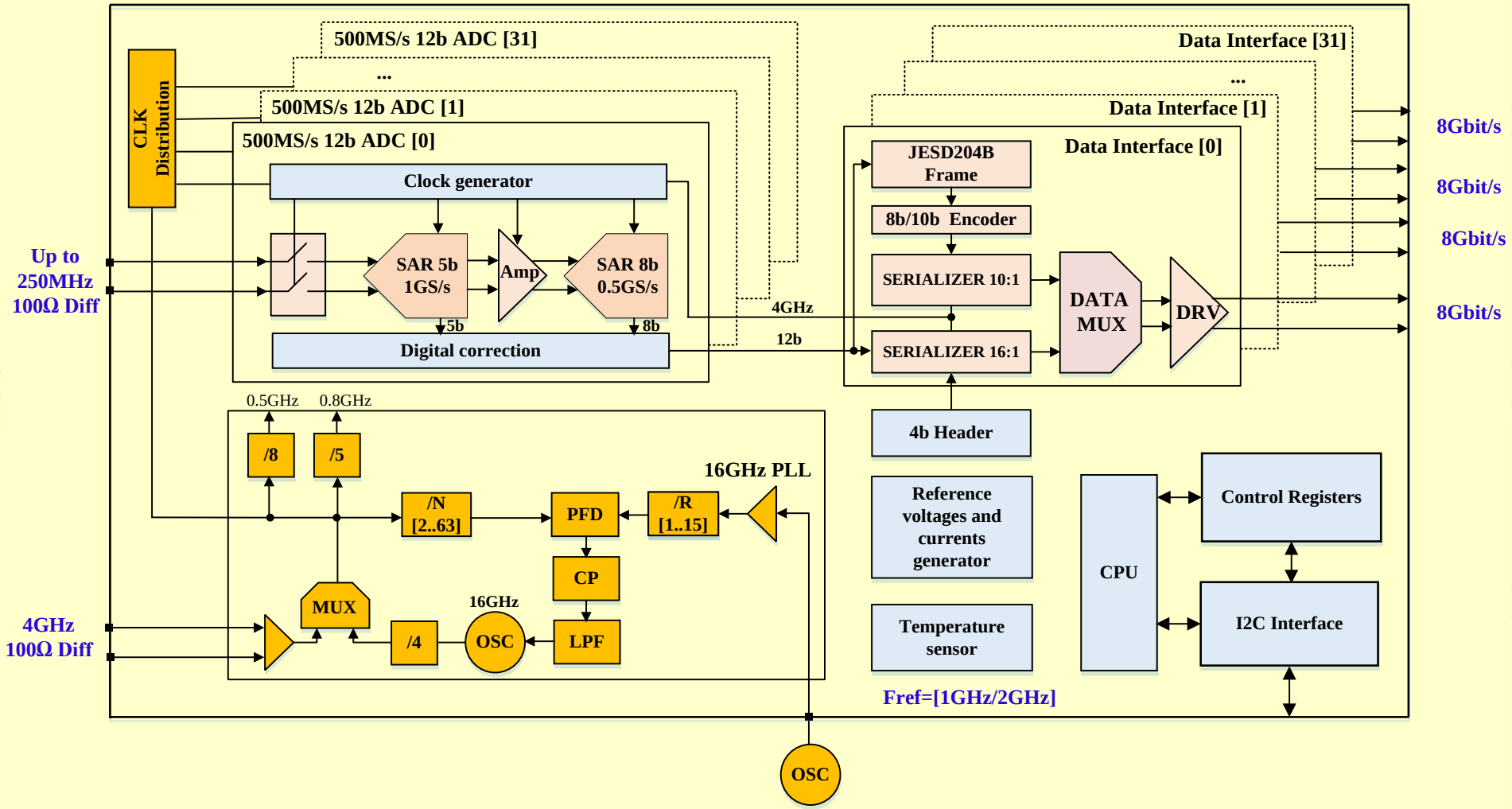
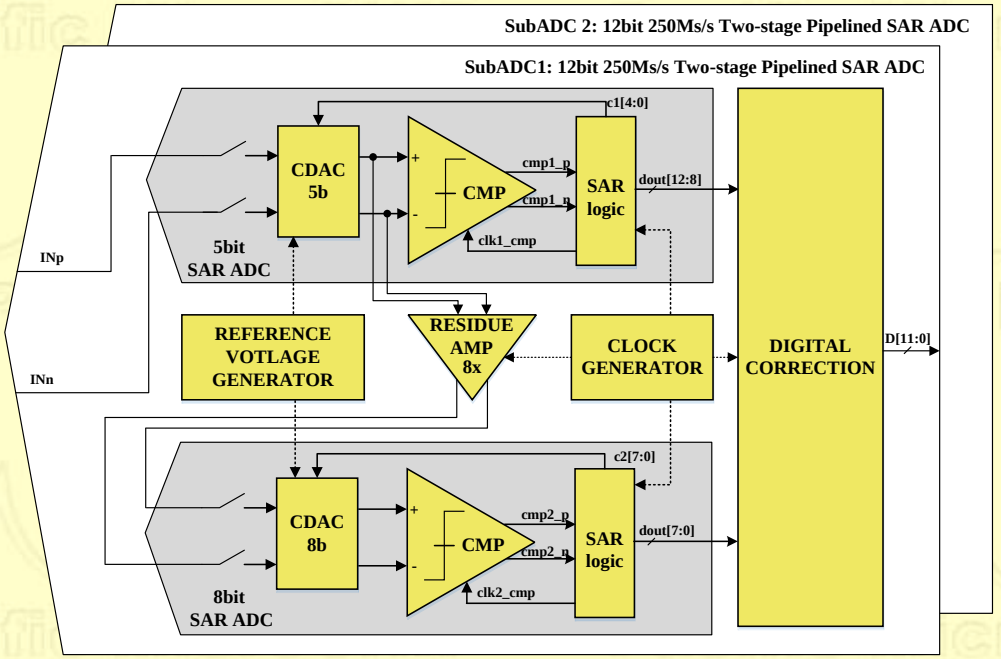
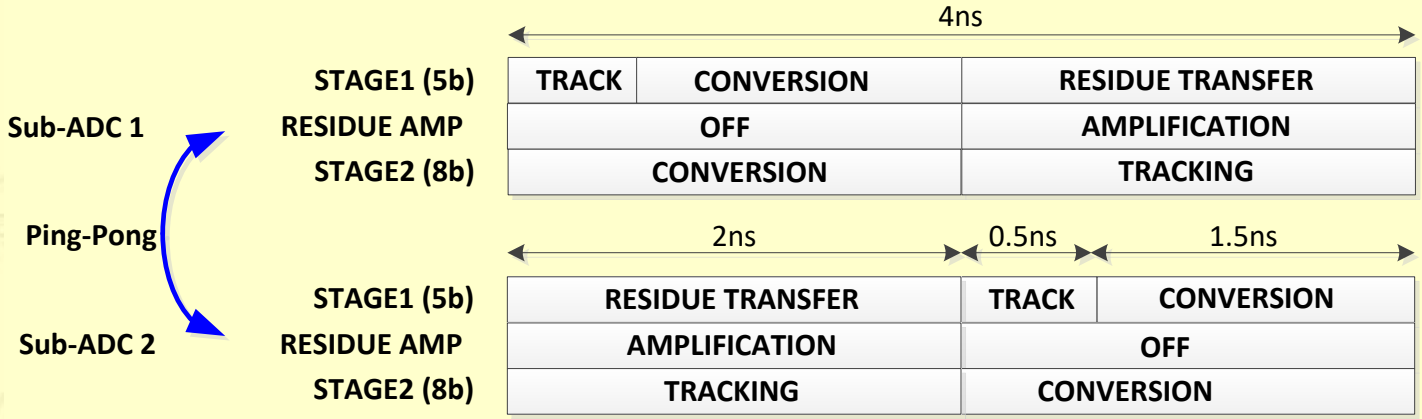
ASIC Block Diagram



12-bit 500MSps ADC Core Block Diagram

- Two-times time-interleaved ADC core
- Sampling clock skew adjustment
- Two-stage pipelined SAR architecture
- Programmable residue Amp gain
- Programmable ADC FS range
- Bootstrapped input switches
- 1-bit redundancy between ADC stages





ASIC Top-level Layout

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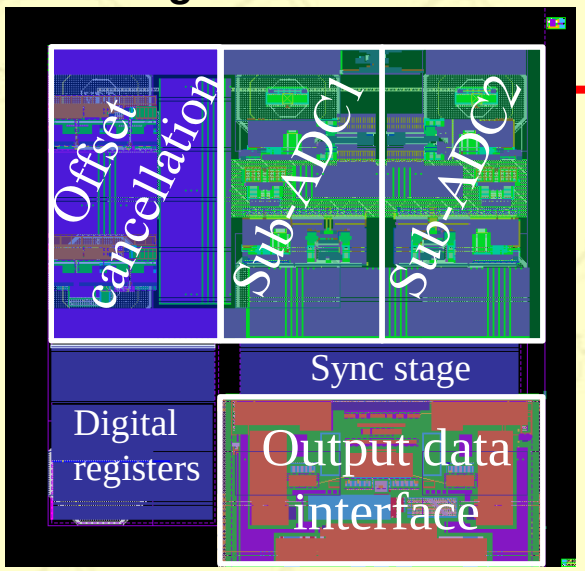
Chip's periphery:

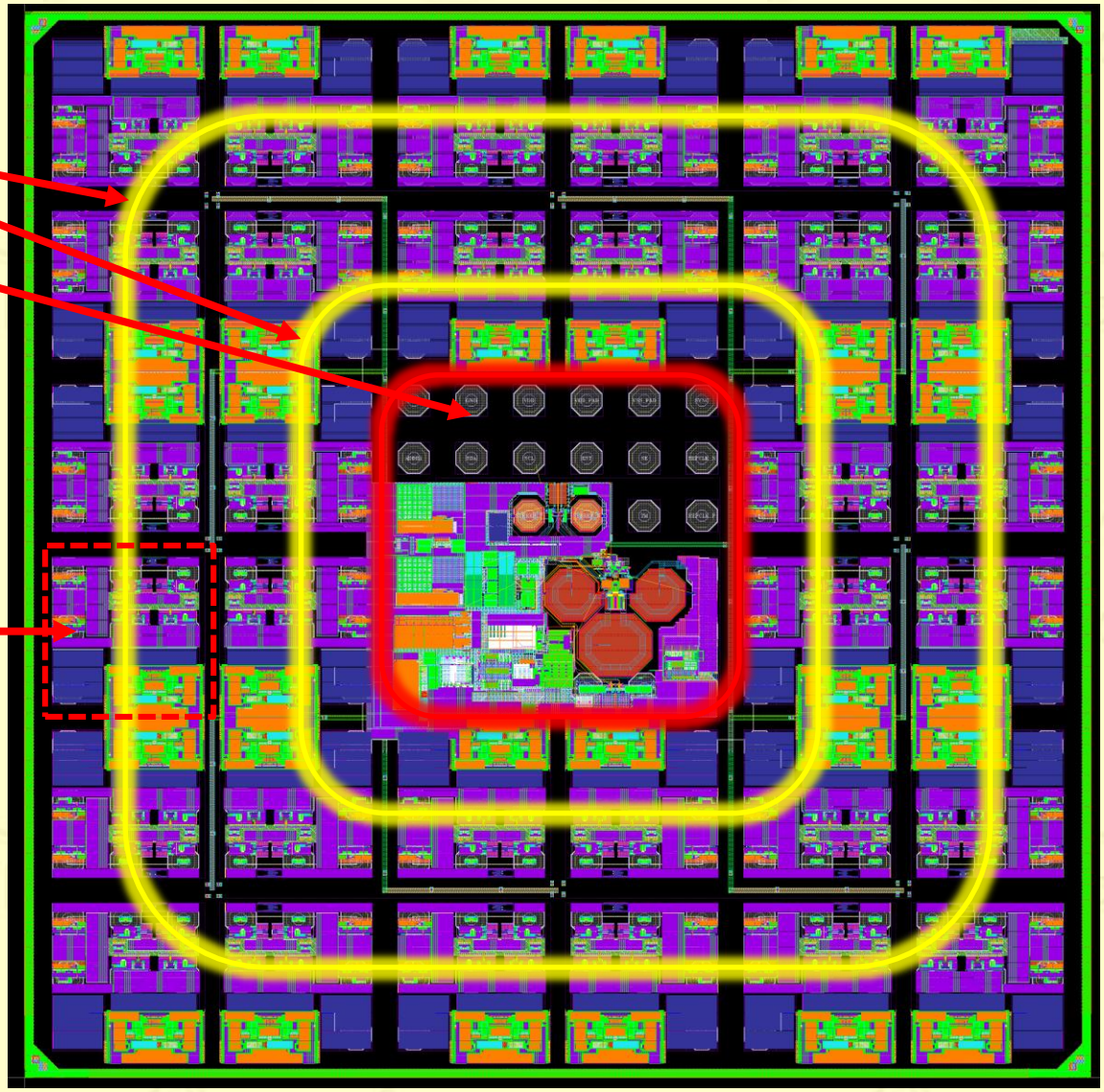
32 independent ADC channels located in 2 circles

Central part:

- **PLL with a clock tree**
- **Temperature sensor**
- **CPU for calibration**
- **I2C control interface**

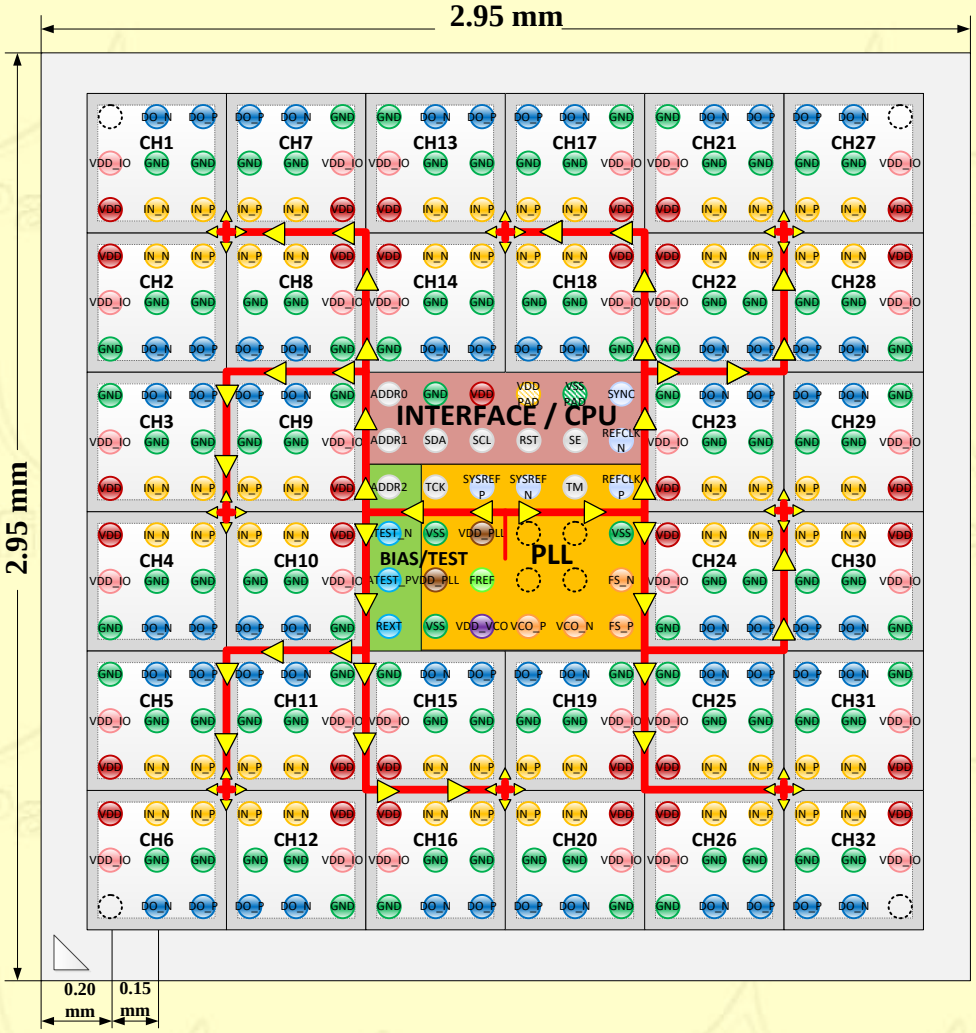
Single ADC channel





ASIC Bump Map

Clock distribution network
Clock arrival time to ADC channels is matched to support data alignment



LEGEND:

- IN_P, IN_N — ANALOG SIGNAL INPUTS(100 Ω DIFFERENTIAL, BANDWIDTH > 1GHz)
- CLK_P, CLK_N — SAMPLING FREQUENCY CLOCK INPUTS, 2GHz, 100 Ω DIFFERENTIAL, BANDWIDTH >2GHz
- VDD_IO — JESD OUTPUT INTERFACE TX SUPPLY 1.2V
- VDD — ADC CORE SUPPLY 0.9V
- VSS PAD, VDD PAD — DIGITAL IO PAD SUPPLY 1.8V
- VSS — GROUND
- REXT — OUTPUT FOR EXTERNAL RESISTOR (DC CURRENT <1mA)
- ATEST_P, ATEST_N — ANALOG TEST OUTPUT (DC CURRENT <1mA / DC VOLTAGE)
- DO_P, DO_N — CML DATA OUTPUT (UP TO 8GBit/s, BANDWIDTH >6GHz, 100 Ω DIFFERENTIAL)
- SYSREF_N, SYSREF_P, REFCLK_N, REFCLK_P — JESD204B INTERFACE RELATED SIGNALS 100Ω DIFFERENTIAL LVDS <1GHz)
- SYNC — JESD204B INTERFACE RELATED SIGNAL (SINGLE ENDED CMOS PULSE)
- ADDR0, SCL, SDA, RST, SE, TCK — I2C INTERFACE RELATED SIGNALS
- FREF — PLL REFERENCE FREQUENCY INPUT
- VCO_P, VCO_N — DIVIDED VCO FREQUENCY OUTPUT
- FS_P, FS_N — EXTERNAL SAMPLING FREQUENCY (BYPASS PLL)
- VDD_PLL — PLL SUPPLY VOLTAGE
- NO BUMP

12-bit 32 Channel 500MSps Low Latency ADC Power Budget

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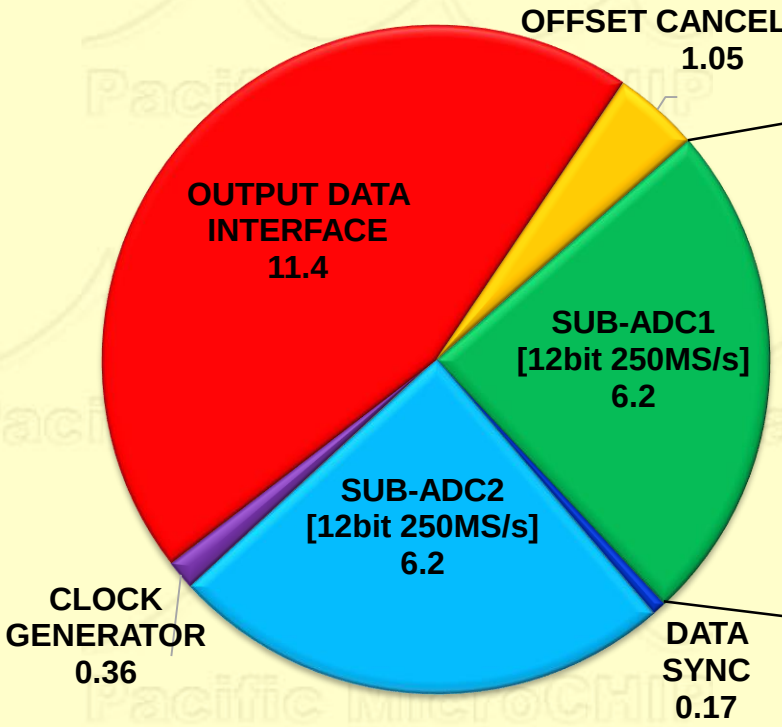
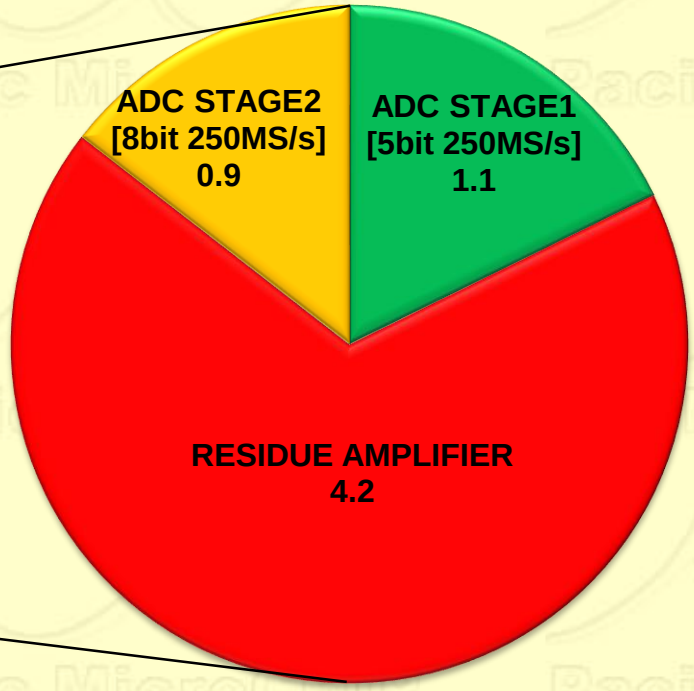
ADC channel power budget, 25mW



Sub-ADC power budget, 6.2mW

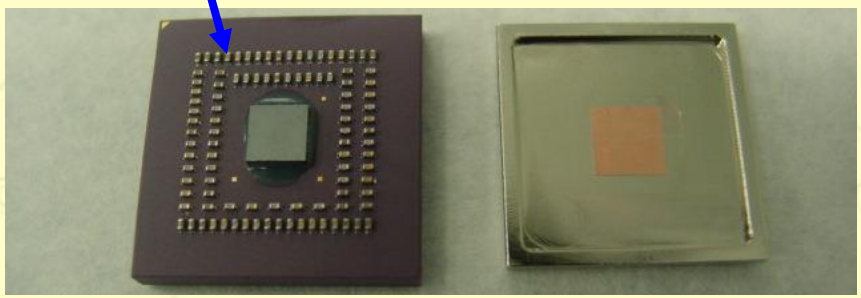


Expected Part Appearance

BGA 18 x 18 balls, 0.8mm ball pitch

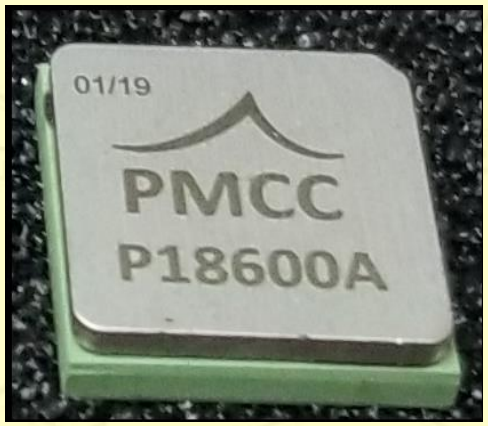
Bypass capacitors on the chip carrier

Lid

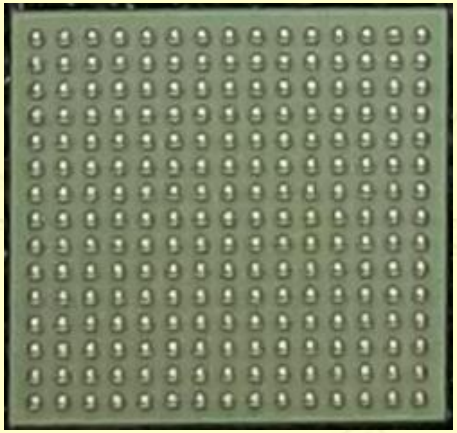


Note: Images are based on a previously developed similar BGA package.

Final part, top view



Bottom view



Comparison to ADCs Available on the Market

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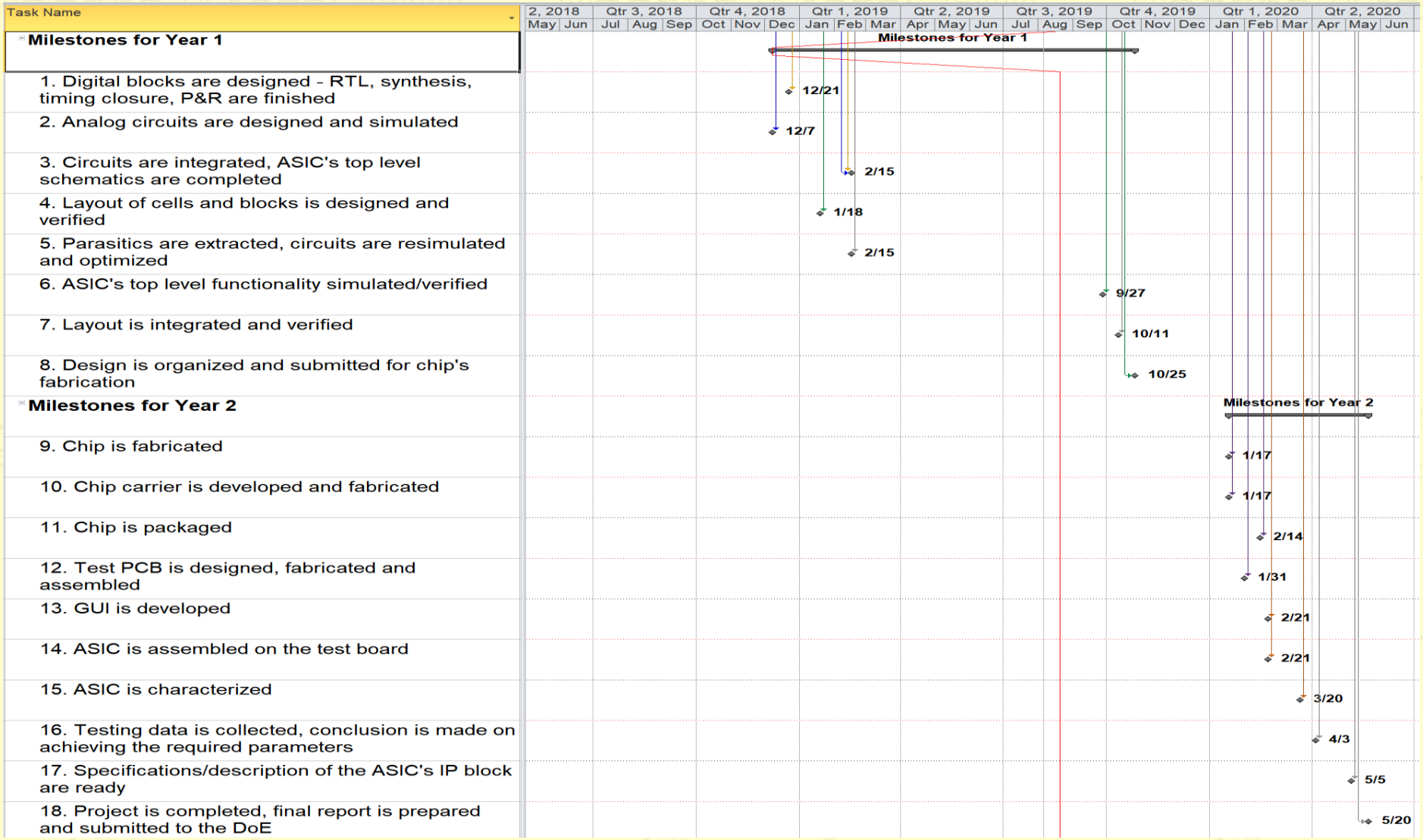
#	Vendor	# of Channels	Sample Rate, MS/s	Power Cons. per Channel	Architecture/ Latency
1.	TI 12-bit ADS52J90	32	40	41mW	Pipeline/ 2.5us
2.	TI 12-bit ADS5403IZAYR	1	500	1W	Pipeline/ 240ns
3.	TI 12-bit ADS54T04IZAYR	2	500	1.15W	Pipeline/ 240ns
4.	ADI 12-bit AD9234BCPZRL7	2	500	1.5W	Pipeline/ 240ns
5.	Pacific Microchip Corp. 12-bit*	32	500	25mW	SAR/Pipeline/ 8ns

* Expected performance

Project Milestones and Deliverables



Plans for the Future
What is Beyond Phase II?

Pacific MicroCHIP Corp.

- **End of Ph II - the chip's prototype is ready.**
- **Redesign chip based on testing results and the feedback from the customers.**
- **Fabricate the final chip.**
- **Test/evaluate it.**
- **Prepare chip description and datasheets.**
- **Organize the ADC ASIC design as an IP block and advertise it.**
- **Provide the chip to the DoE community and commercial customers.**

We would appreciate any application ideas and customer leads for the presented ADC ASIC !

THANK YOU