Distributed digital data acquisition system with network time synchronization

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Phase I: 2017-2018, Phase II: 2018 – 2020 (2021)

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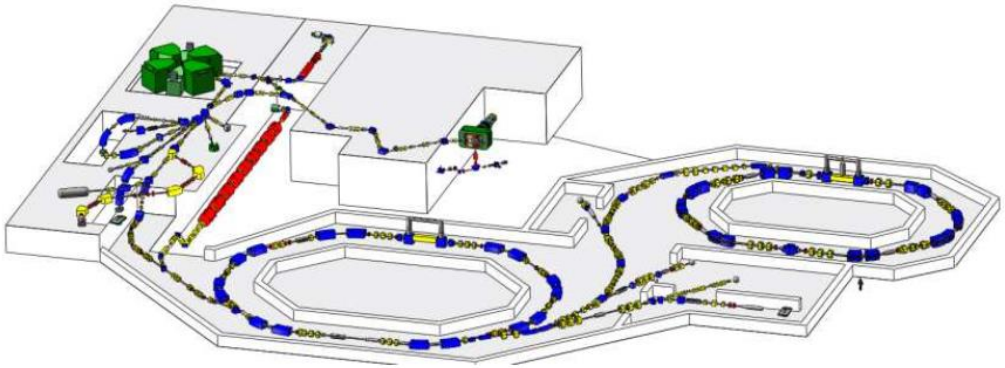
Distributed digital data acquisition system with network time synchronization

Motivation

Large nuclear physics experiments often use physically separated radiation detectors

Electronics to read out detectors must be synchronized to 100ns-100ps, ideally <10ps

Traditionally use clock/trigger cables for synchronization ☹



XIA has been developing digital data acquisition electronics for radiation detector applications for over 20 years

Modern technologies allow time synchronization through data network

New DAQ electronics with White Rabbit / PTP synchronization

Motivation

XIA SBIR Project Goals

- Adapt IEEE 1588 Precision Time Protocol technologies to XIA's detector readout DAQ modules for clocking and develop a "software triggering" concept
- Stay within standards, use open HW/SW environment, remain compatible

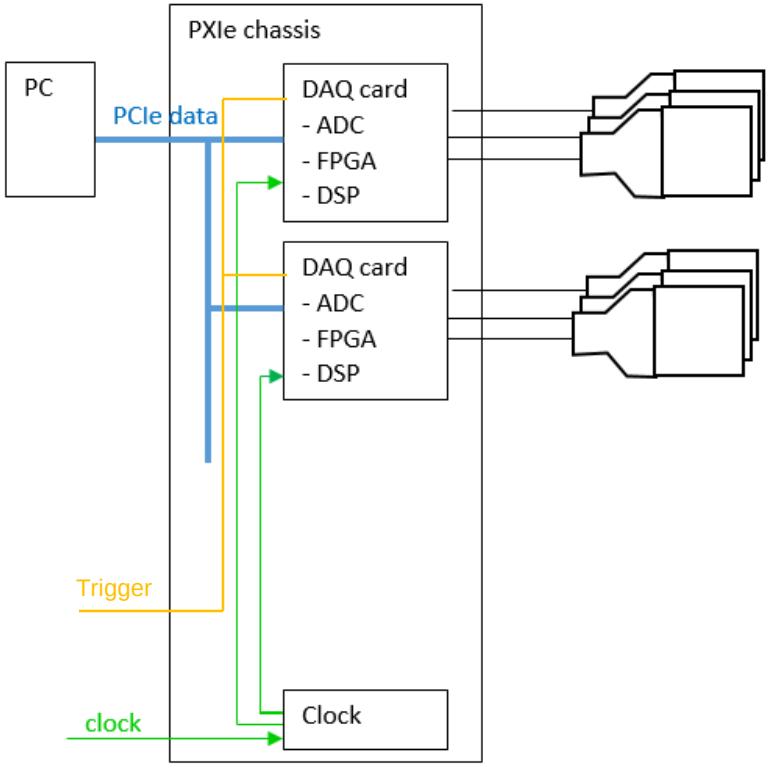
⇒ Phase I: Standard PTP (1588-2008) and Synchronous Ethernet

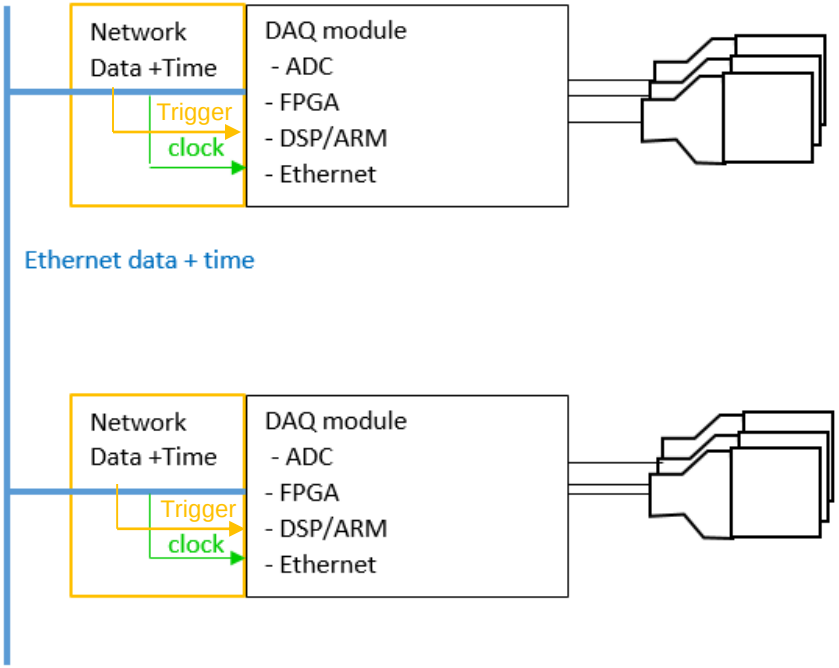
⇒ Phase II: White Rabbit (now 1588-2019 high accuracy profile)

Requirements for timing precision depends on experiment

Background reduction by coincidence:	Hundreds of nanoseconds
Event building for detector arrays:	Tens of nanoseconds
Time of flight measurements:	Sub-nanosecond
Goal in SBIR topics:	"10 ns"; "1 ns or better"

Detector Readout Electronics Synchronized Through Ethernet Network Timing Techniques





Traditional

Crate with data I/O to host PC and backplane clock/trigger distribution

Tag detector data with backplane clock (48bit)

This Project

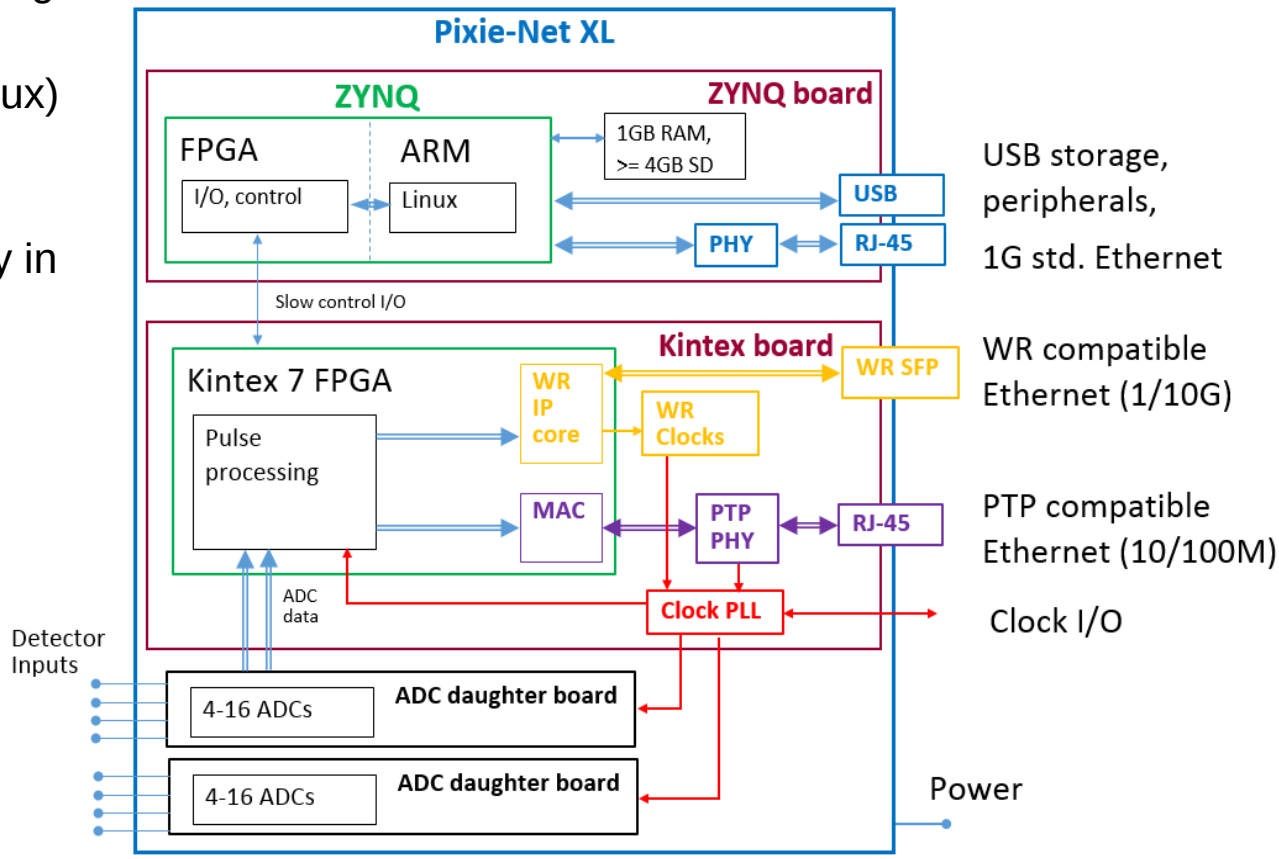
Independent modules with network data, derived clock, and “software trigger”

Tag detector data with UTC-related timestamps (date/time to ns precision)

Distributed digital data acquisition system with network time synchronization

Phase II DAQ hardware: Pixie-Net XL (PXdesk)

- Pulse processor board using Kintex 7 FPGA
- Zynq controller board (Linux) for setup, diagnostics.
- ADC daughtercards for detector readout (flexibility in ADC channels, rate, precision, or non-ADC functions)
- High speed data flow from ADC to FPGA to Ethernet output
- WR, PTP, SyncE can be used as source for ADC and FPGA clocking
- Goals:
  - <100ps timing resolution
  - 10G Ethernet
  - high rate pulse processing



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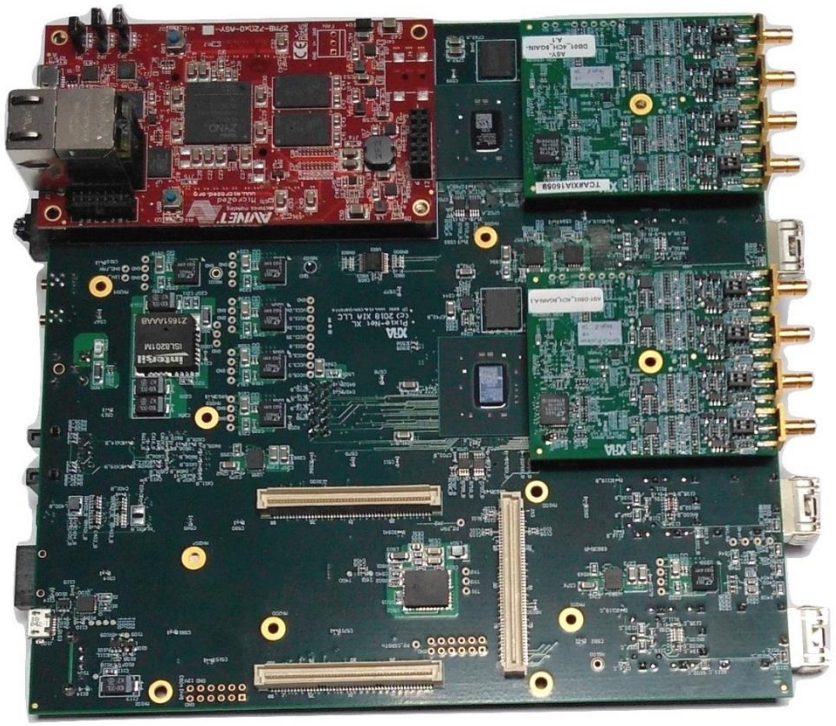
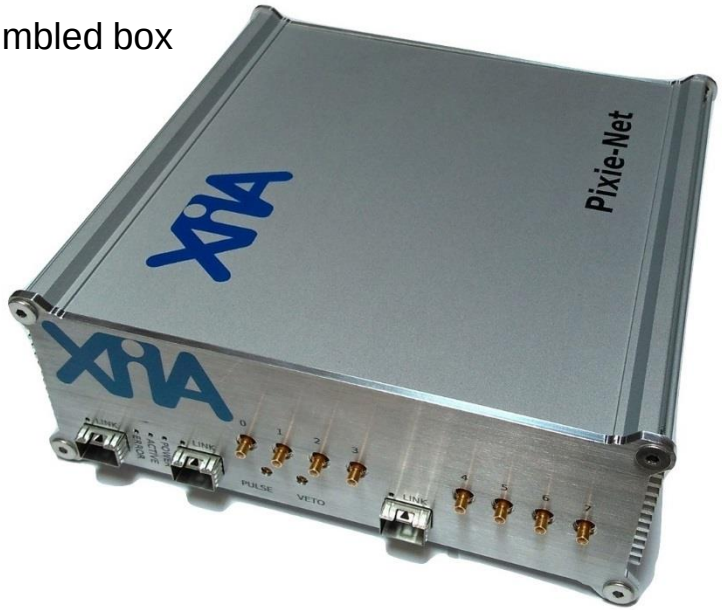
Prototypes built so far



Main board with ADC daughtercards and Zynq controller module card stack

Fully assembled box



4-channel,
75-125 MHz,
14bit ADC daughtercard

4-channel,
16bit, 250 MHz or 14bit, 500 MHz
ADC daughtercard

8-channel, 250 MHz,
12bit ADC daughtercard
Differential inputs via HDMI cable

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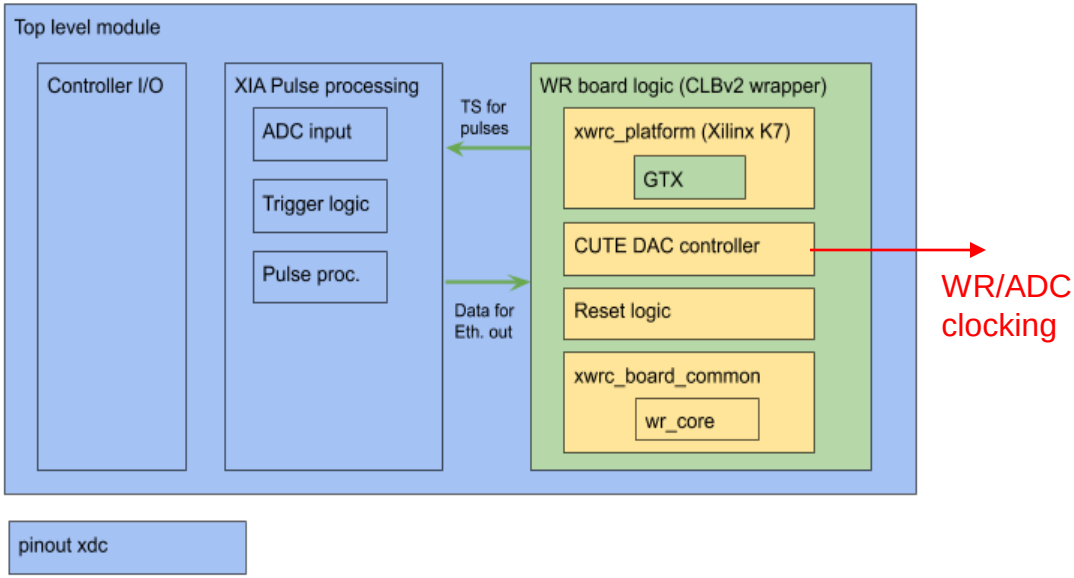
Firmware implementation

Integrated WR open source IP core into XIA pulse processing

=> Pixie-Net XL can

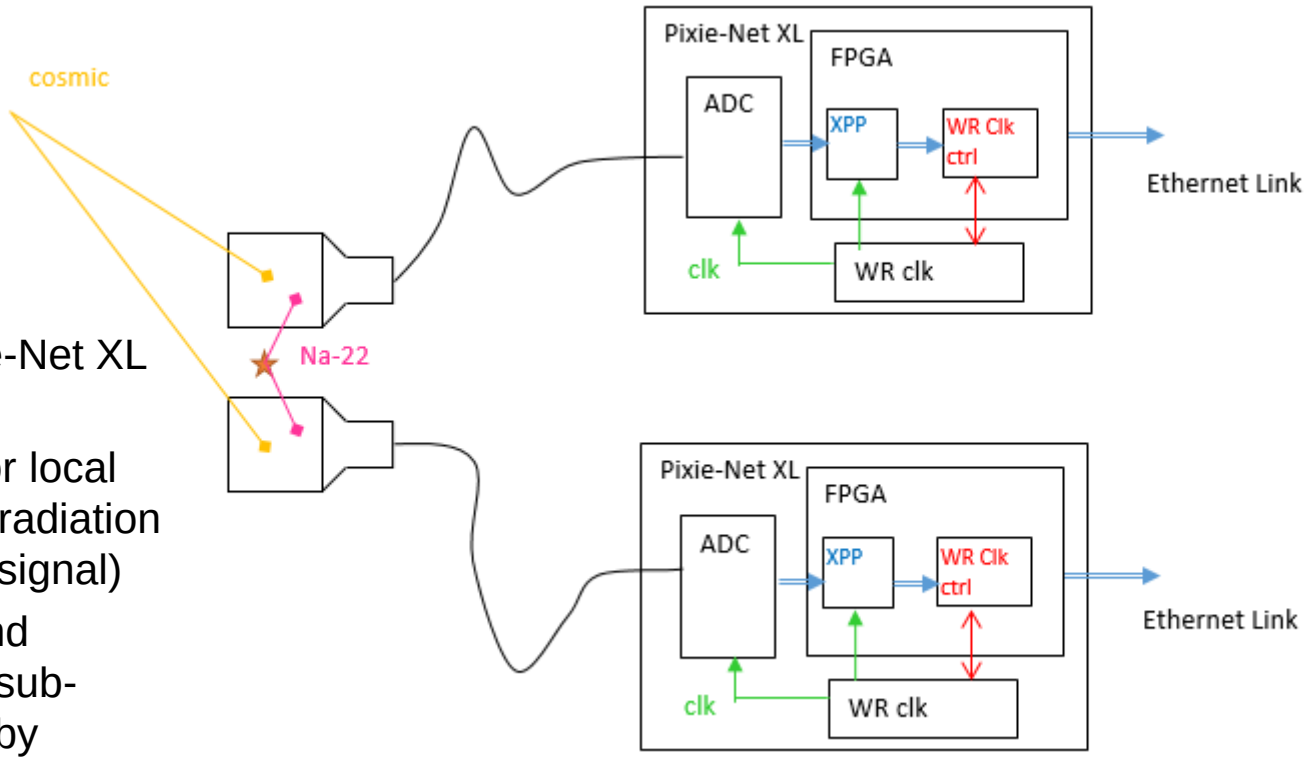
- capture detector pulse data and compute energy, MCA histograms, CFD timing, etc
- tune local clocks for WR and ADC to WR master (frequency + phase)
- record WR date/time in captured detector data
- send out Ethernet data via WR core

FW block diagram



XIA pulse processing adapted to Kintex board
WR open source unchanged
WR open source adapted

Timing Measurements To Characterize Synchronization



- Two detector signals connected to two Pixie-Net XL synchronized via WR
- Use cosmic showers or local Na-22 as coincidence radiation source (or split pulser signal)
- Capture waveforms and timestamps, compute sub-sample time of arrival by interpolation on rising edge (CFD)
- Histogram the difference of time of arrival in both modules, apply Gauss fit

(Pseudo time-of-flight measure of performance)

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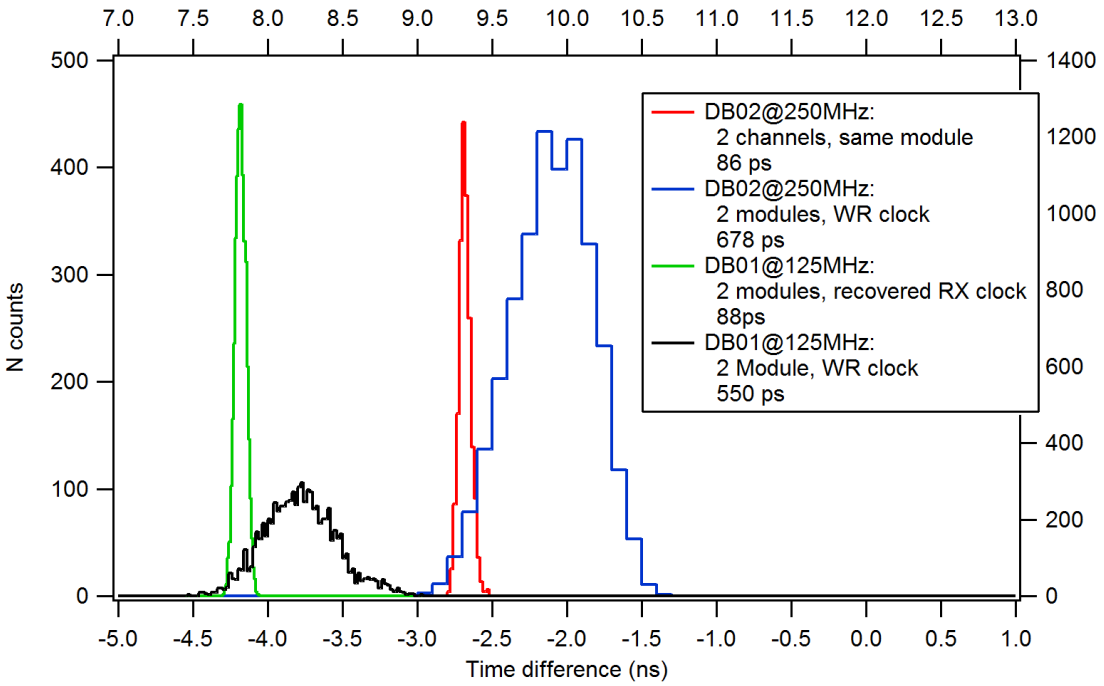
Timing Measurements – Pulser



Time Resolutions

⇒ With 75 MHz ADC daughtercard, pulser, tuned WR clock: 550 ps FWHM

⇒ With 250 MHz ADC daughtercard, pulser, tuned WR clock: 678 ps FWHM
(2 channels in same module: 86 ps FWHM)

⇒ With 125MHz ADC daughtercard, pulser, recovered RX clock: 88 ps FWHM

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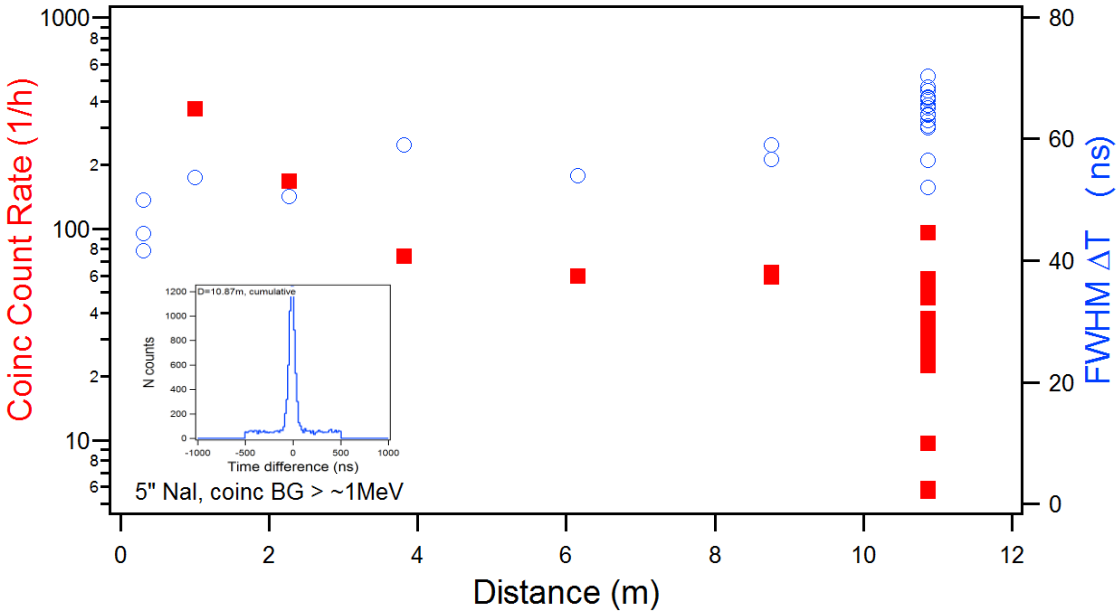
Timing Measurements – Cosmic coincidences

- Demonstrating synchronization over long time and large distance (goal is not high precision)
- Only use WR time stamps, not waveform interpolation



⇒ Background rate ~500 counts/s each detector, recording ~8.5 million records (>1 MeV) per day.

⇒ Coincidence rate decreases with distance. Hundreds of coincidence events per day at ~11m distance.

⇒ Timing resolution ~70 ns FWHM

If modules could share trigger information besides clock synchronization, we would not have to record the 99.984% waste data => use Software Triggering

(P. Auger, et al “, Rev. Mod. Phys. 11, 288 (1939). https://doi.org/10.1103/RevModPhys.11.288)

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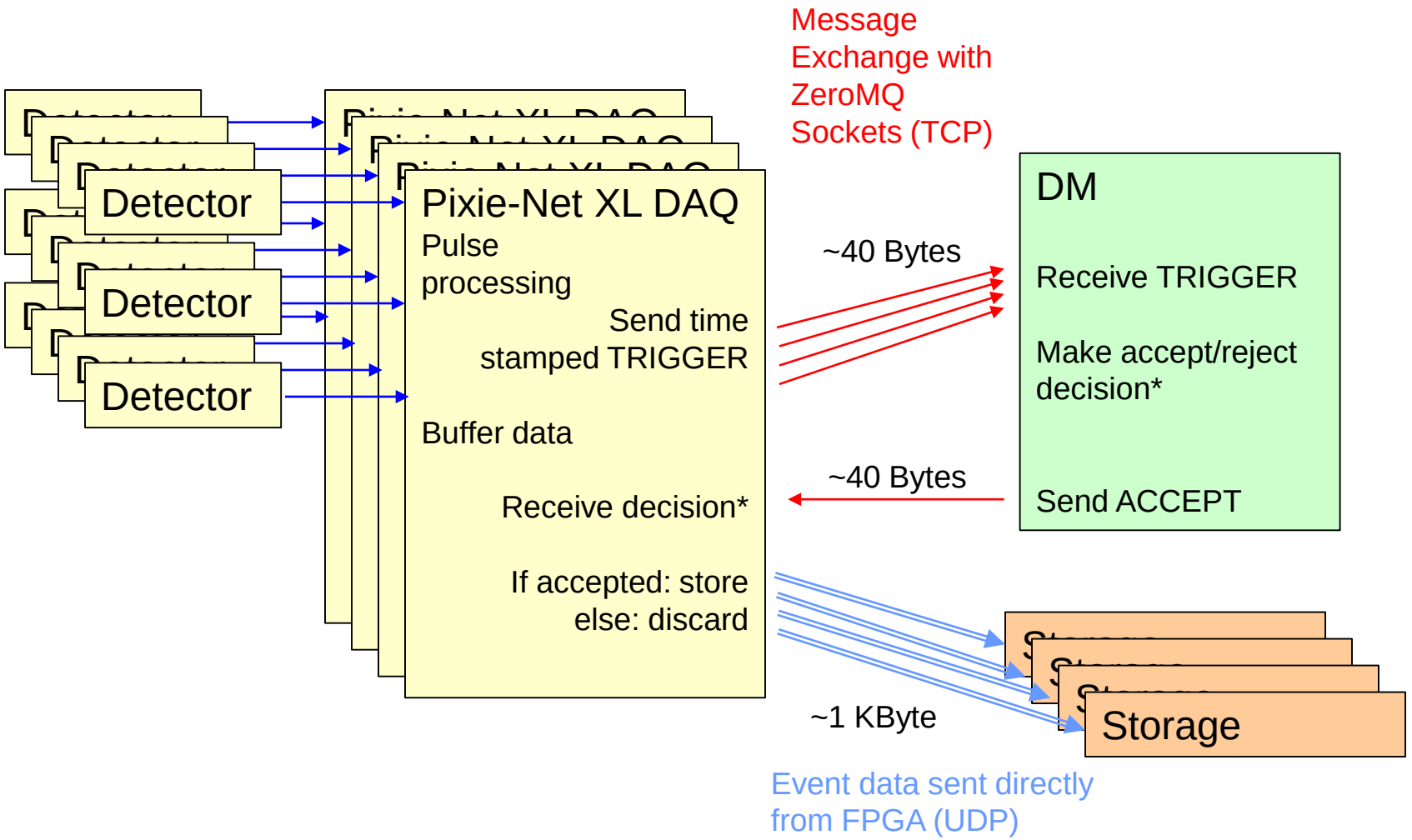
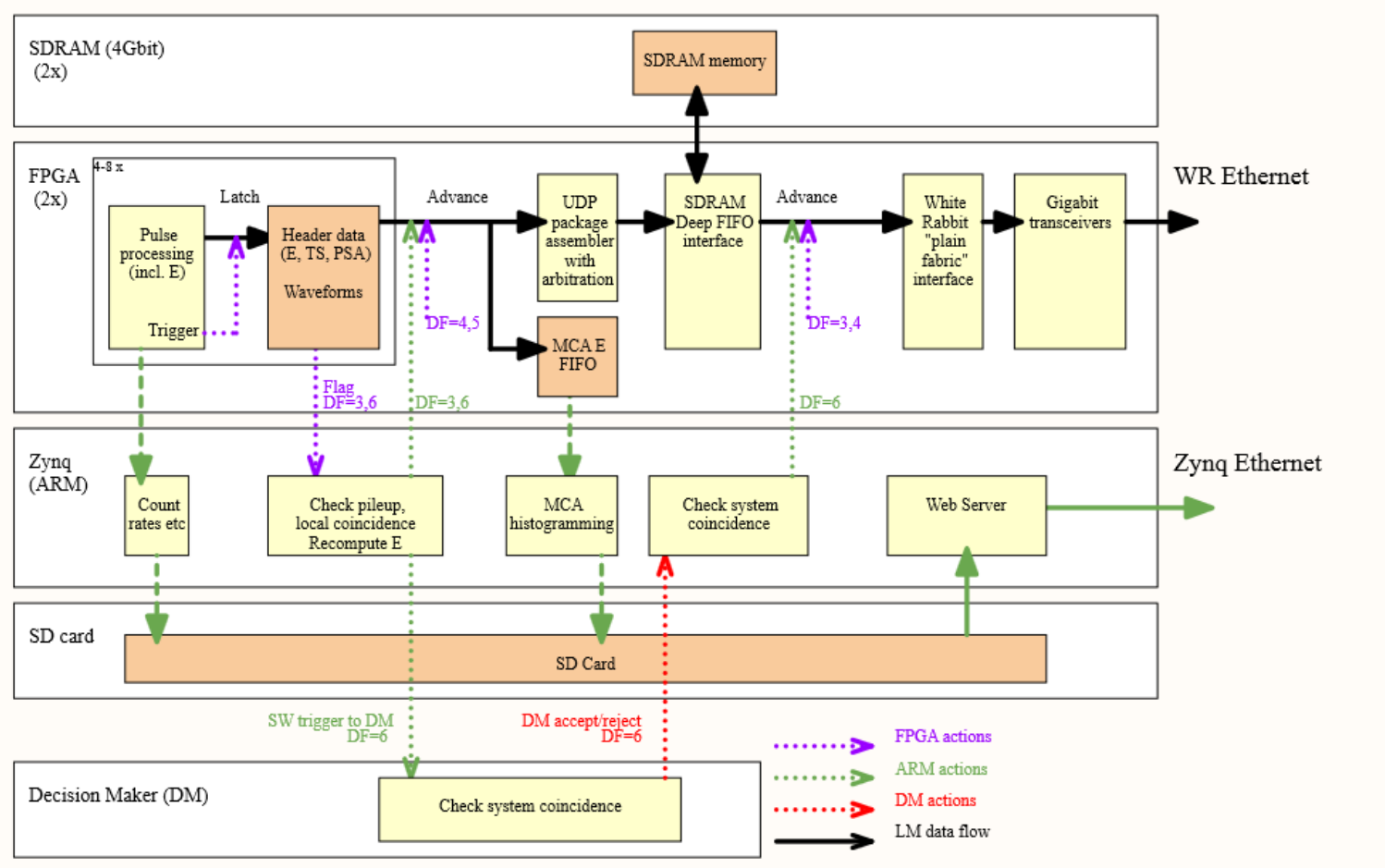
Software Triggering: Overview



* = coded decision making, based on WR time stamp, hit pattern, history, …

Software Triggering: Implementation



Most data flows through FPGA only (and SDRAM buffer)

Meta data used for **coded** decision making in ARM (Linux C/C++) …

… and DM (Ruby)

Various “Data Flow” options, can also simply output all data from FPGA and sort out offline

(xillybus.com/tutorials/deep-virtual-fifo-download-source)

Software Triggering: Applied to Cosmic Coincidences

“Accept all local” mode:
- DM is programmed to respond with ACCEPT to all TRIGGER messages
- ARMs are programmed to approve records matching time and channel of the ACCEPT message
  i.e. **all local** triggers are approved;
  ACCEPT messages due to TRIGGERs from **other** DAQs are ignored)

=> Measured acceptance rates are 150-300 counts/s in 2 neighboring detectors.

“Coincidence only” mode:
- DM is programmed to respond ACCEPT to all TRIGGER messages
- ARMs approve records matching time but not channel of the ACCEPT message.
  i.e **local** events are approved **if** an event occurred within the coincidence window in the **other** DAQ.
  ACCEPT messages due to TRIGGERs from **local** DAQs are ignored.)

=> Measured acceptance rates are ~ 1-2% of the singles rate.

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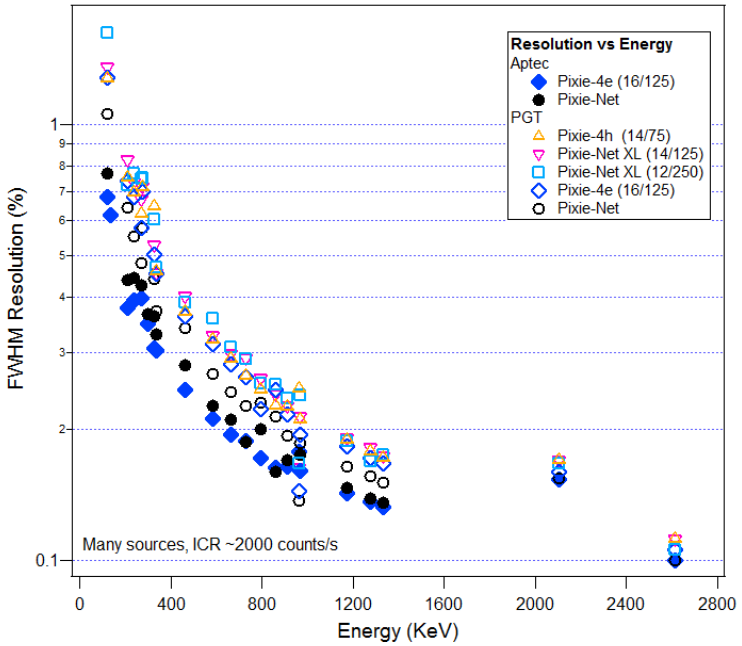
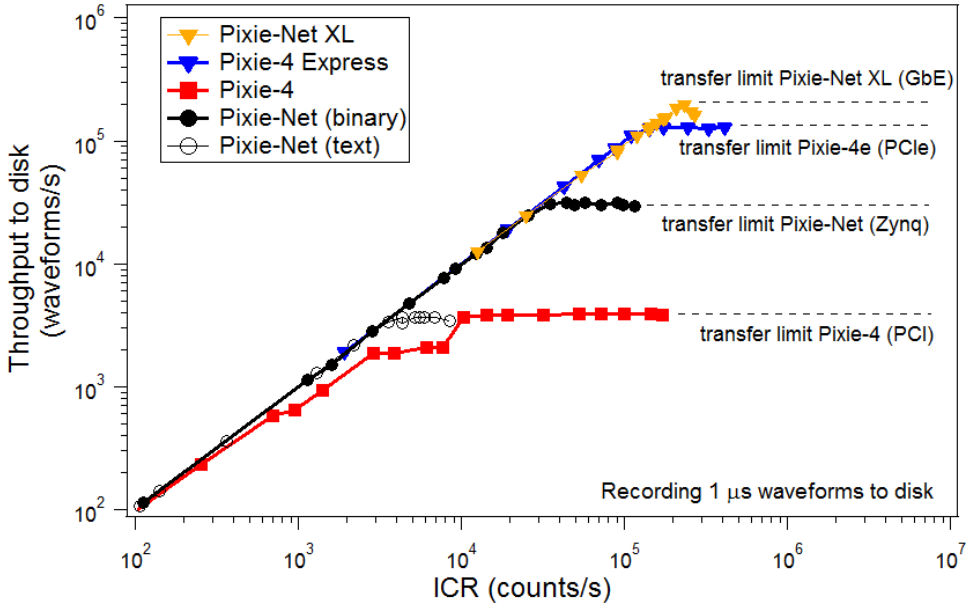
Other Performance Testing (preliminary)



Pixie-Net XL HPGe energy resolution: matching older readout electronics.



Pixie-Net XL list mode throughput surpassing older electronics.

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Commercial Branches: SBIR work adopted in other XIA products*

- **Pixie-Net PTP**
  Phase I PTP prototype commercially available. Several units sold

- **Pixie-16 MZ-TrigIO**
  Trigger I/O module for XIA's 6U PXI pulse processor boards with PTP clock option.
  Several units sold.
  Also available as desktop PTP GPIO module

- **Pixie-4 Hybrid**
  Update of XIA's 3U PXIe pulse processor board with WR synchronization and data output.
  Reusing same ADC daughtercards
  Product release October 2020 (firm PO)

- **PXIarge**
  Update of XIA's Pixie-16 pulse processor board
  Reusing same ADC daughtercards.
  Product release est. March 2021

* Mainly funded by XIA

Summary

Hardware platform

- Implemented WR network time synchronization on new detector DAQ electronics, the Pixie-Net XL
- Easily reaches “<1 ns” timing resolution goal, demonstrated <100ps, but needs more tweaks to reach “best WR” performance of <20ps (in progress)

Software triggering

- Developed concept and demonstrated principle of operation
- Alternatives under consideration (Dolosse, White Rabbit Trigger Distribution)

Outlook

- Upgrade Ethernet data to 10 Gbps rates (new WR switch under development)
- Performance testing, beta testing at NP labs, and product release (2021)

(dolosse.org) (ohwr.org/project/wrtd/wikis/home)

Detector Readout Electronics Synchronized Through Ethernet Network Timing Techniques

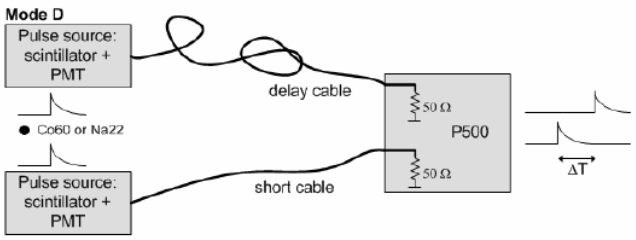
Thank You

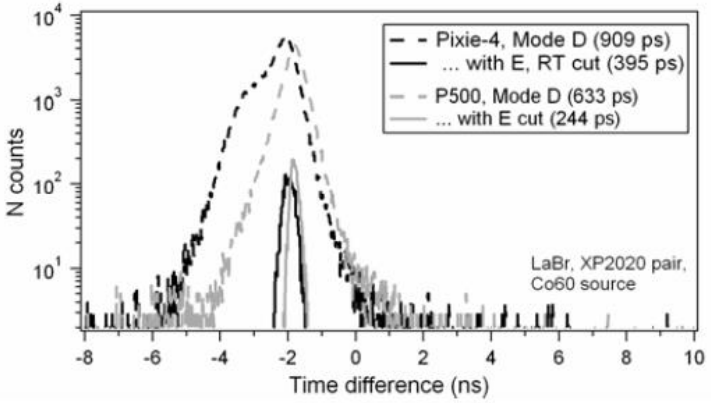
Questions?

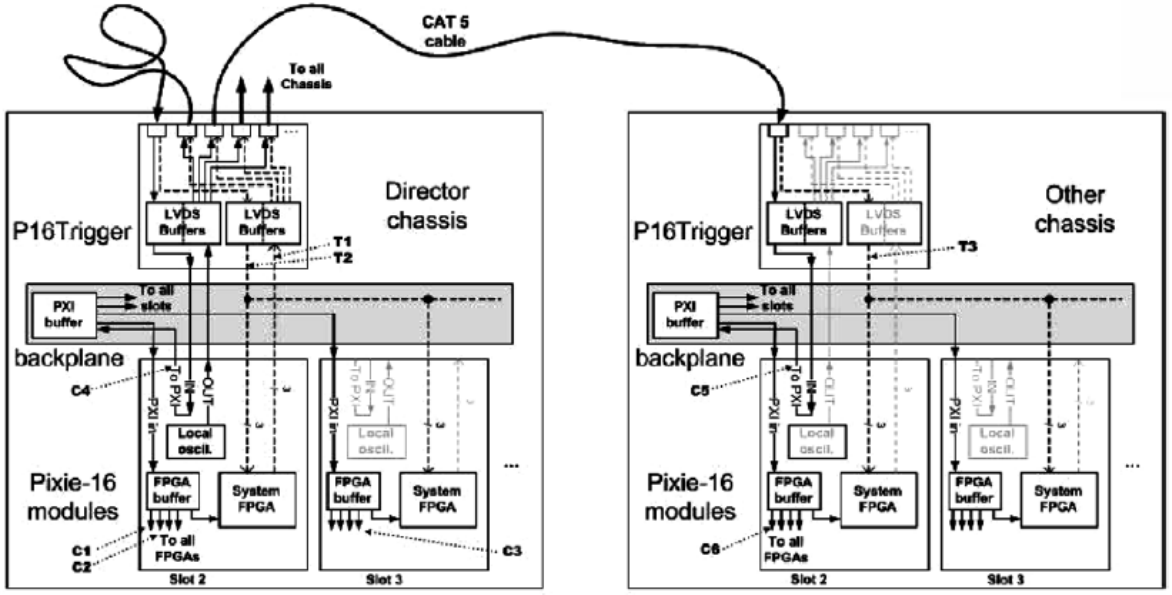
Traditional Synchronization

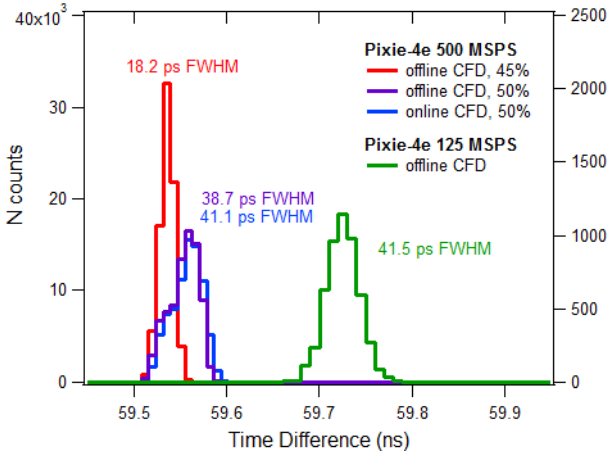
Traditionally, time synchronization between multiple channels of digital data acquisition is accomplished by sharing clocks, clock reset signals, and triggers.

With suitable algorithms (CFD), timing resolutions can be ~20 ps for idealized signals and a few hundred ps for detector signals digitized with 100-5000 MSPS.









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Existing Technologies

- **Shared Clock Signal**
  Works, but requires dedicated cabling. Not ideal for distributed DAQ systems.
  Reported time resolution: sub-nanosecond, even tens of picoseconds

- **IEEE 1588 Precision Time Protocol (PTP)**
  Processors exchange synchronization messages over network to measure delays
  PTP Time Stamping Units (TSU) built into several commercial Ethernet MACs, Ethernet physical layers (PHY). Commercial PTP switches available ($$).
  Open source software for managing time synchronization (LinuxPTP, ptpd)
  Reported time resolutions: milliseconds (software TSU)
  low nanoseconds (hardware TSU)

- **Synchronous Ethernet (SyncE)**
  Extract clock from Ethernet link and use for local processing

- **CERN's White Rabbit (WR)**
  Extension of PTP standard with synchronous Ethernet
  Open hardware project. WR network switch commercially available. WR modules developed by scientists
  Reported time resolution: sub-nanosecond, even tens of picoseconds

UDP Data Output Discussion

Pro:

- Simple to implement in FPGA (WR code) and on receiving side
- Easy transfer to one or more storage nodes
- Faster

Contra:

- Possible loss of data — but 1 packet = 1 event; but how bad is it actually? [Ref]; but DM has TRIGGER data
- Possible data out of sequence — but all packets timestamped
- Error checking pushed to “higher level application”

=> Will look into firmware updates for UDP package management or for TCP

(M.J. Christensen et al: Achieveing reliable UDP transmission at 10 Gb/s using BSD socket for data acquisition systems, arXiv:1706.00333v1 [physics.ins-det] 1 Jun 2017)