Low Cost Data Acquisition Synchronization for Nuclear Physics Applications

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SkuTek Instrumentation
SkuTek.com

Outline

- Outline
  - The company and its capabilities.
    - Customers.
    - Success Story: LZ deployment.
  - Description of the Phase I project: Proof of principle.
  - Description of the Phase II project: The goal.
  - Phase II progress and achievements.
  - Highlights of the final products.
  - Plans.

The company and its capabilities

- The team: two physicists, a senior software engineer, a part time engineering associate, and a manager. We regularly work with a local EE consultant.
- We worked with several interns listed on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, DM search, etc.

Our capabilities: Everything, what we needed to develop a cutting edge digitizer.

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, especially Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in the FPGA (VHDL, Verilog) and in embedded processors (Pascal, Python, C).
- Processing data from nuclear detectors of any kind.
- Development of simple detector assemblies using scintillators, PMTs, or SiPMs.

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Our customers

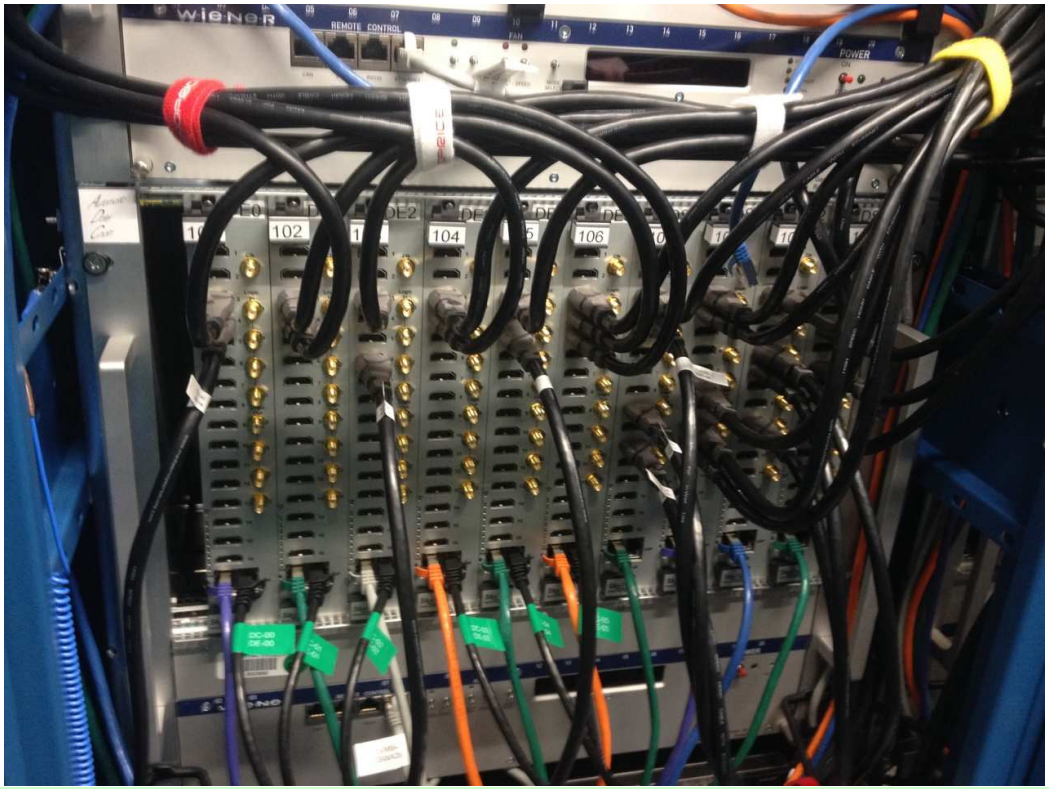
National Superconducting Cyclotron Laboratory

Brown University

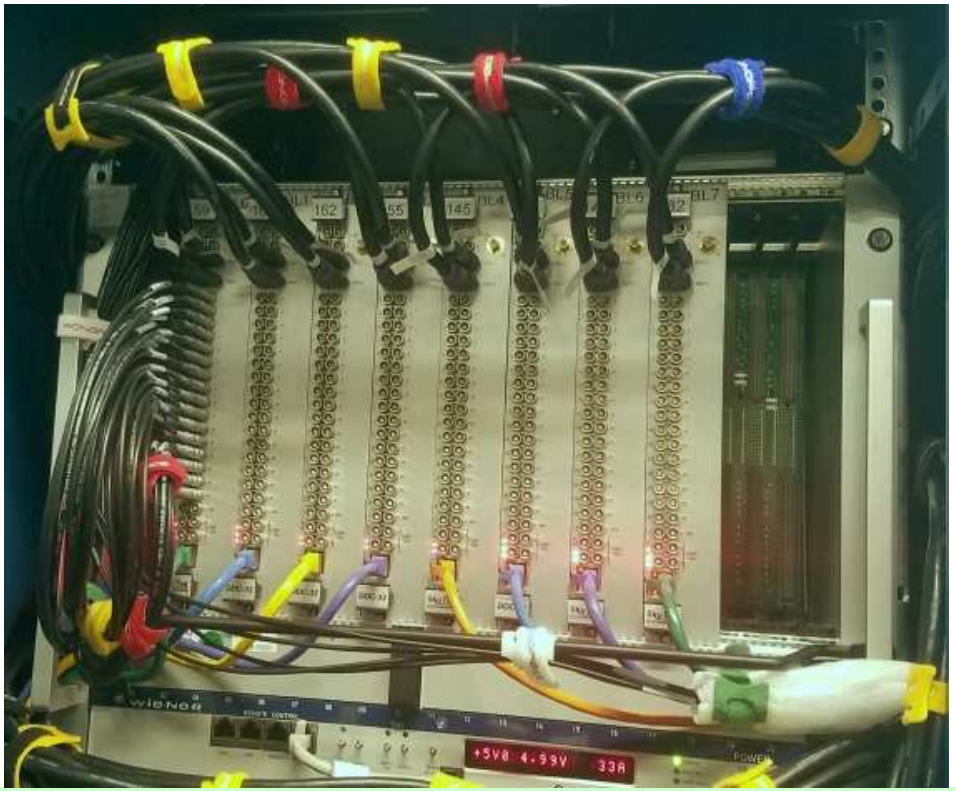
Success Story: LUX-Zeplin Data Acquisition

- LUX-Zeplin is the world's largest Dark Matter Search liquid xenon two-phase TPC (10 ton LXe).
- We delivered **1,632 channels** of the DAQ electronics to the LZ Collaboration.
- No bad channels.
- The DAQ was deployed in Sanford Underground Research Facility at -4850' last Summer.
- No problems were found with the DAQ while collecting noise signals since November 2019.
  - Continuous operation for over 6 months collecting and analyzing noise samples.

26 Logic Boards, sixteen 4 Gbps links each



51 Digitizers, 32 channels each



Phase I Project

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Phase I Project

Problem or situation that is addressed.

GRETINA and Digital Gammasphere (DGS) both use LBNL 10-channel digitizers, which were used successfully for many years. Although the hardware units are still in good shape, the legacy VME interface is limiting the data throughput due to a sequential nature of the VME readout (one digitizer at a time). Additionally, the Spartan-3 FPGAs are filled with the present firmware to about 90%. It makes the new firmware developments rather difficult.

How this problem or situation was addressed.

We proposed development of digital DAQ modules with a ***new FPGA*** generation and on-board ***Linux*** for setup & control. The *readout* and the *setup & control* paths will be ***separated***. Both paths can be ***optimized*** for their respective tasks. The digitizers will be ***compatible*** with the GRETINA & DGS environments through the use of the ANL Time and Trigger Control Link (TTCL).

Phase I project.

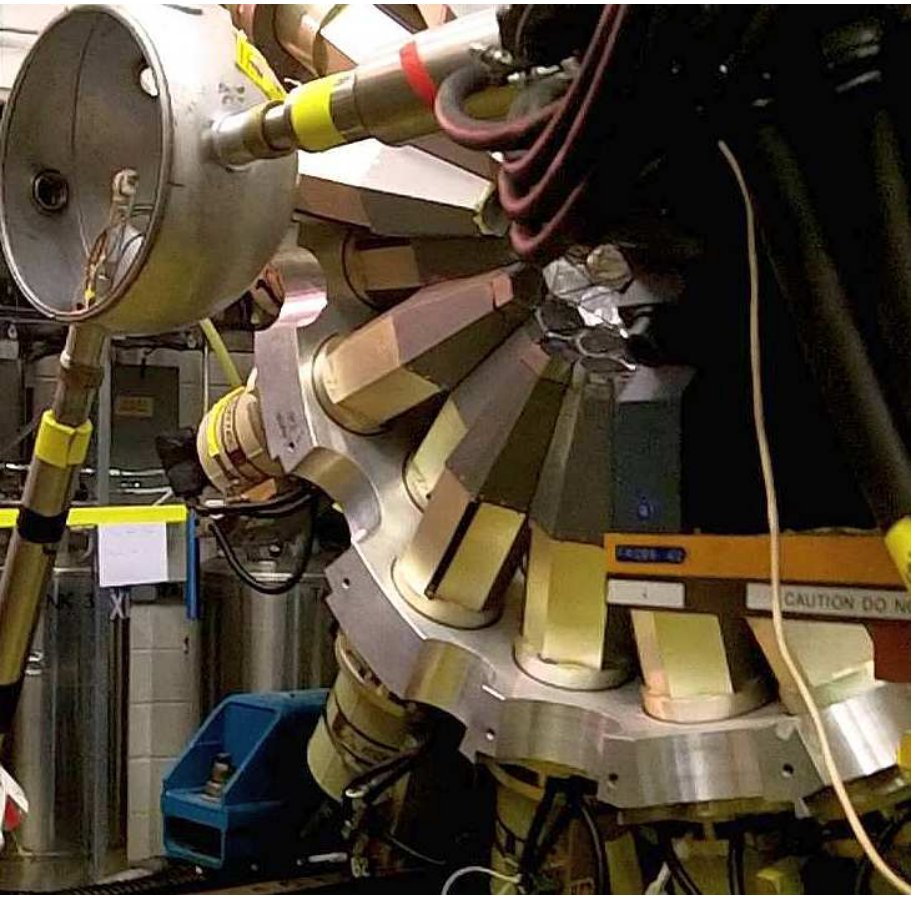
In Phase I we performed measurements with Gammasphere, using our hardware prototypes in parallel with the present LBNL DAQ electronics. The goal was to evaluate whether or not our prototypes would perform on par with the established LBNL units.

Digital Gammasphere (DGS)

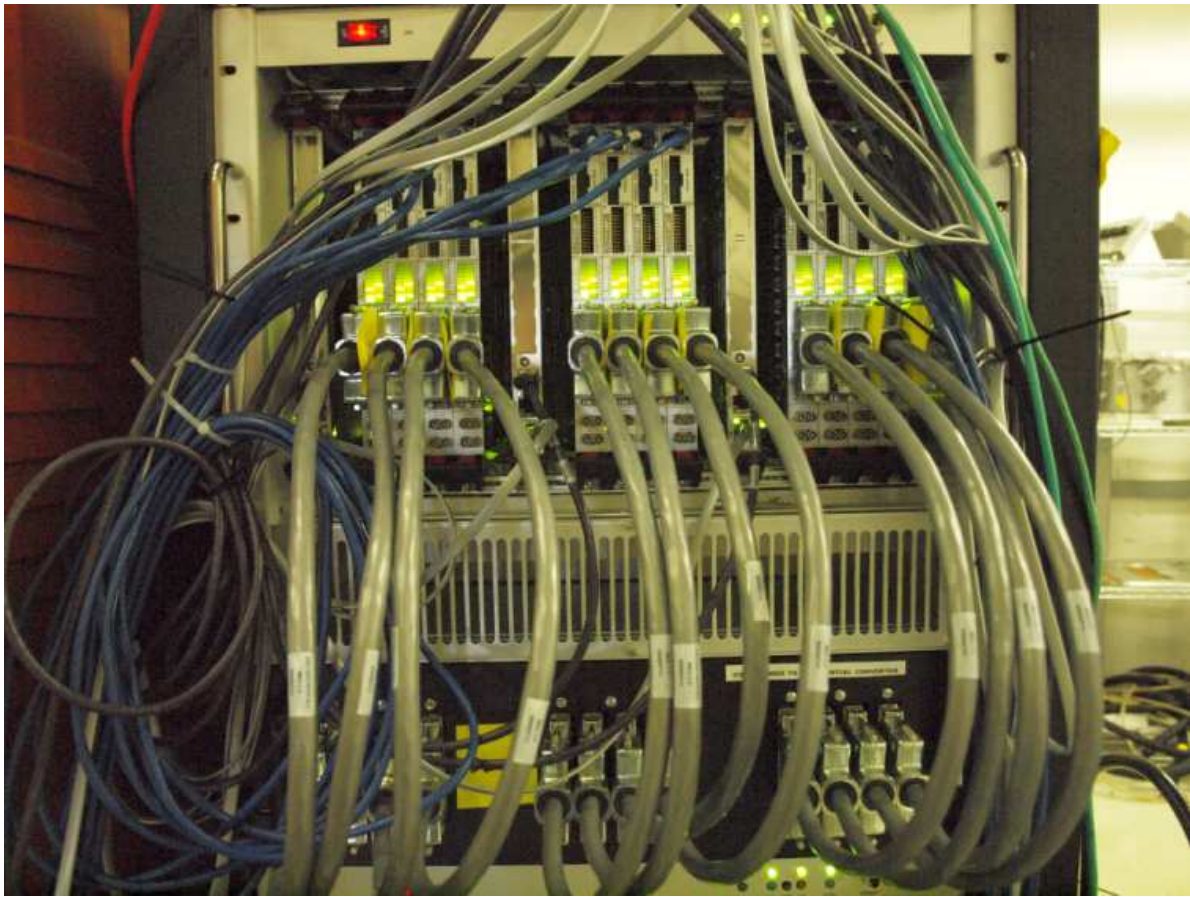
Gammasphere consists of 108 Compton-suppressed high-purity germanium (HPGe) detectors surrounded by the BGO anti-Compton shields.

The Digital Gammasphere is equipped with the digital electronics originally developed by LBNL for GRETINA. Each LBNL digitizer provides 10 channels, 14 bits @ 100 MSPS.

Gammasphere Detector Array



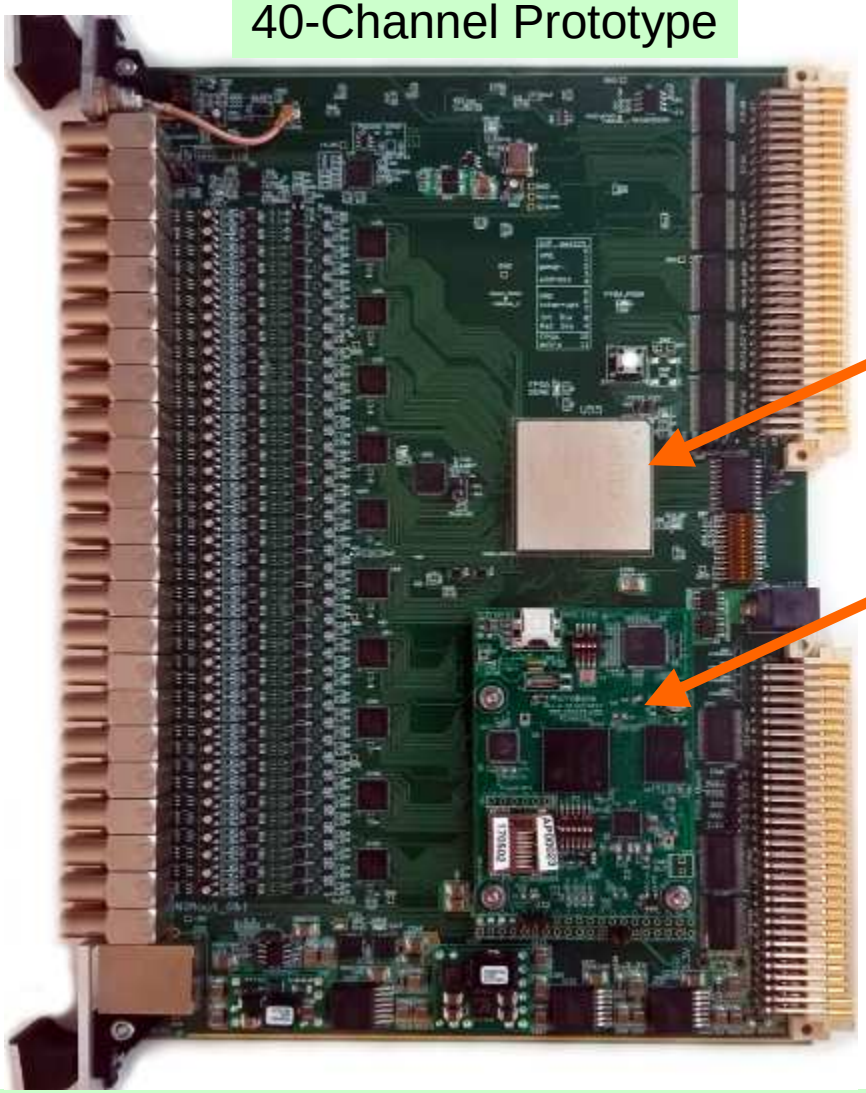
Digital Gammasphere LBNL Electronics



We Used 40-Channel Prototype by SkuTek

- In **Phase I** we used the 40-channel prototype, 14 bits @ 100 MSPS.
- We used the on-board Linux to setup the digitizer and to collect the waveforms.

40-Channel Prototype



Optional external clock
Four NIM in
Four NIM out

40 analog inputs

GbE over RJ-45

VME Interface

Kintex-7

ARM processor running Linux
1GHz clock, 512 MB of RAM
Parallel memory interface to FPGA
GbE interface to front panel

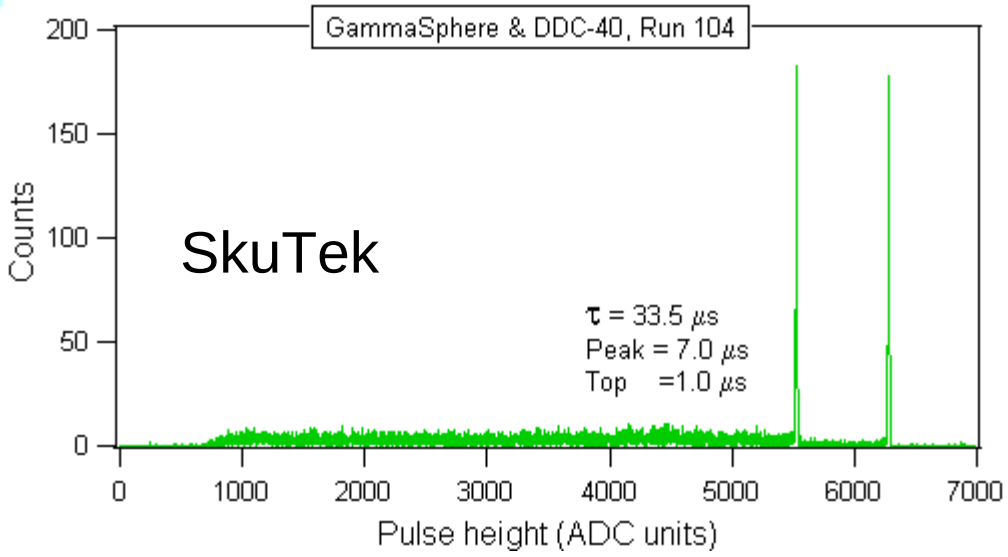
Can perform **real-time diagnostics**

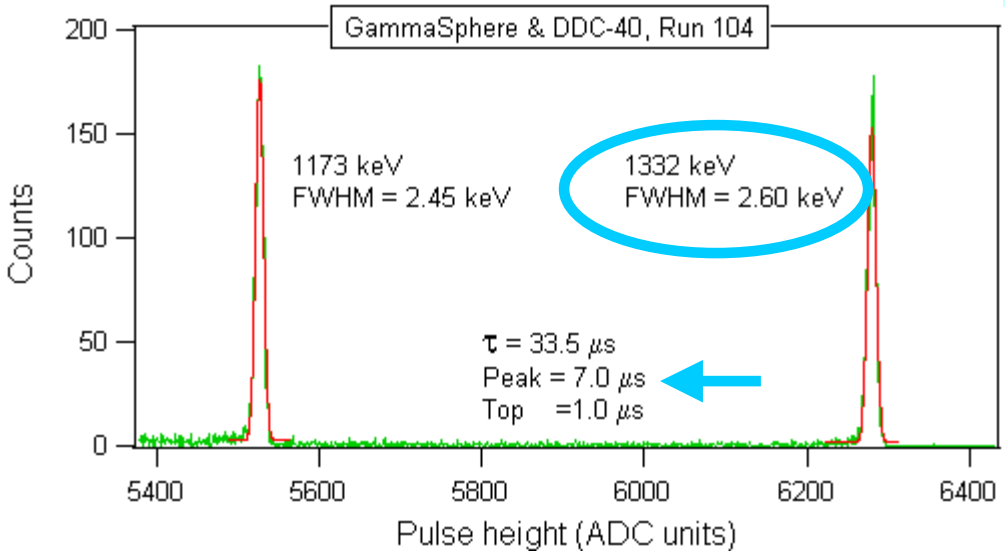
Prototype Installation at ATLAS Counting House

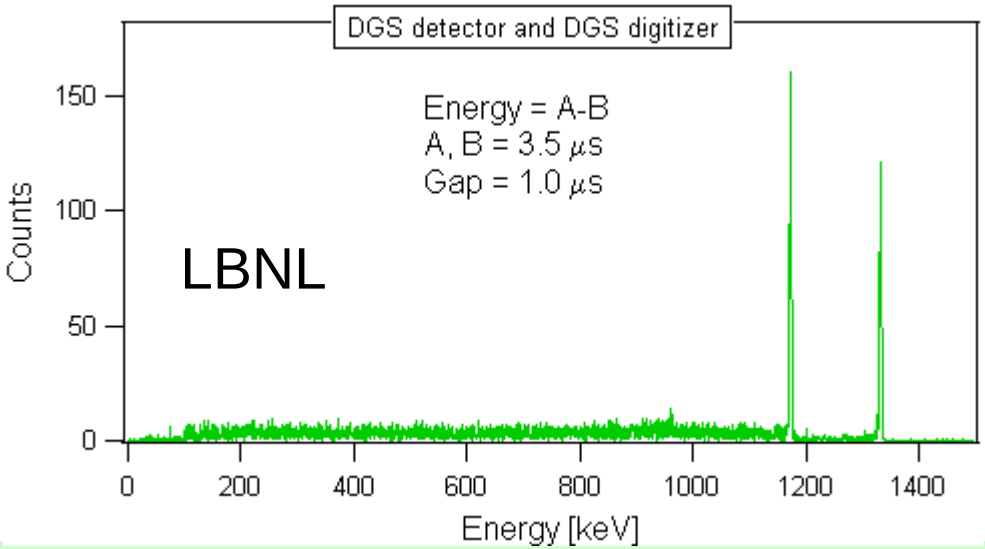
In **Phase I**, DDC-40 was installed alongside the current DGS system. The clock, trigger, and trigger validation were shared between the DGS and DDC-40, using LEMO cables. The two systems could collect **the same events** with synchronized time stamps.

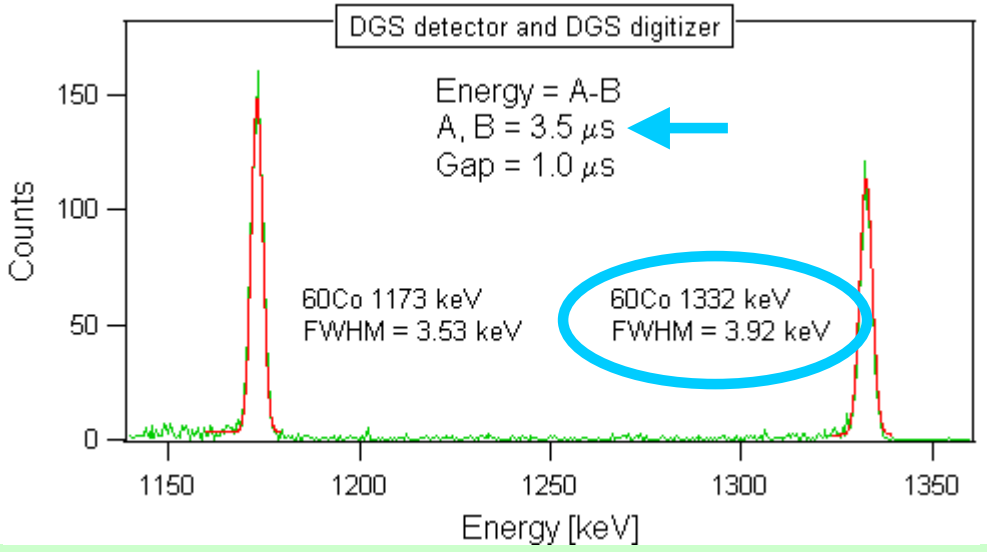
Phase I Was a Great Success

- Comparing the energy resolution with Co-60 and Gammasphere --> **PASS**!
- In offline analysis our digitizer achieved a SQRT(2) better resolution than the LBNL digitizer, because we could apply 2 * *longer running sums* to offline waveforms. With equal sums, the resolution is the same.









Phase II Project

Phase II Project

The challenge: How to actually use the digitizer within the established environment?

How can the digitizers be **interfaced with** and **integrated into** the established GRETINA or DGS environments which are providing clock, trigger, and time stamp synchronization among many digitizers and logic modules?

How this problem or situation was addressed.

We proposed a **modification** of our digital DAQ modules, replacing the VME readout with **gigabit Ethernet** of two variants: 1G and 10G. The on-board Linux will serve for setup and control over Ethernet. The control and the readout are thus separated. The modules will be linked with the GRETA / GRETINA / DGS DAQ using the Optical Time and Trigger Control Link (TTCL). Optical TTCL is forward-compatible with **GRETA**.

The development is performed **in collaboration** with the ANL Physics Division.

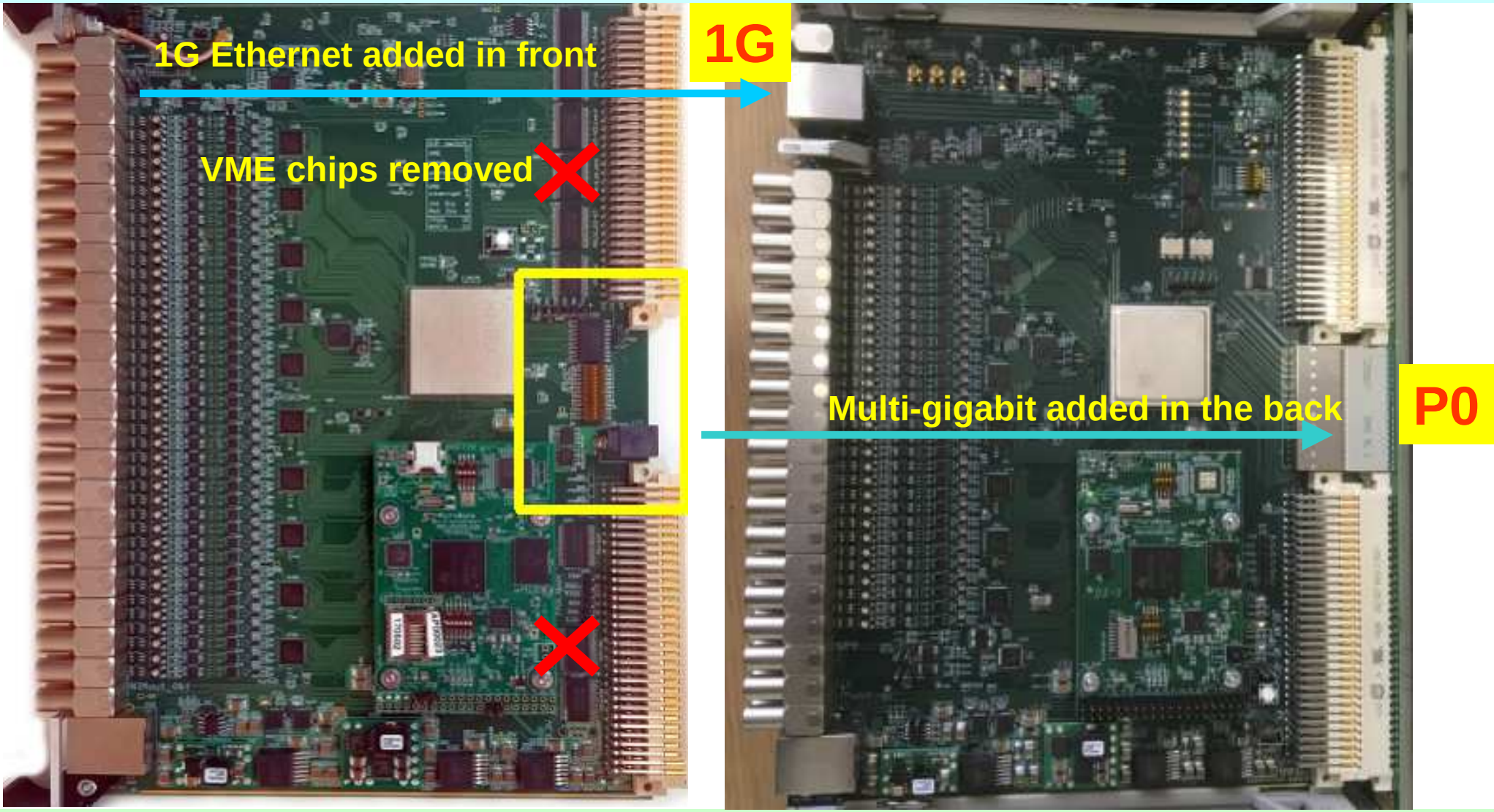
Phase II project.

We are developing the hardware, firmware, and software. We work in close collaboration with the ANL Physics Division.

SkuTek Adding the Fast Data Transfer to the Digitizer

We **removed** the legacy VME chips (marked **X**). We **added** the Hard Metric P0 multi-gigabit connector in the space between P1 and P2. We **also added** a front panel 1G gigabit Ethernet.

The digitizers can be operated in the legacy plain VME crates, and still deliver ~ 110 Mbytes/s per digitizer. The back panel 10G will work in VME64x crates. It will deliver ~ gigabyte per second from every digitizer.



P0 Connector for 10 G Ethernet and TTCL

The Hard Metric P0 is a high-speed, shielded connector with controlled impedance. We routed the high speed Multi Gigabit Transceivers (MGT) and general purpose IO to this connector in order to pass the gigabit traffic to the Rear Transition Board.

Kintex-7

P1 for power

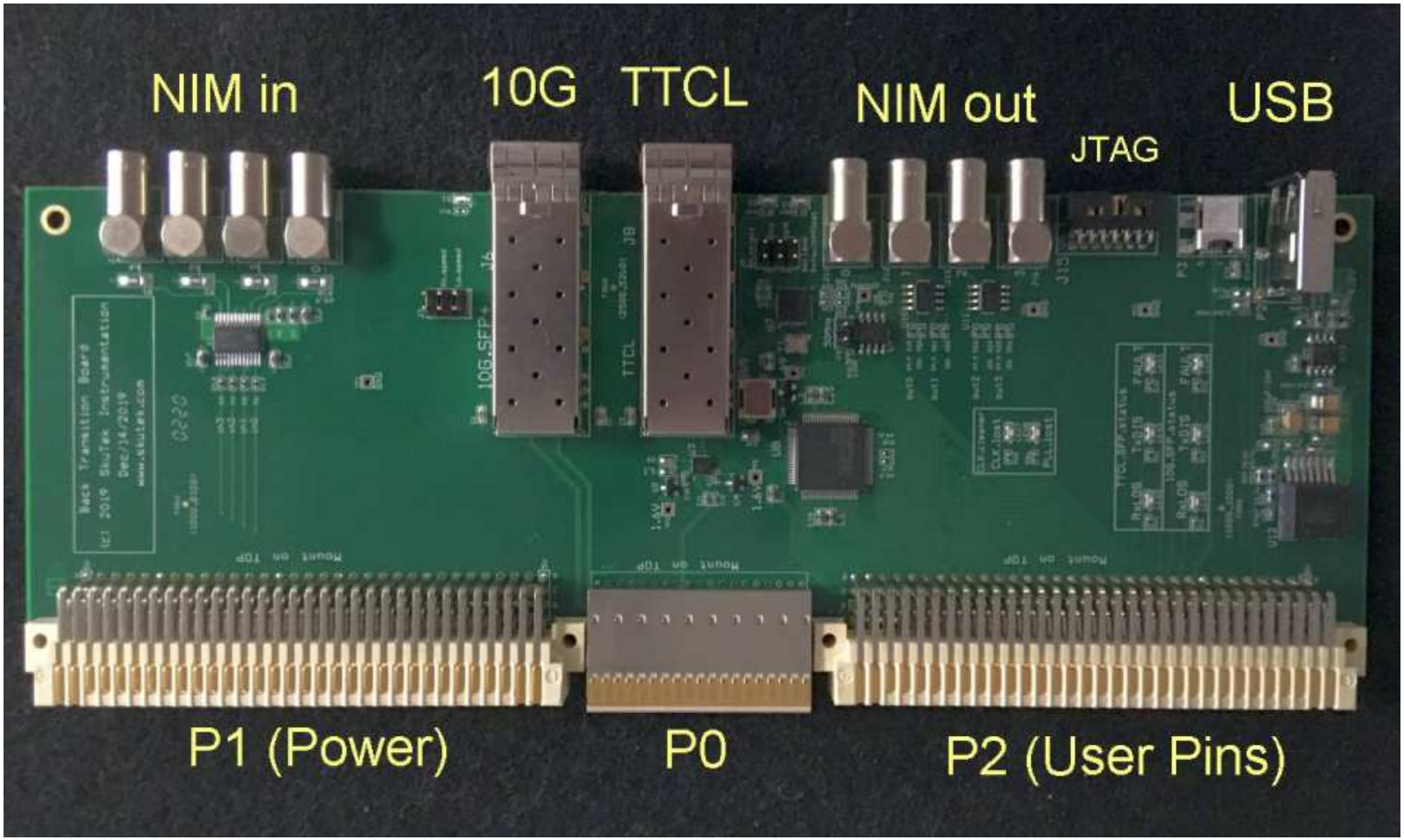
P0 for high speed transfer

Linux computer daughter card

P2 for User Pins

Rear Transition Module with 10 G Ethernet and TTCL

- We developed a Rear Transition Module (in the back of VME64x) with two optical SFP+ modules, the TTCL serializer / deserializer (SerDes), and additional NIM I/O for auxiliary logic.
- The 10G Ethernet will provide for event streaming at ~one gigabyte per second from each digitizer.
- The optical TTCL will be forward-compatible with GRETA.



32-Channel Digitizer With the Rear Transition Module

The Rear Transition Module is plugged into the back of VME64x crate. It reaches the redesigned main board via the low speed P2 User Pins and high speed P0 pins. **Note that the LED's are ON!**

32-Channel Digitizer

Rear Transition Module

1 GbE (FPGA)

Digital HDMI

32 Analog inputs

2 Analog outputs

1 GbE (Linux)

4 * NIM in

10 G Ethernet

Optical TTCL **Compatible with GRETA**

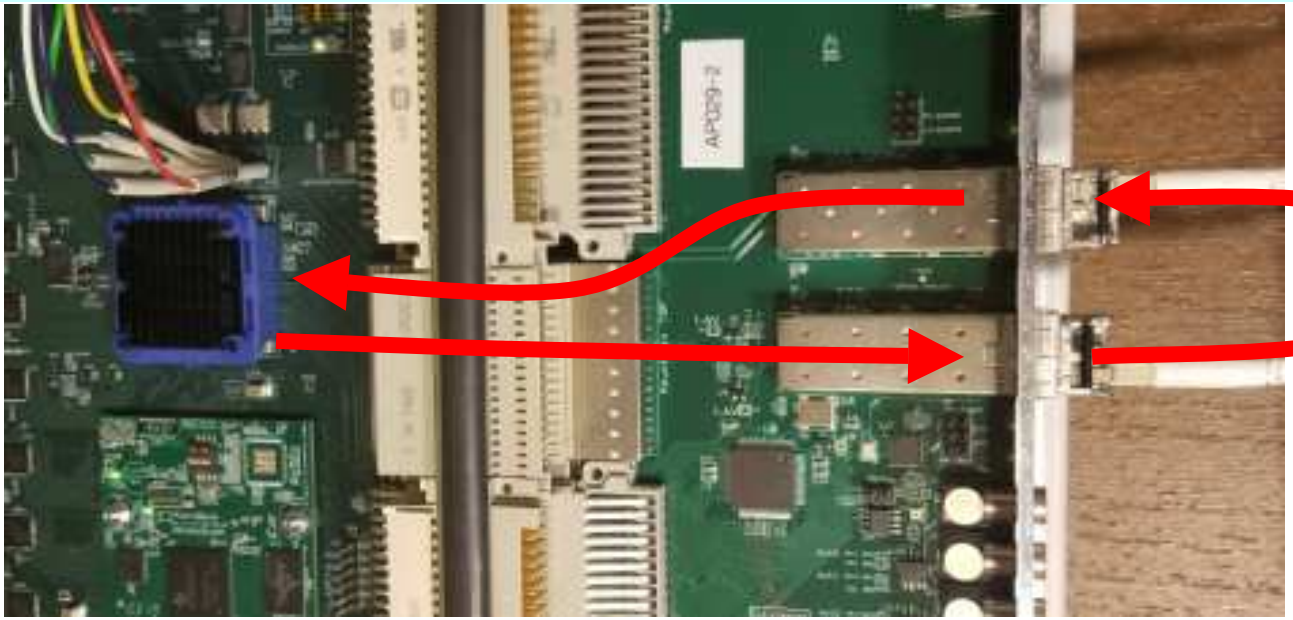
4 * NIM out

USB-2 (Linux)

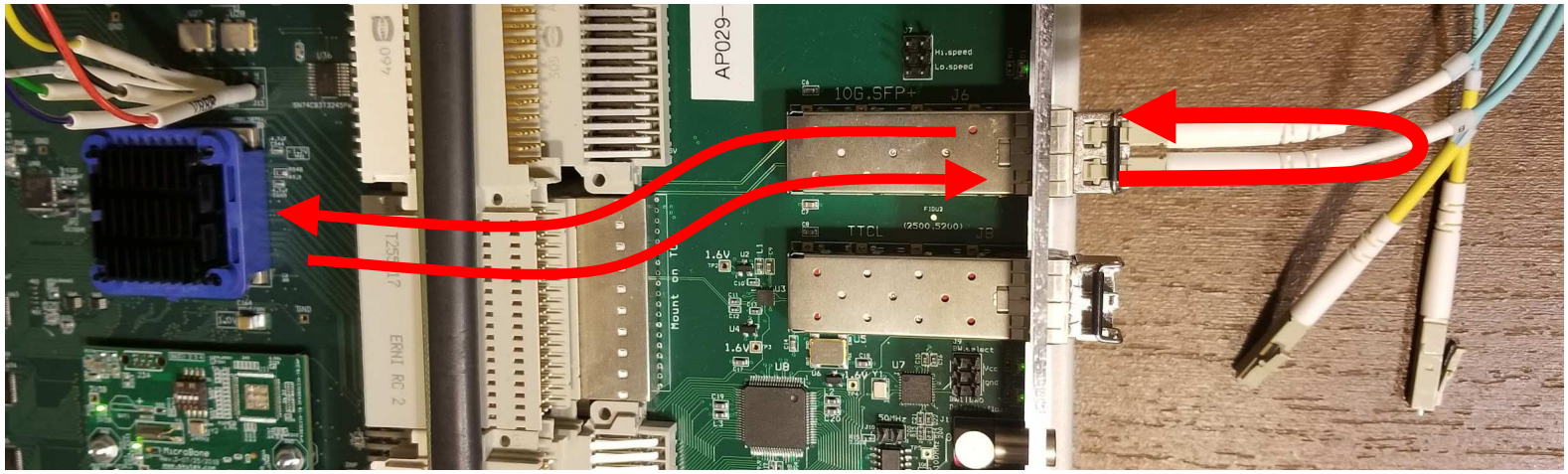
Rear Transition Module Hardware Testing

We tested the loop back throughputs using the optical links. We achieved up to 6.25 Gbps per differential pair. It meets the TTCL requirements, but it falls short of the needed 10G Ethernet.

Remedy: We will switch to the Extended Attachment Unit Interface (XAUI) to address the latter limitation.



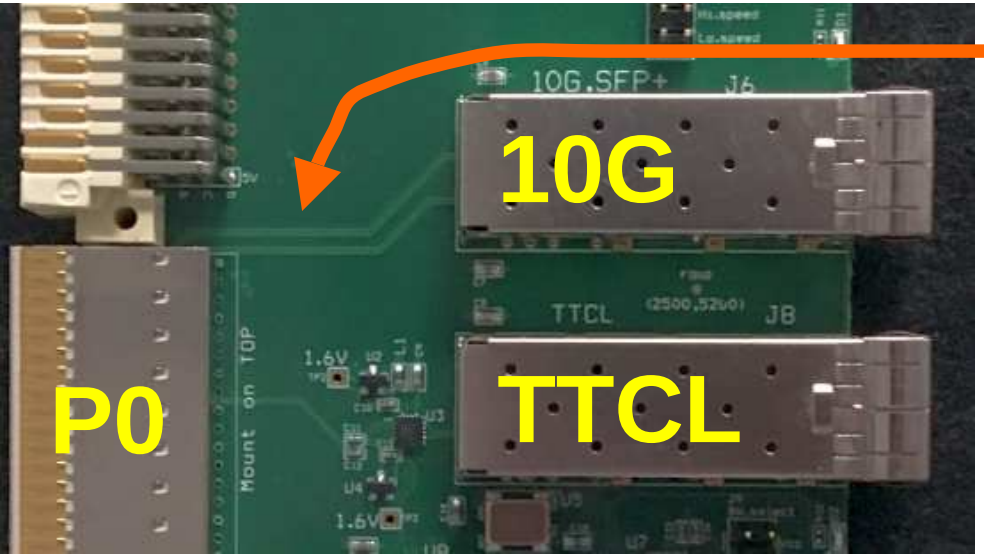
Optical TTCL
Loop back test.
Goal 4 G,
achieved 4 G



10 G Ethernet
Loop back test.
Goal 10 G,
achieved 6.25 G

Rear Transition Module 10 G Hardware Change

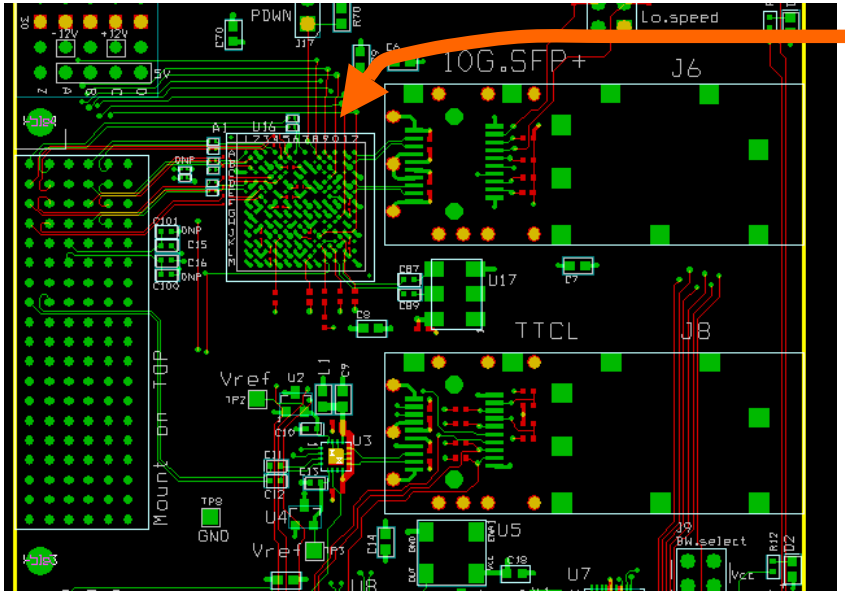
The measured upper speed limit was 6.25 Gbps per one differential pair. Sufficient for the TTCL, but not sufficient for the 10 G Ethernet. **Remedy**: Use XAUI with four differential pairs rather than one.



Revision 0: Direct, too optimistic

Goal 10 G, achieved 6.25 G

Goal 4 G, achieved 4 G



Revision 1: XAUI

Modification: replace 10 G direct with XAUI, which is 4 * 3.125 Gbps.
Modification is marked with an arrow.

The board was shipped on Aug/12

Summary

Summary of Technical Achievements

- **Phase I:** We tested our 40-channel prototype digitizer with HPGe Gammasphere detectors.
  - Pulse height resolution was equivalent to LBNL digitizers.
  - The success led to the Phase **II** collaboration with the ANL.
- The goals of **Phase II:**
  - *Integration* of the digitizers into the digital DAQ used at ATLAS, using the optical Trigger Timing and Control Link (TTCL), *compatible with GRETA* in the future.
  - *Fast readout* using 1G or 10G Ethernet links directly from the digitizers.
  - Setup and ***low latency monitoring*** using the on-board *Linux*, separate from the readout.
  - Develop *Interface Control Documents* for the ANL integration.
  - *Achieve operation* of our prototypes in the ATLAS environment (after the pandemic).
- Achievements:
  - *Redesigned* the digitizer to provide 1G Ethernet in front, and P0 connector for the back.
  - *Developed* the Rear Transition Module with the TTCL and 10G optical links.
  - *Met* the TTCL design throughput @ 4 Gbps, using the optical SFP+ module.
  - *Measured* the maximum throughput of the P0 path @ 6 Gbps per differential pair.
  - *Redesigned* the RTM to use the 10G XAUI interface which works @ 3.125 Gbps per pair.
- The redesigned RTM was shipped on Aug/12/2020. We will test as soon as it arrives.

Future Plans

- Continue development of *firmware* and *software* for our digitizers.
- Develop *readout* over 1G and 10G Gigabit Ethernet.
- Develop *protocols and interfaces* compatible with the ATLAS environment.
  - We are now *working with the ANL* on a series of Interface Control Documents.
- Port the extant *ANL firmware* from the LBNL digitizers to our digitizers.
  - This portion of the project is performed by ANL ATLAS personnel.
- Develop *software interfaces* for setup, control, and monitoring using the on board Linux.
  - *Low-latency* detector and signal *monitoring* with on-board Linux.
- *Achieve operation* of our prototype digitizers in ATLAS environment (after the pandemic).

Highlights of The Final Products

- High density digitizers: **32 channels** per unit, 14 or 16 bits @ 100 MSPS.
- **Low noise design**: RMS about 160 microvolts, that is ~ 1.3 LSB @ 14 bits.
  - Tested and proven with LUX-Zeplin Dark Matter Search detector (10 ton liquid xenon).
  - We delivered 1,632 channels to LZ, no bad channels.
- **Future-proof design**. Protocol and readout on the rear board, whose modification is easy.
- Compatible with **Digital Gammasphere / GRETINA / GRETA** infrastructure.
  - Timing and Trigger Control Link (TTCL) is connected to each digitizer via the RTM.
- Individual UDP Ethernet **readout from each digitizer**, directly from the FPGA.
  - Front-panel 1 G Ethernet tested and working (~ 110 megabytes / second per digitizer).
  - Rear-panel 10 G Ethernet is under development. We expect a Gbyte/s per digitizer.
- Setup and **low-latency monitoring** with on-board Linux Single Board Computer (SBC).
  - Linux SBC can perform readout at the rate ~ a few megabytes per second.
  - Linux SBC can write formatted event files directly to NFS mounted disks.
- A **variety of options** for the control software and GUI executed by the Linux SBC.
  - SSH, command line, Python, Jupyter, and Remote Python Call (RPyC).
  - JavaScript GUI compatible with any browser, any host platform (even a cell phone).
    - Software will be described tomorrow in greater detail.

Acknowledgements

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Special thanks to Michelle Shinn and Manouchehr Farkhondeh

Backup slides

Kintex-7 Provides More Resources Than Legacy Spartan-3

Kintex-7: **5x** more logic and memory

- **Spartan-3** was the best tradeoff between price and performance circa fifteen years ago.
- The new **Kintex-7** FPGAs now offers more digital resources at a reasonable cost.

Feature	LBNL digitizer XC3S5000 Spartan-3 a)	New SkuTek digitizer XC7K410T Kintex-7 b)	Improvement relative to XC3S5000
Equivalent logic cells from Data Sheet	74,880	406,720	5.4
Equivalent logic cells per channel	7.5 k	12.7 k	1.7
Multiply-accumulate units	104 c)	1540	14.8
Waveform memory (k samples) d)	104 k	1,590 k	15.3
Waveform memory per chan (k samples)	10.4 k (10 chan)	49.7 k (32 chan)	4.8
DigiKey price (900 balls) e)	$284	$1,933	6.8
$$ per channel f)	$28 (10 chan)	$60 (32 chan)	2.1

a) XC3S5000 is used in present GRETINA digitizers.

c) These Kintex-7 chips are used in our high density digitizers (both the 32 and 40 channels).

c) XC3S5000 provides multipliers without the built-in accumulate register.

d) Total number of block RAM bits divided by 18.

e) There are some variations of the price depending on the speed grades. We chose the most relevant speed variants, 5C and 2C, respectively. The details are explained in the respective Data Sheets.

f) Approximate FPGA cost per channel for 10 channels (Spartan-3) or 32 channels (Kintex-7).

Digitizer Hardware Diagram

VME chips were removed. Setup and control are exercised with Linux Single Board Computer (which is also a SkuTek product). We developed the Rear Transition Module with components aiming at system integration: 10G Ethernet, NIM in and out, and the ANL Trigger and Timing Control Link (TTCL).

The Fast Serial Link using HDMI cable is a future option.