12-bit 32 Channel 500MSps Low Latency ADC

Award Number: **DE-SC0017213**
Ph II project, Year 2 (under NCE)

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Presentation Outline

Pacific MicroCHIP Corp.

- The Company, Its Specialization/Expertise
- A 12-bit 32 Ch 500MS/s ADC (being developed)
- Relevance to the NP Program
- Project Goals
- Chip Specifications and Architecture
- Comparison to ADCs Available on the Market
- Physical Implementation
- Chip Carrier and Packaging
- Testing Setup and Results
- Project Schedules and Milestones
- Future Plans

The Company

- **Pacific MicroCHIP Corp. was incorporated in 2006.**
- **It is headquartered in Culver City, California.**
- **Main focus of the Company – providing IC/ASIC design services and turnkey solutions.**

Office in Culver City, CA

Our Offerings

Pacific MicroCHIP Corp.

IC/ASIC Design Services:

- **Circuit Design (analog, RF/mixed, digital)**
- **Simulation**
- **Physical Design**
- **Chip Assembly**

Turnkey Solutions:

- **IC Design**
- **Chip Fabrication Logistics**
- **Package Development (involving a 3rd party)**
- **Chip Packaging (involving a 3rd party)**
- **PCB Development for Testing/Eval. (involving a 3rd party)**
- **Testing/Characterization (an in-house lab)**
- **Delivery of Chips, Parts and Board Level Solutions**

Relevance to the NP Program

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NP detectors require thousands of signal processing channels =>

need for digitizers to:

- **Shrink in size – our ASIC combines 32 independent ADCs per chip.**
- **Reduce power consumption – expected 25mW / ADC (w/o JESD buffers).**
- **Reduce wire congestion – our ADCs have a serial interface that can be shared between 2 or 4 ADCs**

Upgrades in these systems demand for:

- **Digitizing accuracy - our ADC features 12-bit resolution.**
- **Adequate sampling speed - our ADC features up to 0.5GS/s.**
- **Low conversion latency - we offer 8ns.**

Targeted specific applications:

- **Low latency particle beam control systems.**
- **Imaging and spectroscopy systems for gamma-ray detectors.**
- **Multichannel detectors based on tube and silicon photo multipliers.**

Project Goals for Phase II

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Within this project we will:

- **Design circuits and layout for the ADC ASIC.**
- **Fabricate the chip.**
- **Develop a special chip carrier.**
- **Package the chips.**
- **Develop a test PCB and a DUT socket.**
- **Develop a GUI and a test bench.**
- **Test and characterize the ADC ASIC.**
- **Prepare a datasheet for marketing.**
- **Submit deliverables to the DoE.**

12-bit 32 Channel 500MSps Low Latency ADC

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Specifications (expected performance):

- 32 independently operated ADC channels
- 500 MS/s sampling rate
- 0.6Vpp differential input swing
- 10-bit ENOB
- 250MHz input signal bandwidth
- -40C..+125C temperature range
- 25mW/channel power consumption (with interface)
- JESD204B output data interface
- 8ns latency (direct ADC data output mode)
- 32x8Gb/s output data rate
- I2C interface for ASIC control
- 7.7mm^2 ASIC layout footprint
- A solder bumped die in a BGA package
- 28nm CMOS technology

12-bit 32 Channel 500MSps Low Latency ADC

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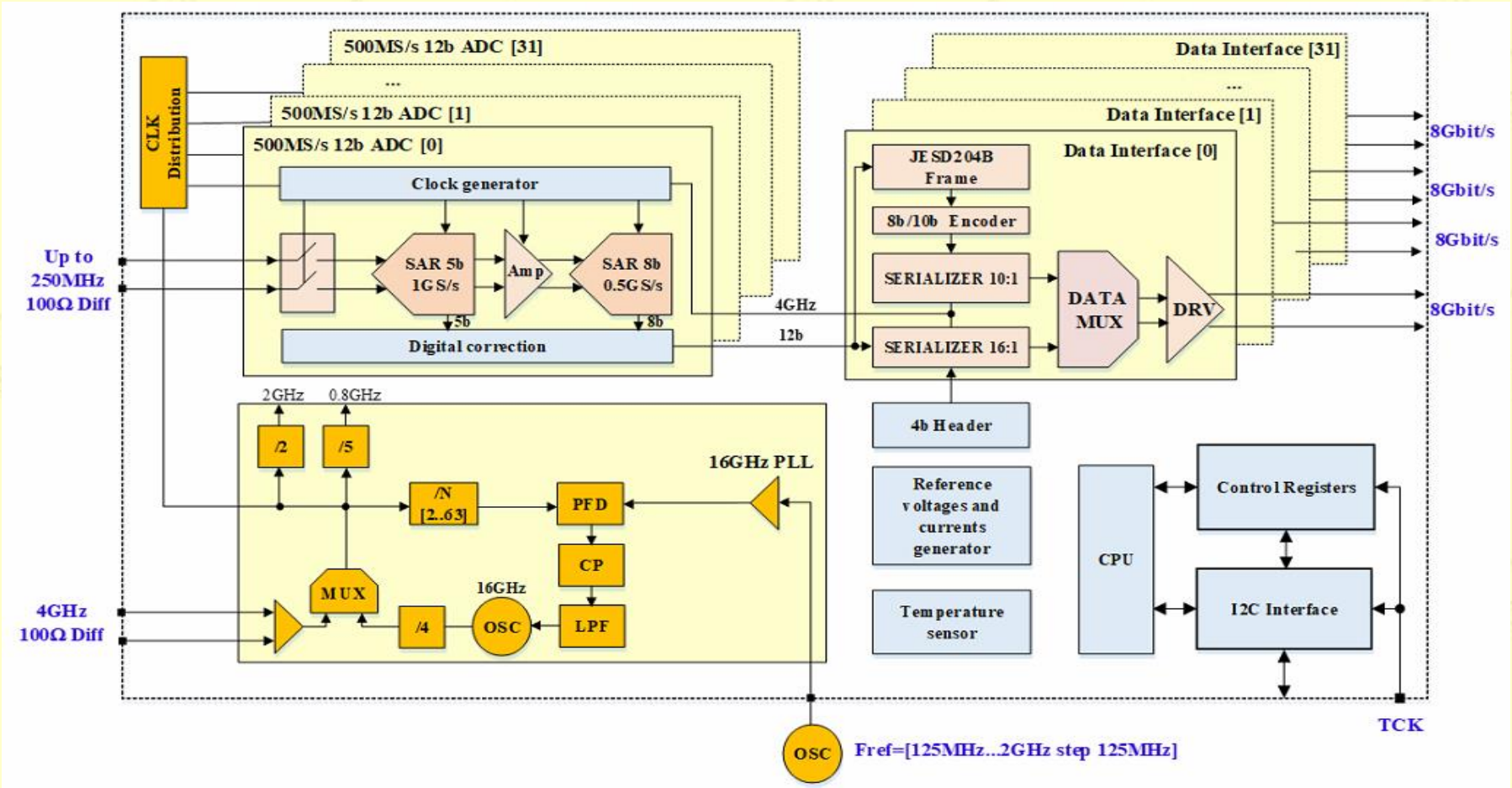
ASIC Block Diagram



12-bit 500MSps ADC Core

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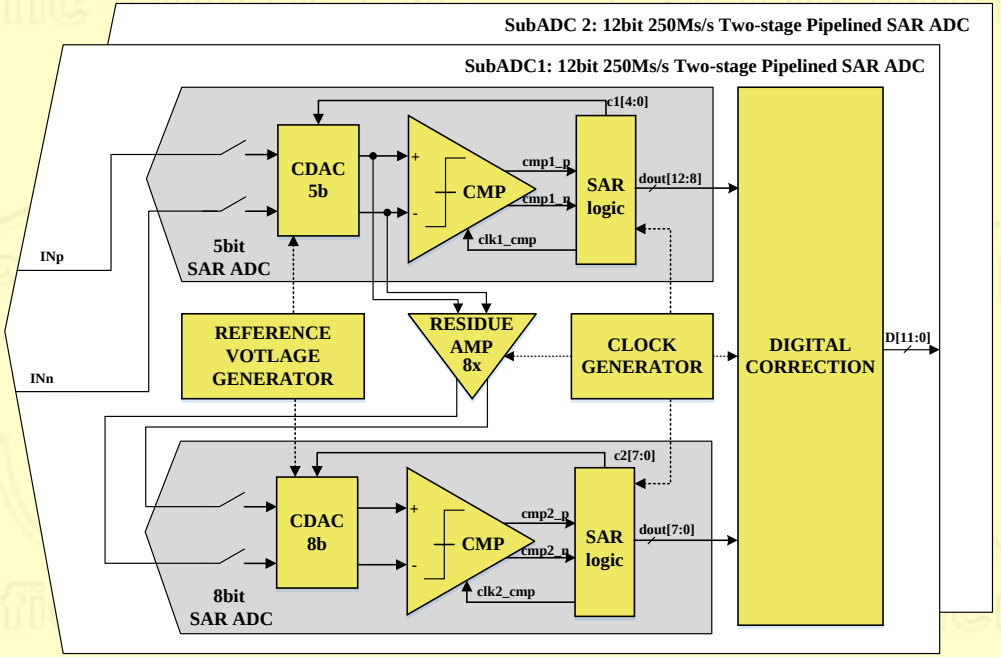
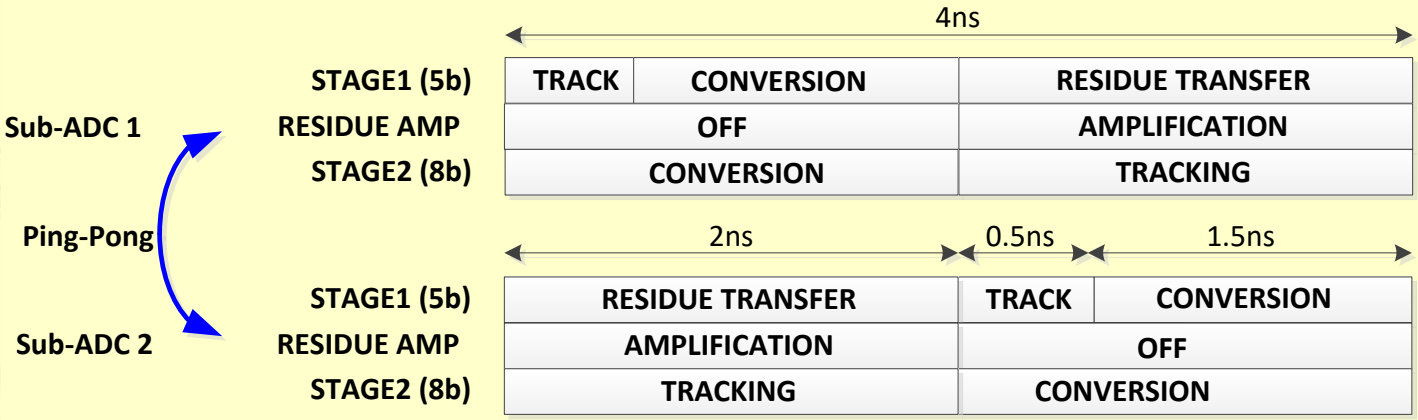
- Two-times time-interleaved ADC core
- Sampling clock skew adjustment
- Two-stage pipelined SAR architecture
- Programmable residue amplifier gain
- Programmable ADC FS range
- Bootstrapped input switches
- 1-bit redundancy between ADC stages





12-bit 32 Channel 500MSps Low Latency ADC Power Budget

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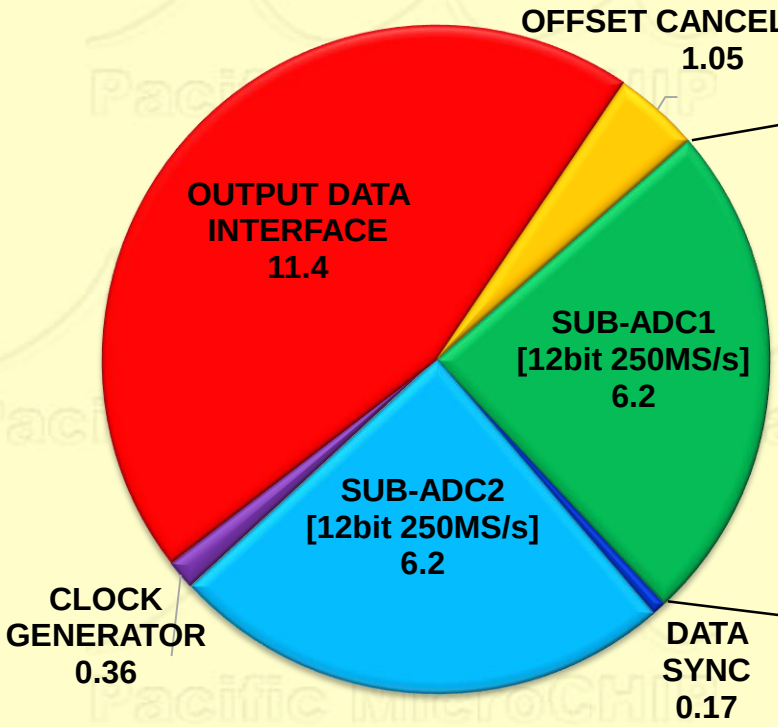
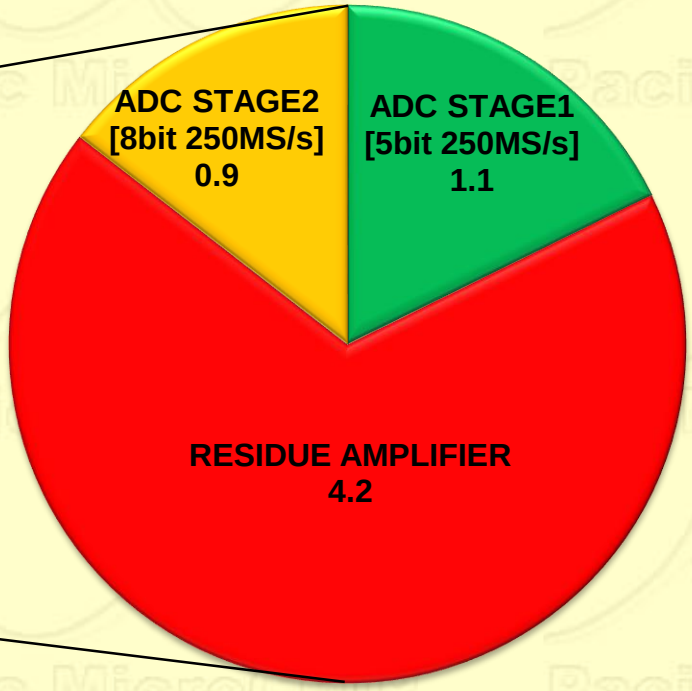
ADC channel power budget, 25mW



Sub-ADC power budget, 6.2mW



Comparison to ADCs Available on the Market

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#	Vendor	# of Channels	Sample Rate, MS/s	Power Cons. per Channel	Architecture & Latency
1.	TI 12-bit ADS52J90	32	40	41mW	Pipeline 2.5us
2.	TI 12-bit ADS5403IZAYR	1	500	1W	Pipeline 240ns
3.	TI 12-bit ADS54T04IZAYR	2	500	1.15W	Pipeline 240ns
4.	ADI 12-bit AD9234BCPZRL7	2	500	1.5W	Pipeline 240ns
5.	Pacific Microchip Corp. 12-bit*	32	500	25mW	SAR/Pipeline 8ns

* Expected performance

ASIC's Physical Implementation

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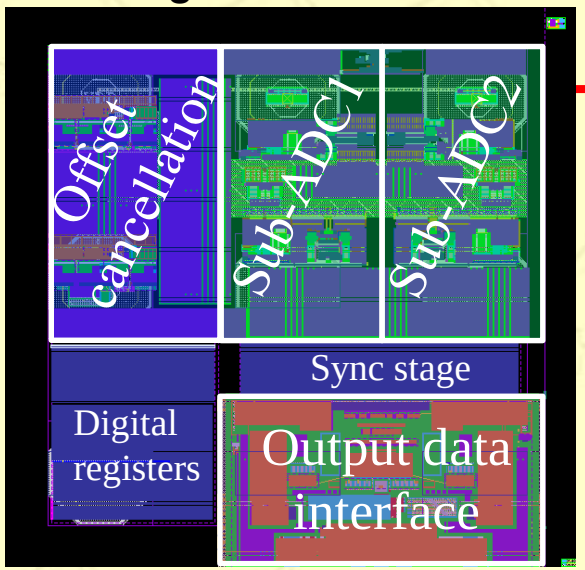
Chip periphery:

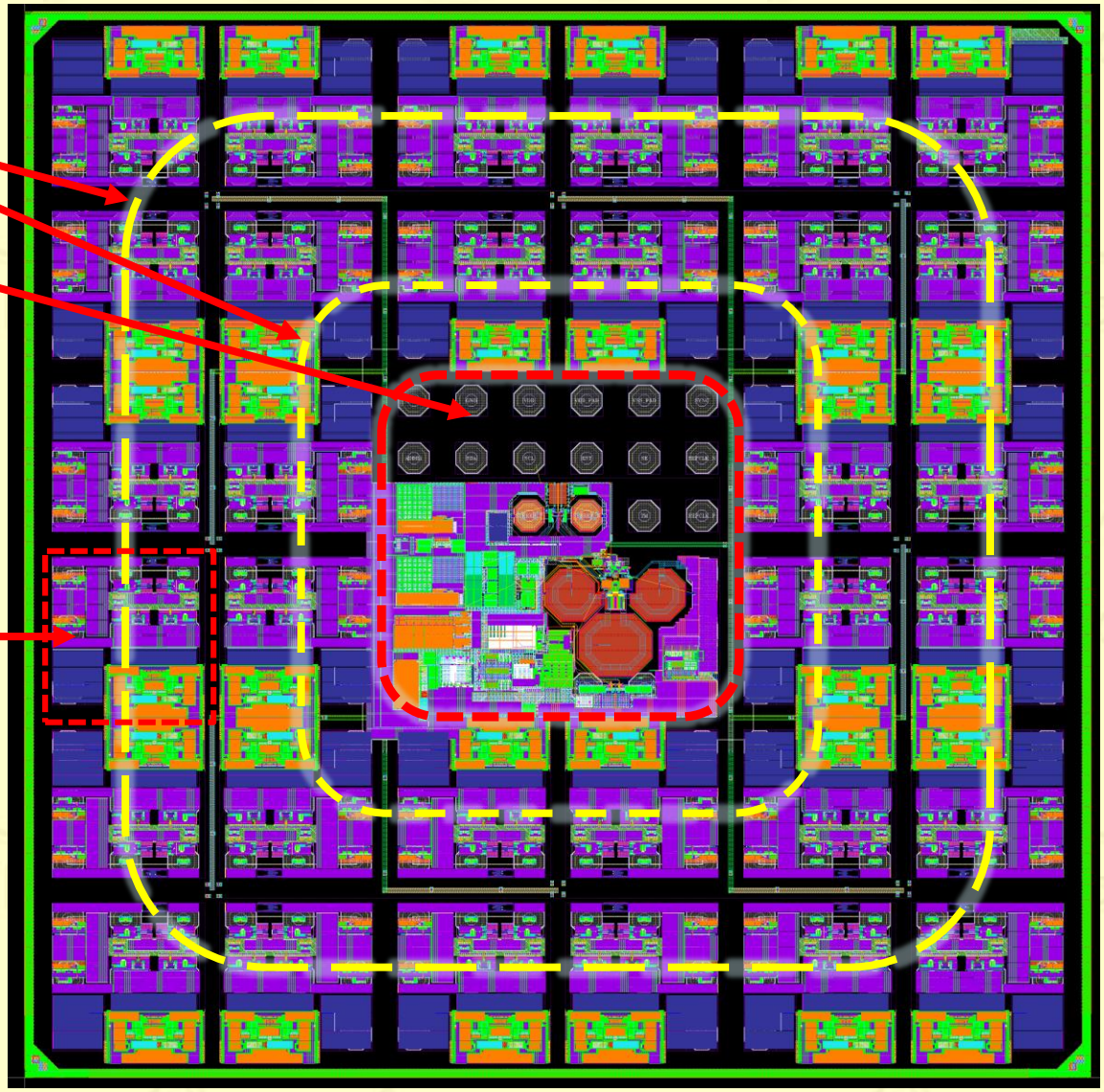
32 independent ADC channels located in 2 circles

Central part:

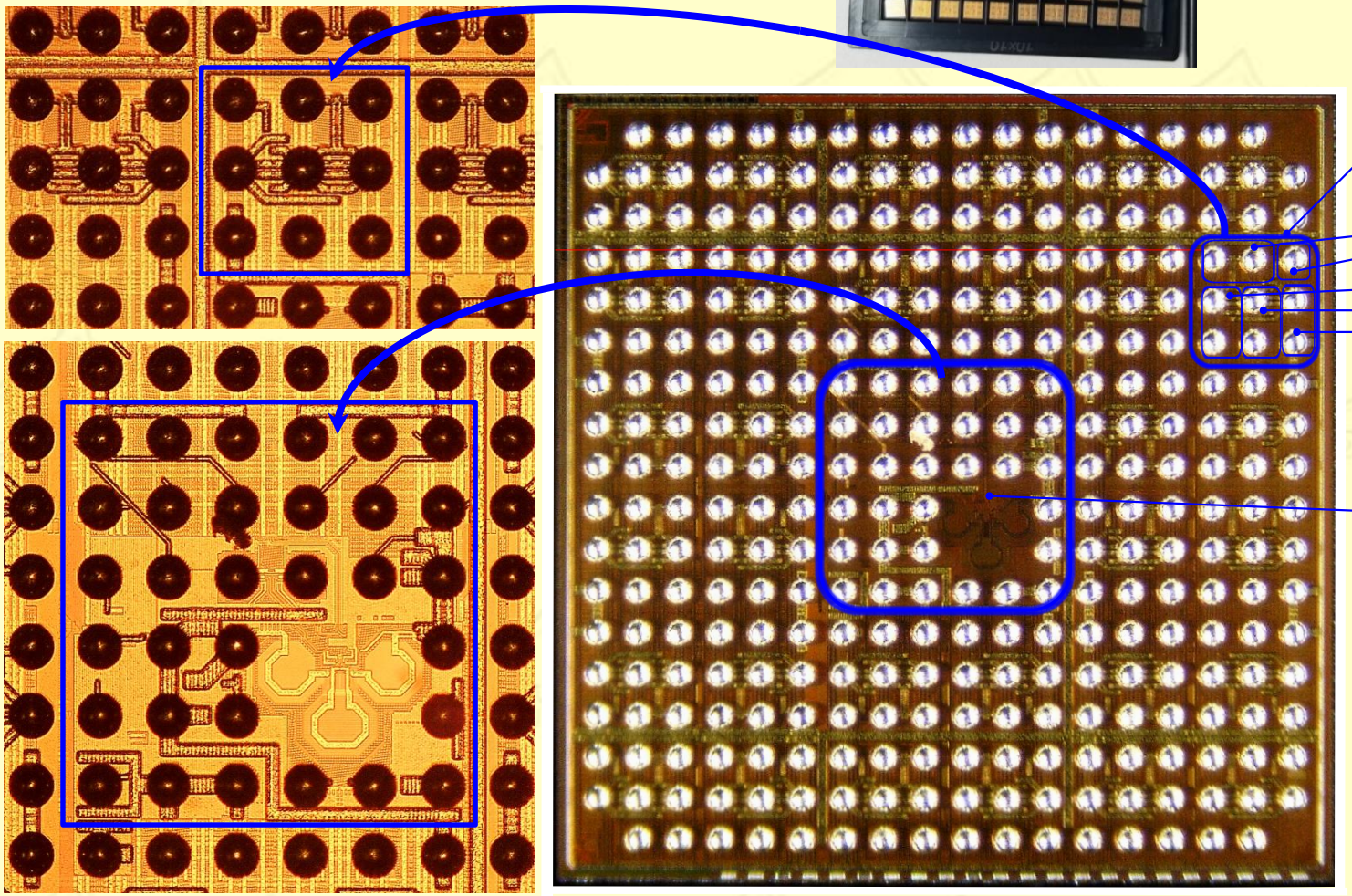
- **PLL with a clock tree**
- **Temperature sensor**
- **CPU for calibration**
- **I2C interface for control**

Single ADC channel





Fabricated Chips

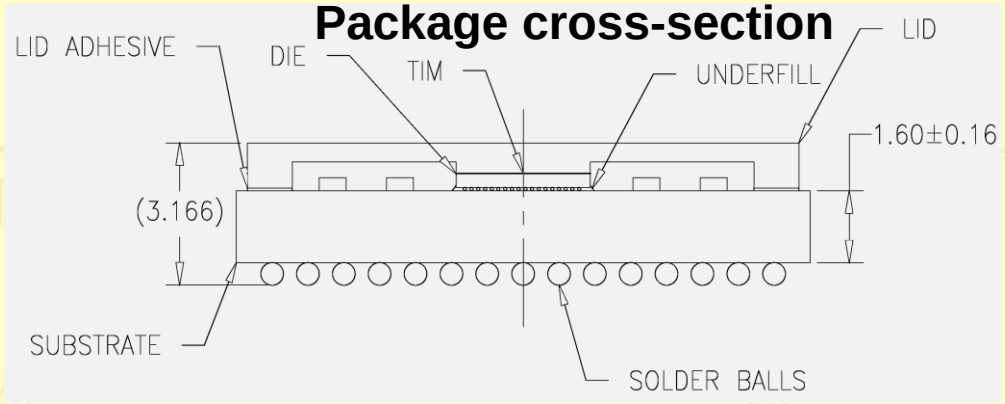


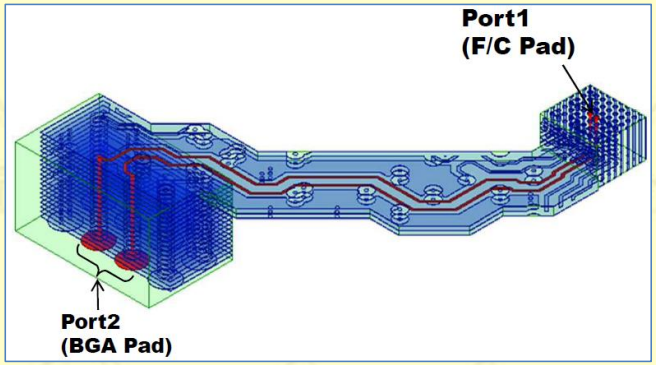
Chip Packaging

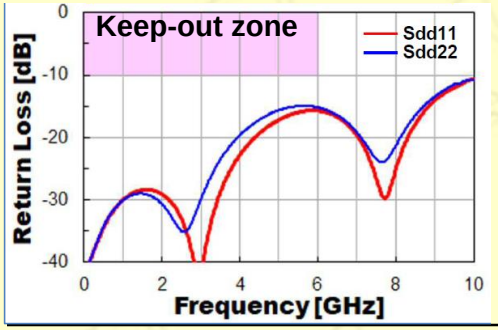
BGA 15.2 x 15.2 mm, 18 x 18 balls, 0.8mm ball pitch

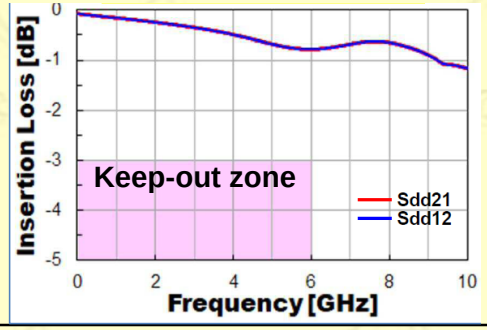
Package Design

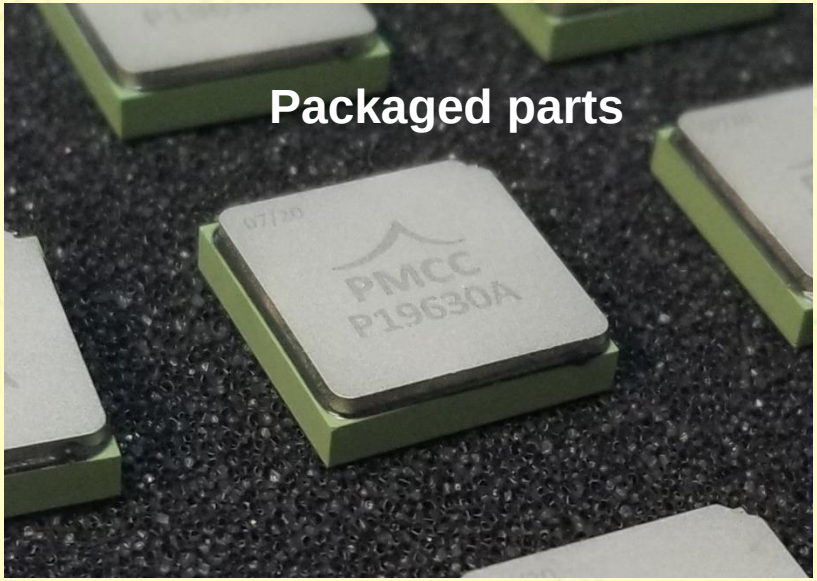
S-parameter simulation results for longest I/O wires:
S11 < -10dB up to 10GHz
S21 > -1dB up to 9GHz











Testing Setup

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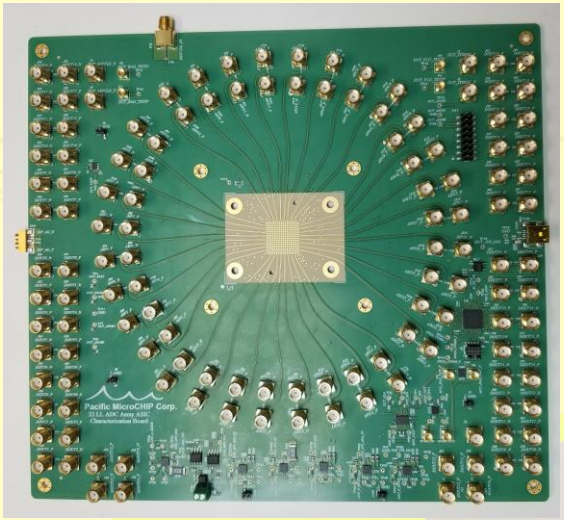
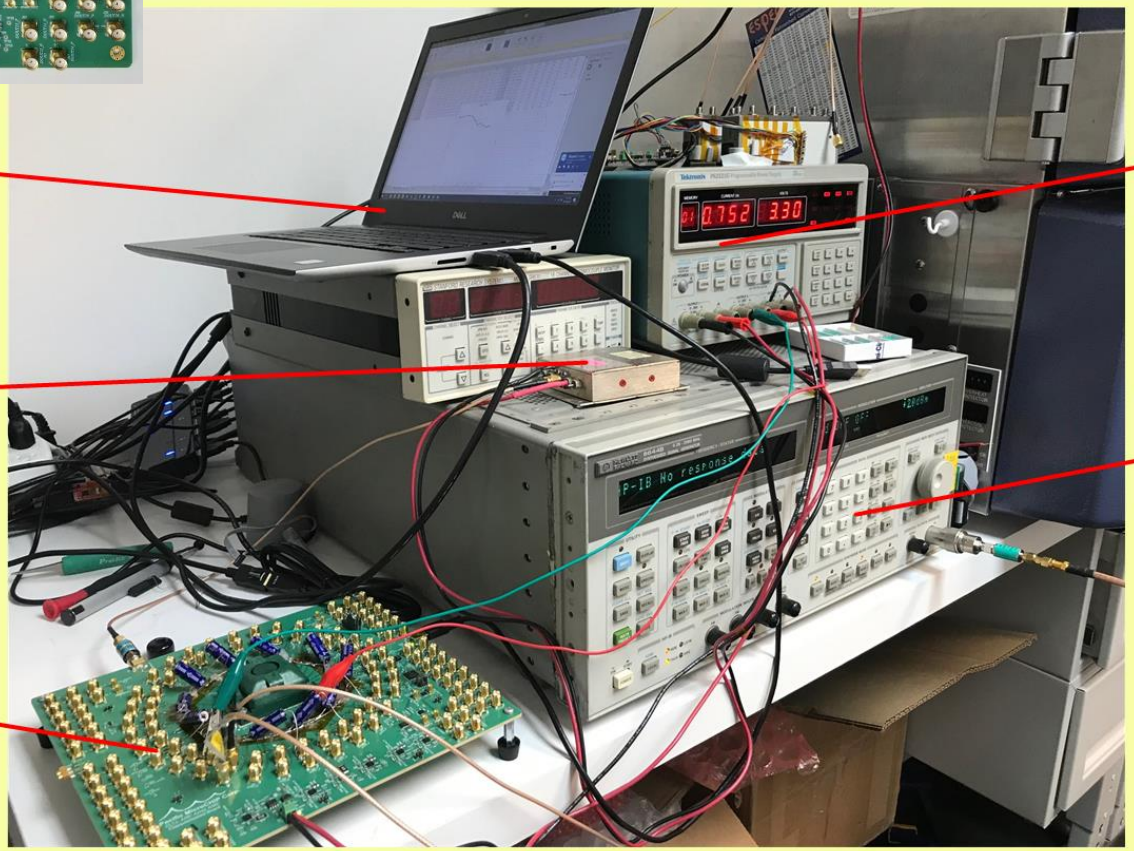


← Test Board

- **Exposed area in the center for DUT socket**
- **32 differential inputs in a circle for delay equalization**
- **32 differential outputs at the PCB's edge (less critical to PCB losses)**



Preliminary Testing Results

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Power Consumption

Supply	V [Volts]	I [mA]	P [mW]
VDDD	0.9	445	400.5
VDD18	1.8	9	16.2
VDDA	0.9	88	79.2
VDD12	1.2	564	676.8
PLL	0.9	60	54.0
Total:			1226.7
Per Channel:			**38.3**

Notes: Power of the JESD204B interface is included. An input signal is applied only to a single ADC out of 32. The VDDD consumption is expected to increase when a signal is applied.

Preliminary Testing Results

PLL Performance

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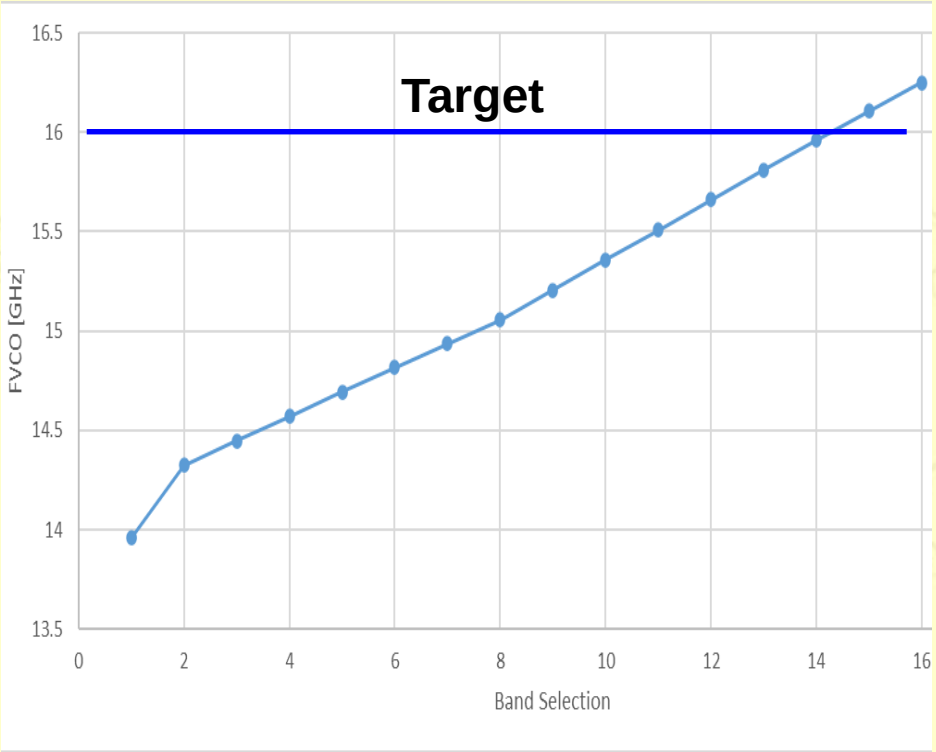
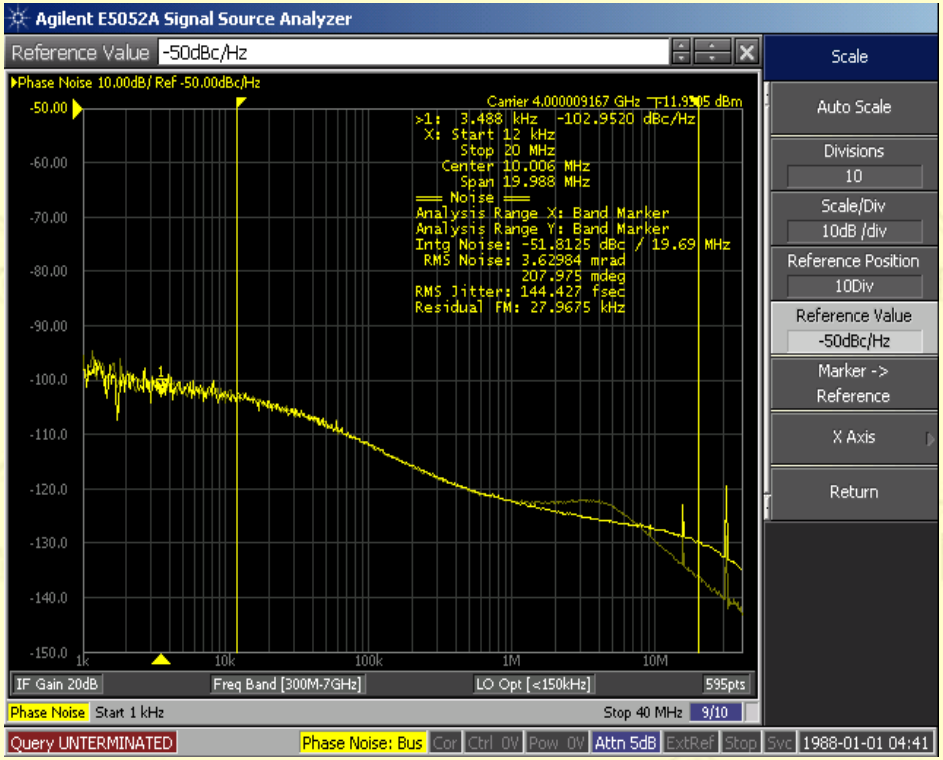
Targeted frequency achieved on the 14th band. It will be tuned up in the 2nd prototype.

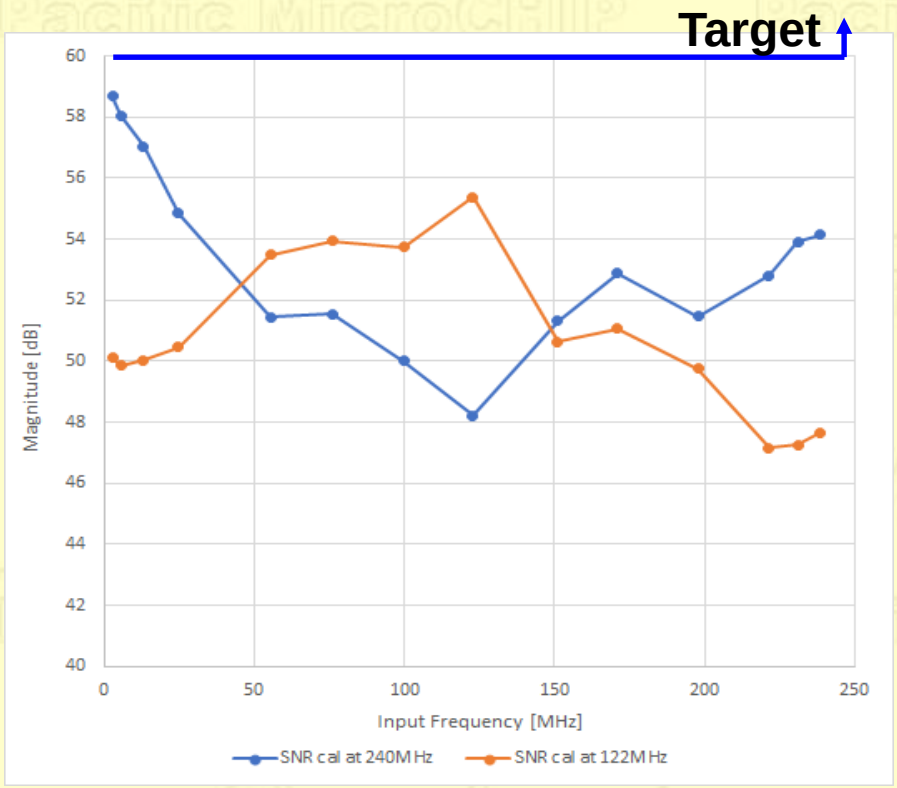
Phase noise tested at 16GHz/4. 144fs RMS jitter (12K-20MHz range). Jitter does not depend significantly on PLL BW.

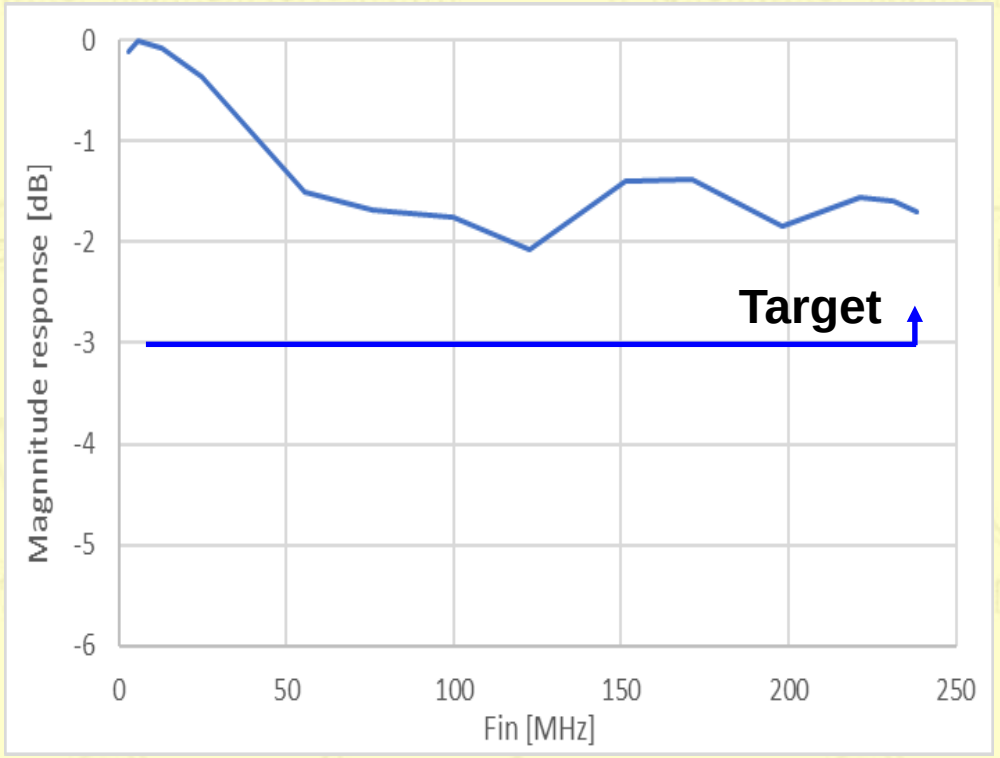




Preliminary Testing Results

ADC Performance





ENOB vs. Input signal frequency.
When ADC is calibrated at 240MHz:
9.5 ENOB @ 5MHz
7.2 ENOB @ 250MHz (Nyquist)
When ADC is calibrated at 122MHz:
8.5 ENOB @ 122MHz

Project Schedule

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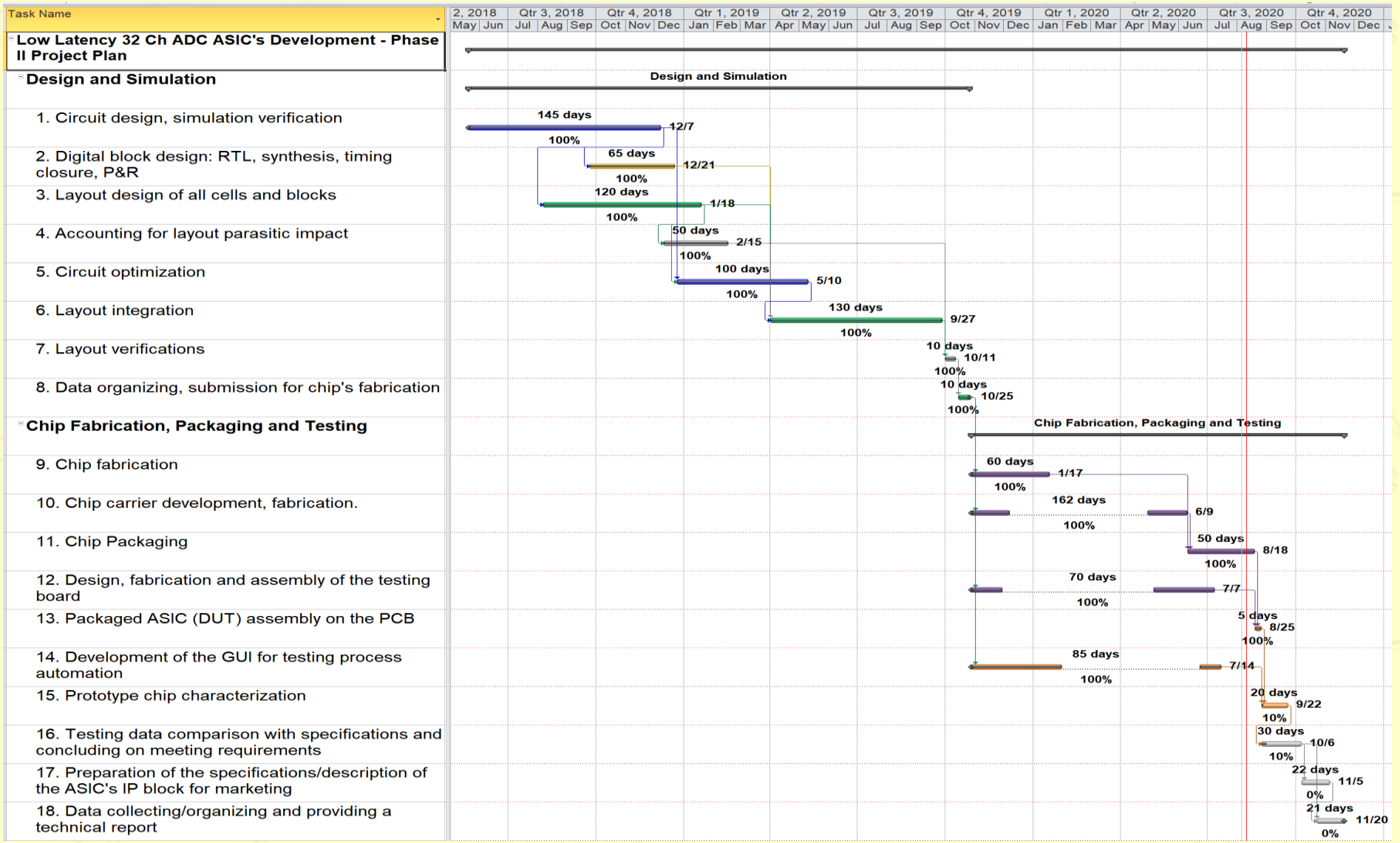

Future Plans

- **Finish testing the chip's 1st prototype (End of Ph II).**
- **Transition to Phase IIA – to redesign the chip, increase its performance, fix issues identified during testing.**
- **Fabricate the final chip.**
- **Test/evaluate it.**
- **Prepare the chip description and datasheets.**
- **Organize the ADC ASIC design as an IP block and advertise it.**
- **Provide the chip to the DoE community and commercial customers.**

We would appreciate any application ideas and customer leads for the presented 32ch ADC ！

THANK YOU !