# Distributed digital data acquisition system with network time synchronization

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*Phase I: 2017-2018, Phase II: 2018 – 2020 (2022)*

# Contents

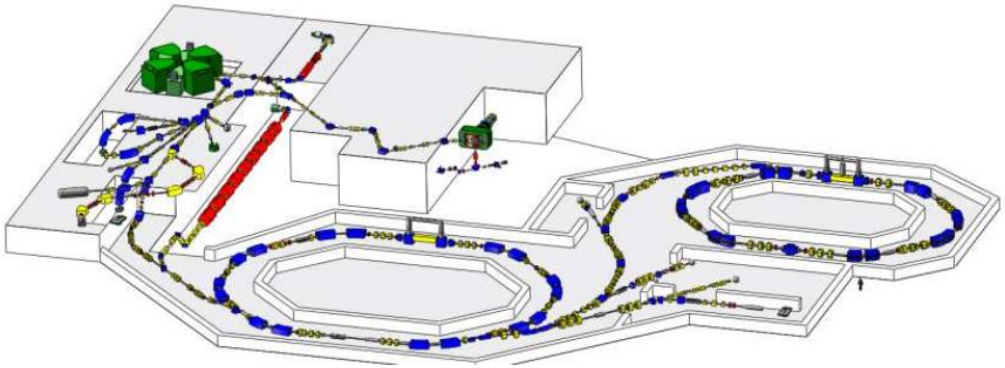
# Distributed digital data acquisition system with network time synchronization

## Motivation

Large nuclear physics experiments often use physically separated radiation detectors

Electronics to read out detectors must be synchronized to 100ns-100ps, ideally <10ps

Traditionally use dedicated clock and trigger cables for synchronization ☹



XIA has been developing digital data acquisition electronics for radiation detector applications for over 20 years


Modern technologies allow time synchronization through data network

**New DAQ electronics with White Rabbit / PTP synchronization**

# Motivation

## XIA SBIR Project Goals

- Adapt IEEE 1588 Precision Time Protocol technologies to XIA's detector readout DAQ modules for clocking and develop a "software triggering" concept
- Stay within standards, use open HW/SW environment, remain compatible

⇒ Phase I: Standard PTP (1588-2008) and Synchronous Ethernet
achieved tens of ns precision

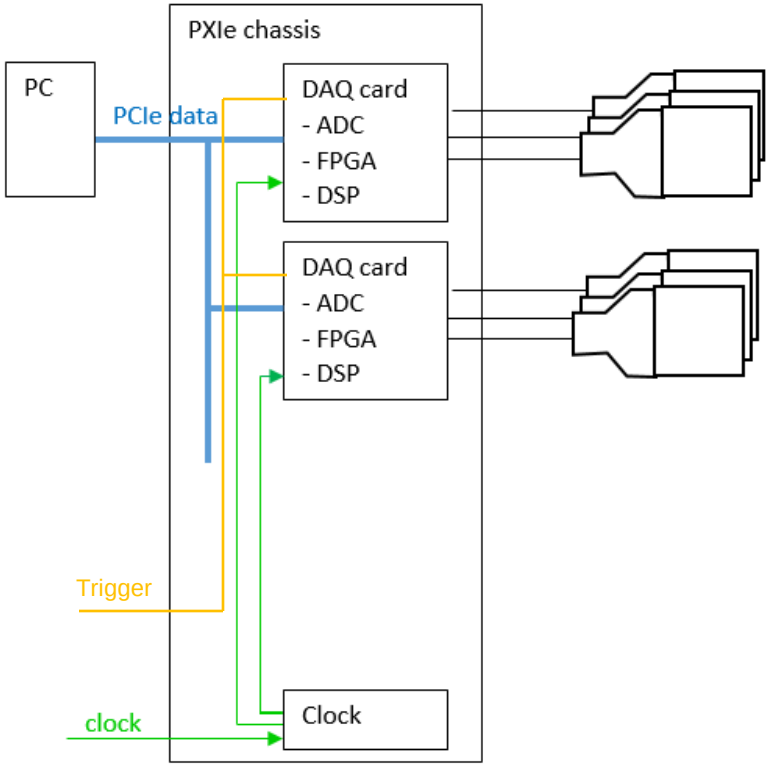
⇒ Phase II: White Rabbit (now 1588-2019 high accuracy profile) "WR"

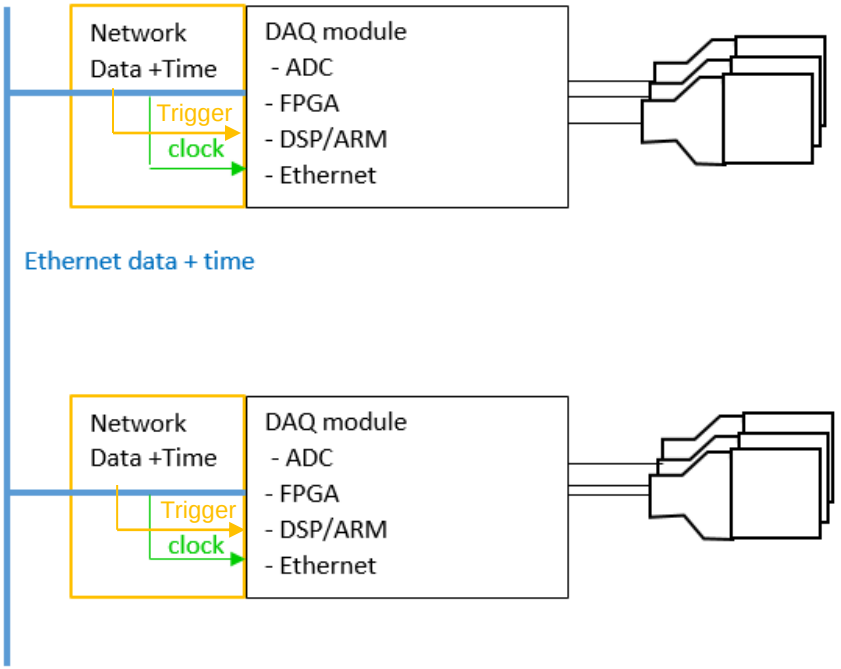
Requirements for timing precision depends on experiment

- Background reduction by coincidence: Hundreds of nanoseconds
- Event building for detector arrays: Tens of nanoseconds
- Time of flight measurements: Sub-nanosecond
- Goal in SBIR topics: "10 ns"; "1 ns or better"

**=> "useable" if better than 1 ns**

# Detector Readout Electronics Synchronized Through Ethernet Network Timing Techniques




## *Traditional*

Crate with data I/O to host PC and backplane clock/trigger distribution

**Tag detector data with backplane clock (48bit)**

## *This Project*

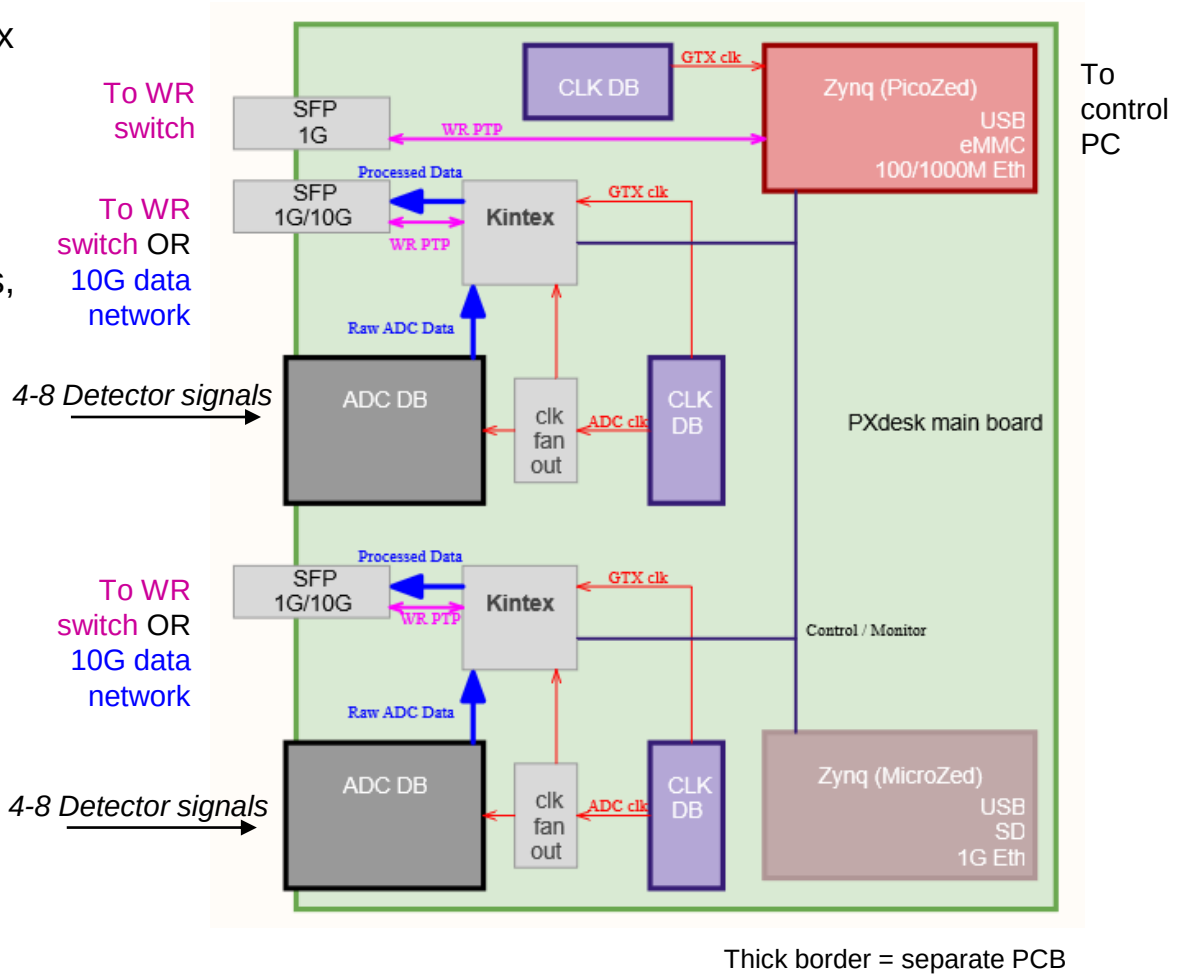
Independent modules with network data, derived clock, and “software trigger”

**Tag detector data with UTC-related timestamps (date/time to ns precision)**

# Distributed digital data acquisition system with network time synchronization

## Phase II DAQ hardware: Pixie-Net XL (PXdesk), Revision B

- Pulse processor board using Kintex 7 FPGA
- Zynq controller board (Linux) for control/monitor.
- ADC daughtercards for detector readout (flexibility in ADC channels, rate, precision, or non-ADC functions)
- High speed data flow from ADC to FPGA to Ethernet output
- Rev. B updates:
  - WR clocking circuitry on DB
  - WR option for Zynq
  - Rogers PCB material for 10G




**Goals for this module:**

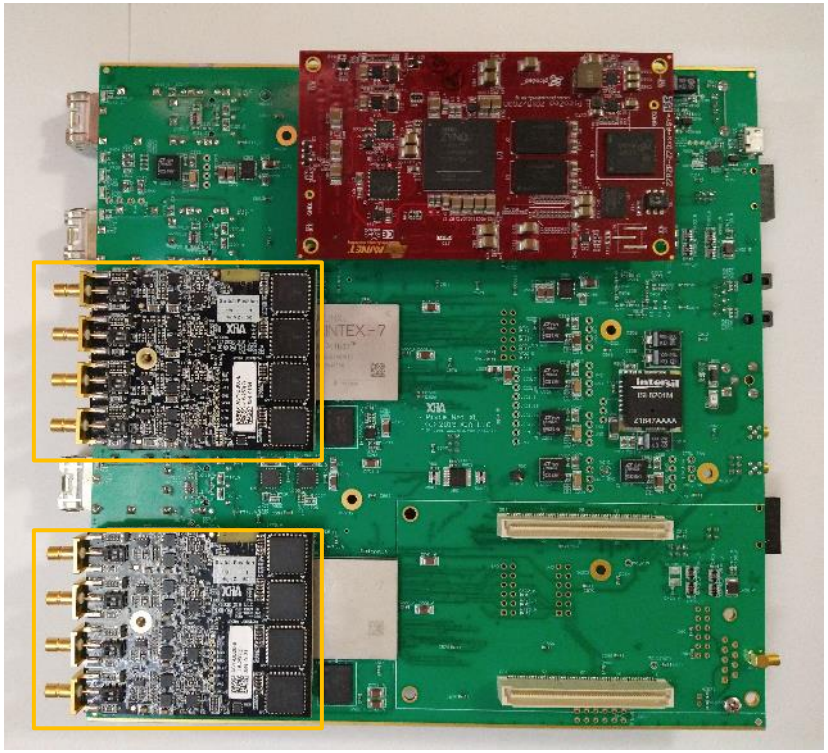
**<100ps timing resolution**

**10G Ethernet … ready for a 10G WR switch**

**High rate pulse processing**

# Distributed digital data acquisition system with network time synchronization

## Prototypes built so far



Main board with ADC daughtercards (black) and Zynq controller module (red).

### Daughtercards

**DB01**:
4-channel,
12-**14**bit, 75-**125** MSPS ADCs
variable gain/offset, uses ¼ of the I/O pins

**DB02**:
8-channel,
**12**-14bit, **250** MSPS ADCs
fixed gain/offset, differential inputs

**DB06**:
4-channel,
**16**bit, **250** MSPS or 14bit, 500 MSPS ADCs
2 gains, variable offset

**DB04**:
8-channel,
12-**14**bit, **250** MSPS ADCs
fixed gain, variable offset, microcoax inputs

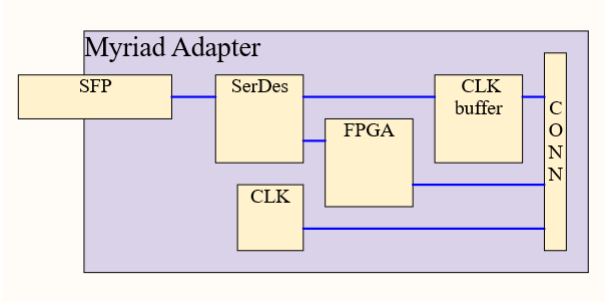
## Clocking and Synchronization

Rev B boards move WR clocking circuitry to a daughtercard to accommodate different modes of operation for ADC and Ethernet:

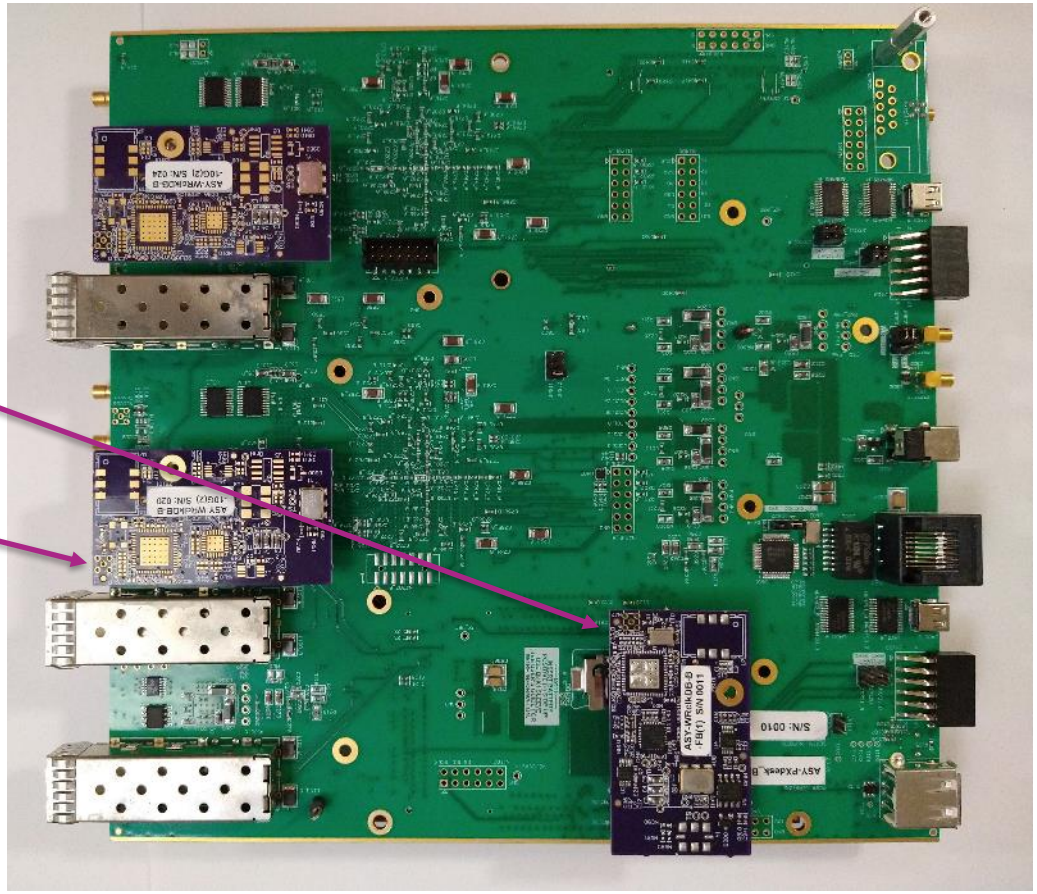
1. **WRclkDB (1G)**:
   WR voltage controlled oscillators, DACs, PROMs
   125 MHz for 1G Ethernet (and ADC)
   option for “low jitter DB” circuitry

2. **WRclkDB (10G)**
   Simple fixed oscillator, no WR sync
   156.25 MHz for 10G Ethernet

3. **Myriad Adapter**:
   SFP and SerDes TTCL to decode Myriad I/O
   Compatibility for DGS, Greta, etc
   “Myriad clock” for ADC
   Separate 156.25 MHz for 10G Ethernet
   (collaboration with ANL, in progress)



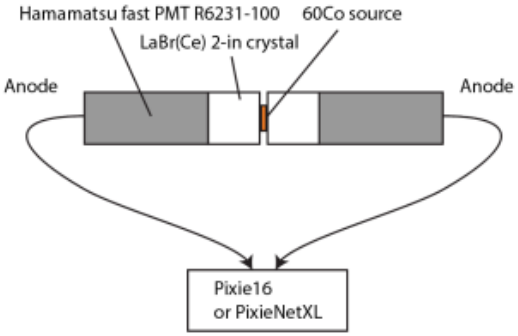

4. **Future 10G WR standard**

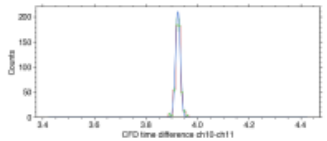
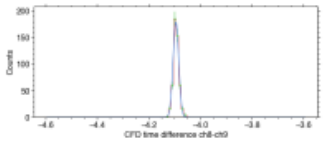
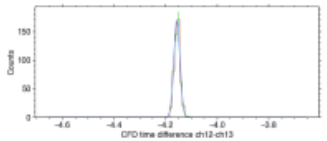
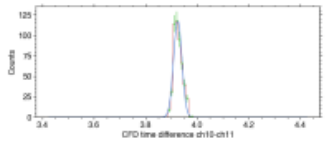
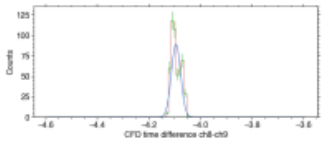
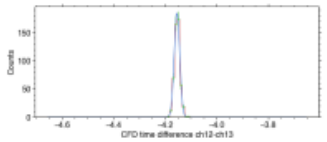


Main board with clock DBs for Kintex and Zynq

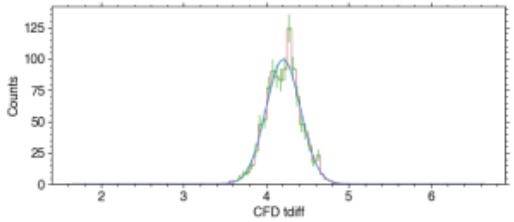
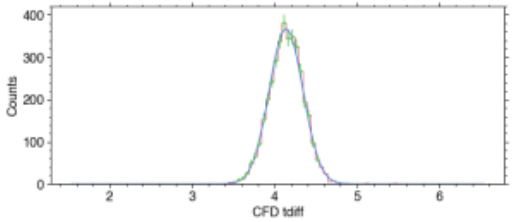
# Timing Measurements: Same-module CFD Timing (DB04, UTK)

**Split NIM signal using channel pairs with different input bandwidth**




| Ch 10/11 Fastest | Ch 8/9 Faster | Ch 12/13 Slowest |
|---|---|---|
|  22 ps FWHM |  26 ps FWHM |  25 ps FWHM |
|  38 ps FWHM |  42 ps FWHM |  26 ps FWHM |

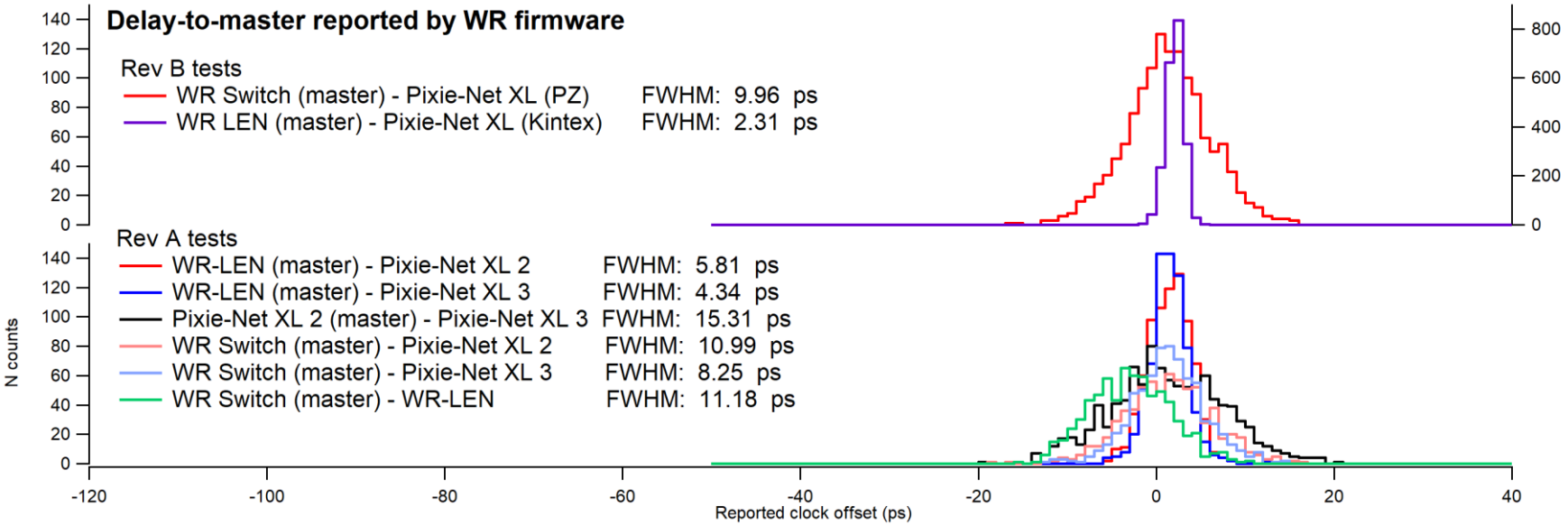
**There is no significant difference in the resolution.**

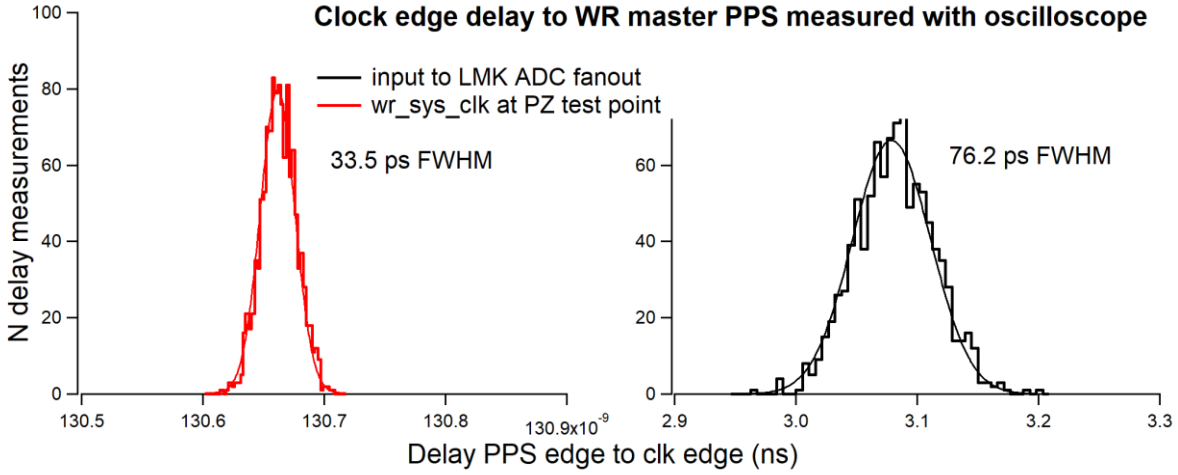
| New ADC board (fastest channel, ch10&11) | Pixie16 |
|---|---|
|  490 ps FWHM |  480 ps FWHM |

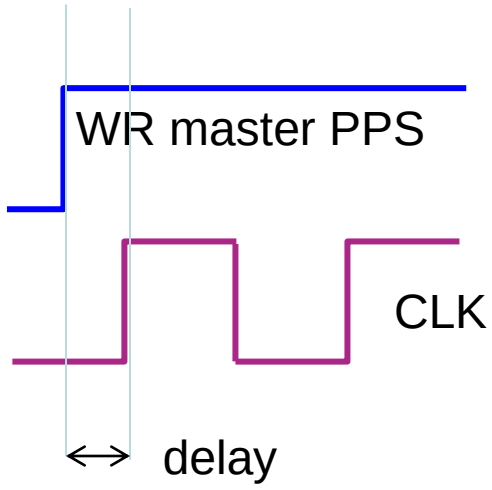
**Real detector, comparison to Pixie-16**

Courtesy of Noritaka Kitamura, UTK, May 2021

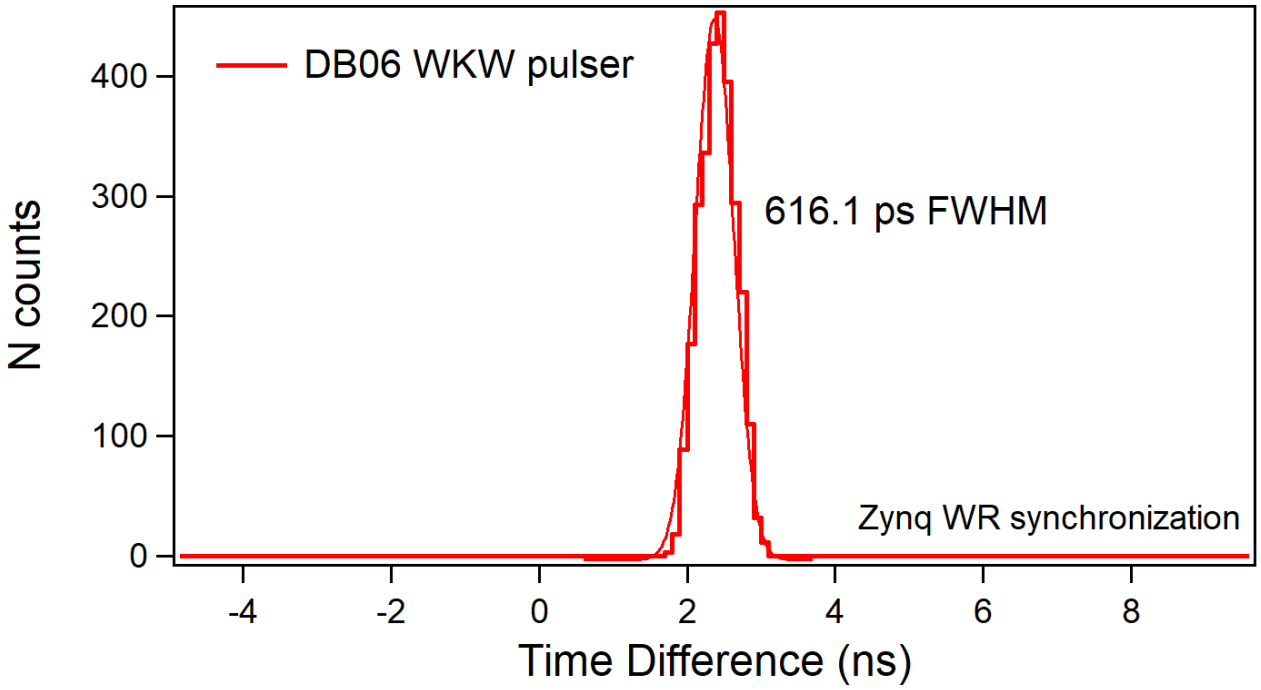
# Timing Measurements: FW log and Oscilloscope



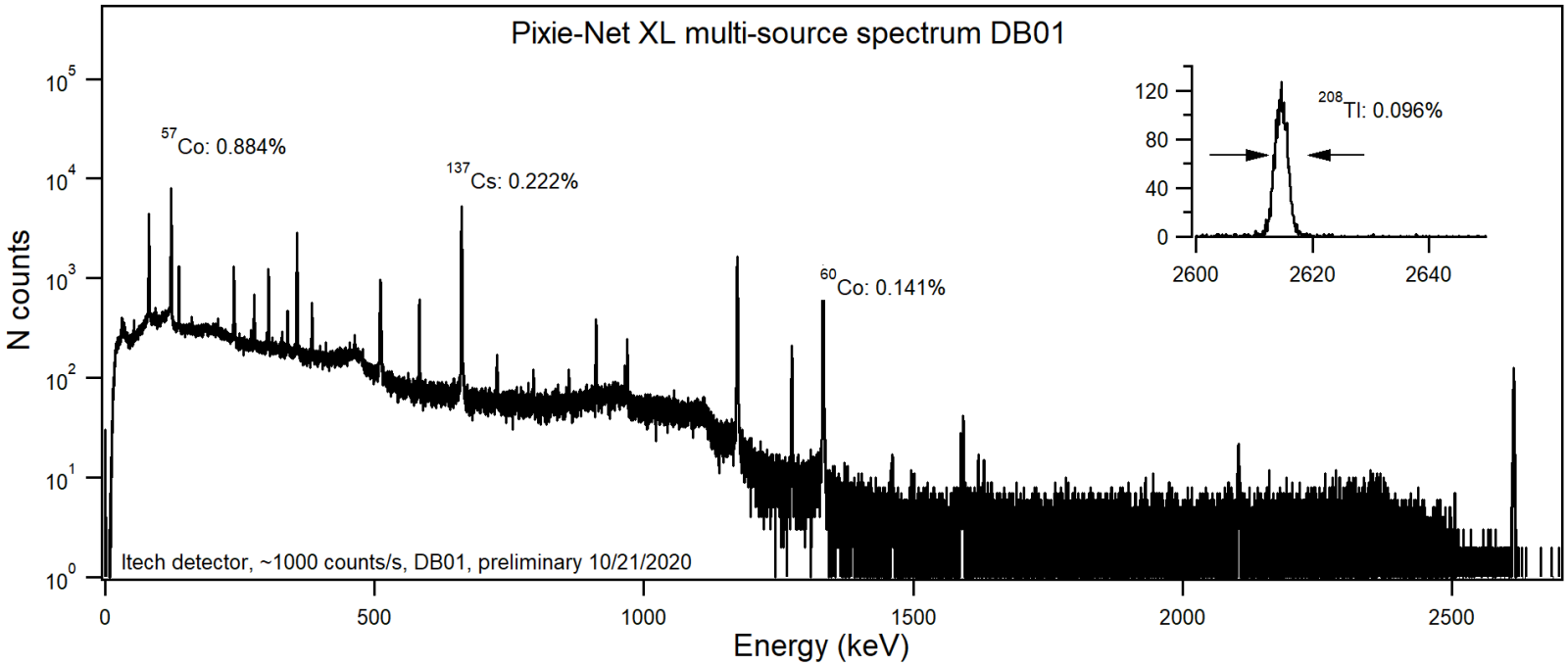



## Timing Measurements: 2-module CFD Timing DB06 (preliminary)




- Not great for a split pulser, but ok for some slower detectors
- Need to improve clock distribution path from Zynq to ADCs
- Need to improve signal source and input bandwidth
- Need to tune CFD parameters

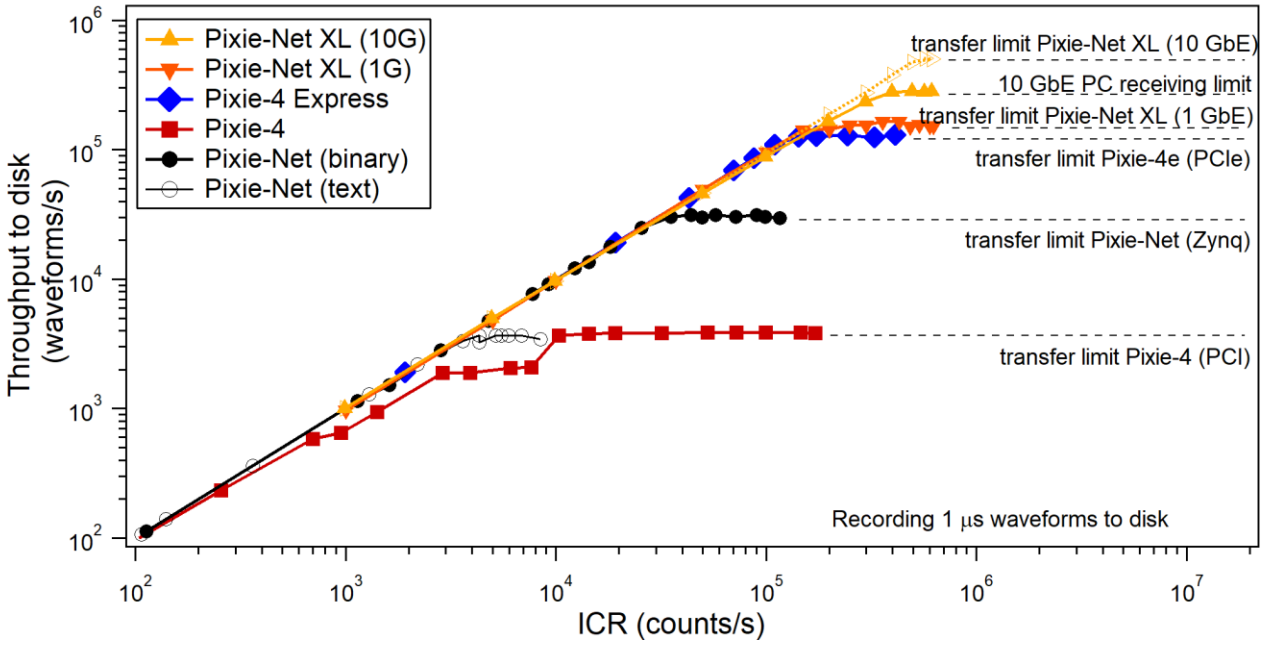
## Energy Resolution

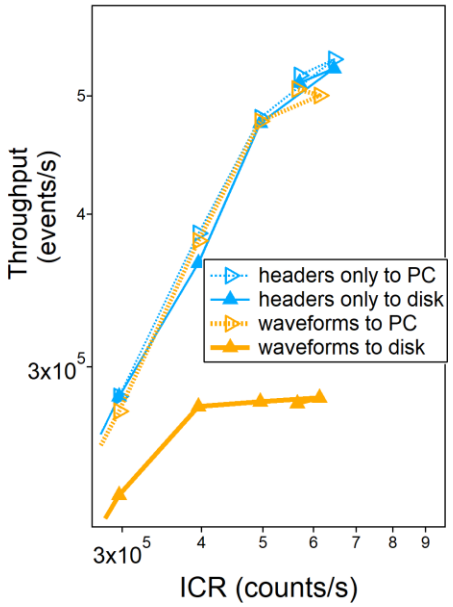


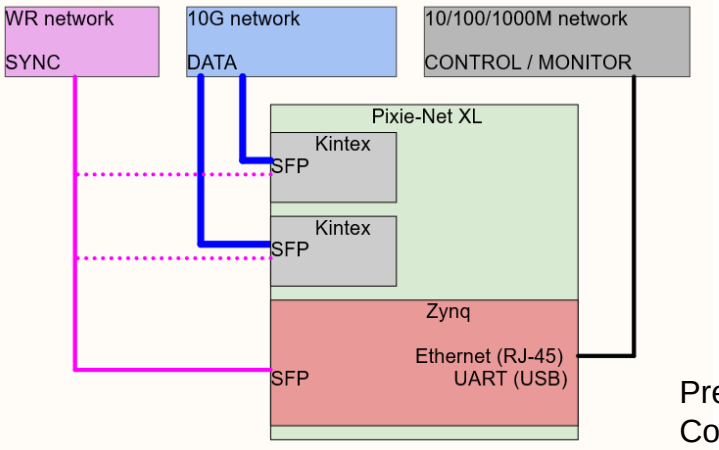

**Pixie-Net XL HPGe energy resolution (DB01)**

# Distributed digital data acquisition system with network time synchronization

## List Mode Data Throughput




- Pixie-Net XL exceeds previous models' throughput for storing event waveforms to disk
- Limited by packets dropped by PC (not by network)
  try multiple PCs?
- Almost 300,000 waveforms/s (or over 500,000 headers/s) per Kintex

Preferred setup architecture uses 3 networks (SYNC, CONTROL, DATA)
Could be all one network, but with lower throughput (two are max 1G)

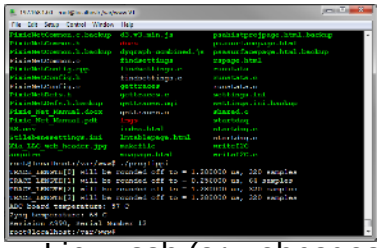
# Distributed digital data acquisition system with network time synchronization

## Commercial Product

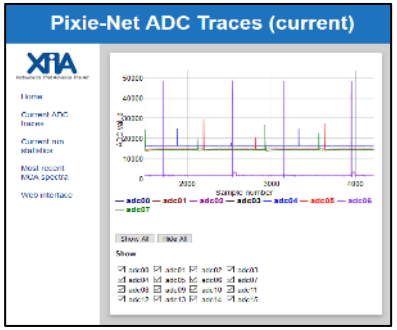

**Pixie-Net XL**
Several units sold to beta testers
3rd party funds for custom features

## Operation

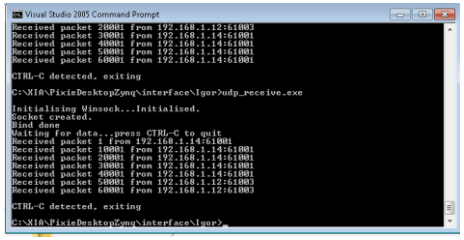
Can use single or multiple PCs for …



… Linux ssh (or webpages) for setup and daq




…webpages to monitor results and status




… receiving UDP data

# Distributed digital data acquisition system with network time synchronization

## Commercial Branches: SBIR work adopted in other XIA products*

- **Pixie-Net PTP**
  Phase I PTP prototype commercially available. Several units sold

- **Pixie-16 MZ-TrigIO**
  Trigger I/O module for XIA's 6U PXI pulse processor boards with PTP clock option
  Several units sold
  Also available as desktop PTP GPIO module

- **Pixie-4 Hybrid**
  Update of XIA's 3U PXIe pulse processor board
  Optional WR synchronization and 1G data output
  Reusing same ADC daughtercards
  Product released October 2020

- **Pixie-16 x1/x2**
  Update of XIA's Pixie-16 pulse processor board
  "HW ready" for WR + 1G data
  Reusing same ADC daughtercards, up to 32 channels per board
  Product release Fall 2021

* Mainly funded by XIA

## Summary

- Implemented WR network time synchronization on new detector DAQ electronics, the Pixie-Net XL
- Easily reaches “<1 ns” timing resolution goal but needs more tweaks to reach “best WR” performance of <20ps (in progress)
- List mode data output via 10G Ethernet
  max. measured output data rate is ~600 MB/s (test mode, one Kintex)
  max. LM data rate **received** is ~360 MB/s max (header only, one Kintex)

## Outlook

- Performance testing, more beta testing at NP labs, and product release
- Complete Myriad adapter
- Waiting for 10G WR switch …

# *Thank You*

# *Questions?*

# Distributed digital data acquisition system with network time synchronization

## *Existing Technologies*

- **Shared Clock Signal**
  Works, but requires dedicated cabling. Not ideal for distributed DAQ systems.
  Reported time resolution: sub-nanosecond, even tens of picoseconds

- **IEEE 1588 Precision Time Protocol (PTP)**
  Processors exchange synchronization messages over network to measure delays
  PTP Time Stamping Units (TSU) built into several commercial Ethernet MACs, Ethernet physical layers (PHY). Commercial PTP switches available ($$).
  Open source software for managing time synchronization (LinuxPTP, ptpd)
  Reported time resolutions: milliseconds (software TSU)
  low nanoseconds (hardware TSU)

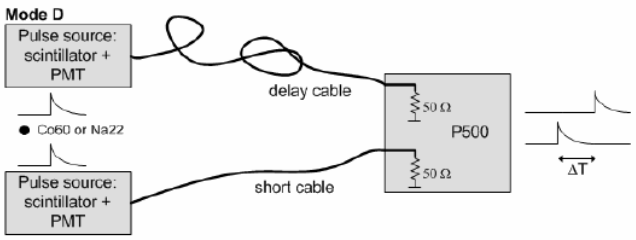
- **Synchronous Ethernet (SyncE)**
  Extract clock from Ethernet link and use for local processing

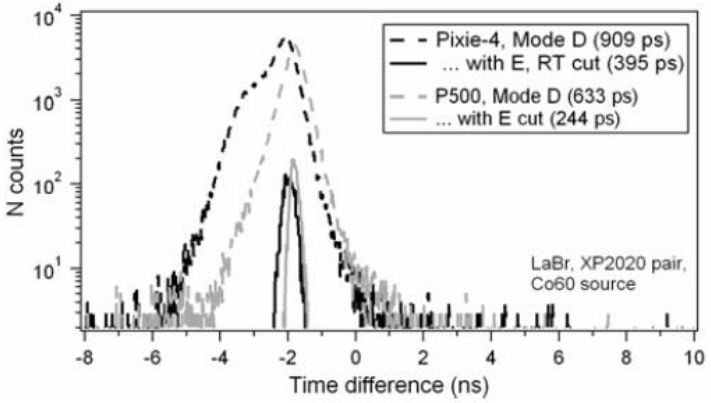
- **CERN's White Rabbit (WR)**
  Extension of PTP standard with synchronous Ethernet
  Open hardware project. WR network switch commercially available. WR modules developed by scientists
  Reported time resolution: sub-nanosecond, even tens of picoseconds

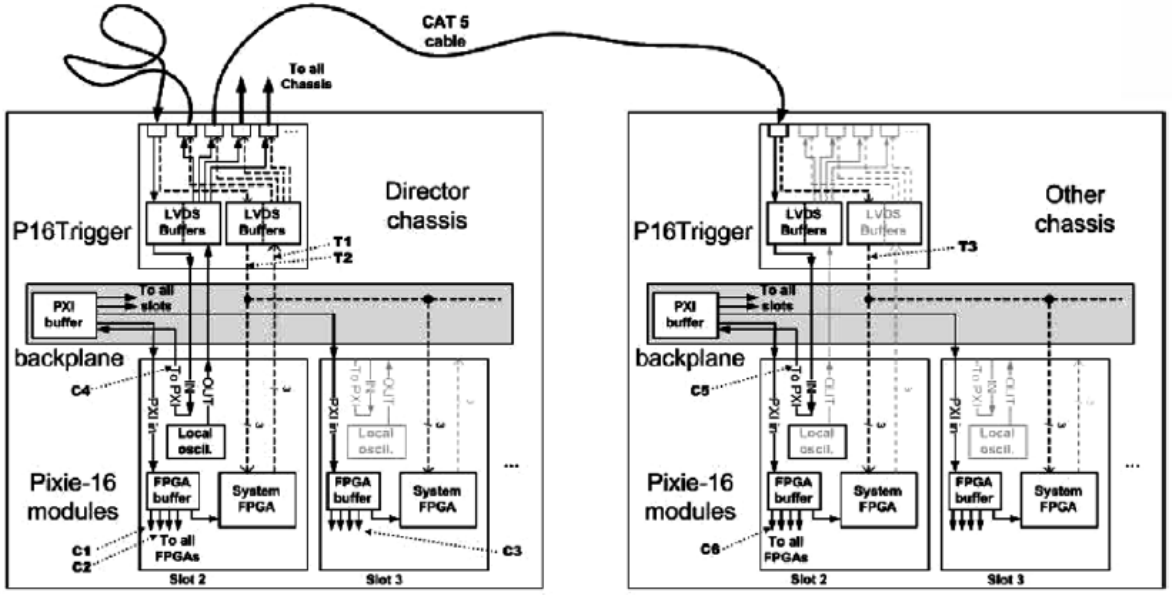
## Traditional Synchronization

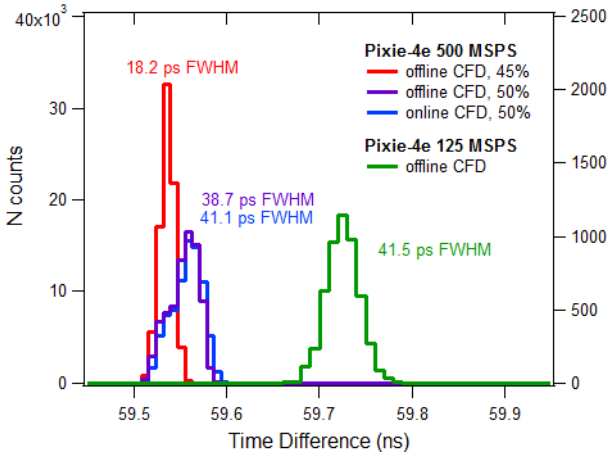
Traditionally, time synchronization between multiple channels of digital data acquisition is accomplished by sharing clocks, clock reset signals, and triggers.

With suitable algorithms (CFD), timing resolutions can be ~20 ps for idealized signals and a few hundred ps for detector signals digitized with 100-5000 MSPS.



## *UDP Data Output Discussion*

**Pro:**

- Simple to implement in FPGA (WR code) and on receiving side
- Easy transfer to one or more storage nodes
- Faster

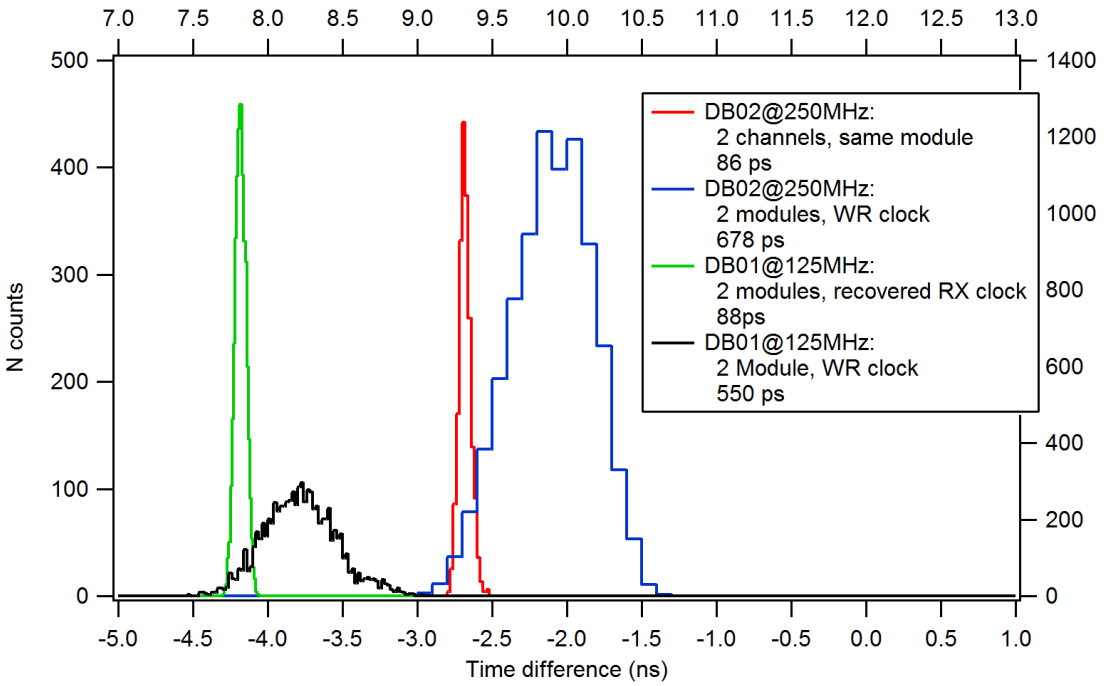
**Contra:**

- Possible loss of data — but 1 packet = 1 event; but how bad is it actually? [*]
- Possible data out of sequence — but all packets timestamped
- Error checking needs to be pushed to “higher level application”

=> Will look into firmware updates for UDP package management or for TCP

* (M.J. Christensen et al: Achieving reliable UDP transmission at 10 Gb/s using BSD socket for data acquisition systems, arXiv:1706.00333v1 [physics.ins-det] 1 Jun 2017)

# Timing Measurements – Rev. A with pulser




## Time Resolutions

⇒ With 75 MHz ADC daughtercard, pulser, tuned WR clock: 550 ps FWHM

⇒ With 250 MHz ADC daughtercard, pulser, tuned WR clock: 678 ps FWHM
(2 channels in same module: 86 ps FWHM)

⇒ With 125MHz ADC daughtercard, pulser, recovered RX clock: 88 ps FWHM