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IP Access Gateway

Continuous Acquisition E-TDC Subsystem

Award DE-SC0017156

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IPAG Goal:

- Integrates Frontend, Backend, and computing subsystems into a software defined, in band time synchronized network through COTS HW, optic links, and IP based protocols (asynchronous).
- Provides ubiquitous timing synchronization with a precision range of 10pS or better and immediate event reconstruction
- Flexibility and scalability for upgrading existing systems or build new systems, providing up to 1.6Tbps network bandwidth per board.

Functional blocks:

- Continuously timestamping ETDC engines, comprising one or several continuous TDC configurable for either accuracy or density (Ex: 16 channels at 500fS v. 400 channels at 10pS). Any combination of configurations coexist on the same FPGA device;
- The network interface – multiples of 10/25/100 GE optical links powered by GTY Ultrascale+ serdes. The system is transparent to the actual data link protocol which is configurable.
- Packet Switch

Features

- ETDC determines the timing of both the rising and the falling edge of a pulse associated with an event
- Minimum pulse width is 500pS. The system is based on signal pattern recognition and allows implementation of 250pS or 167 pS, depending on the bandwidth of the IO pin buffer;
- Sustained, continuous minimal pulse period = 1nS (2x 0.5nS). Can capture timestamps for 1GHz signals.
- Generates 4 timestamps per 600MHz clock for an aggregated 2.4 G timestamps per second;
- The number of bits per Timestamp are configurable with the default of 40b comprising a 16b clock counter, 15 bits encoded fractional period and 9b for additional flags and data;
- Output bandwidth is the product between the number of detected transitions and the bits per transition multiplied with the number of ETDC.
- Timestamps are numerically synchronized, without any timing control hardware, by using a non intrusive General timing Synchronization (GTS) protocol and algorithms. The numerical synchronization will not change local clocks, which eliminates transient errors and instability.
- Can provides very fast ADC equivalent functionality for pulse width modulation (PWM) of the measured signal;
- SW defined operation.
- Seamless interface and retiming of timestamps data from third party detectors
- Provide embedded switching, and timing to all machines in the DAQ or computer farm.
- Lower cost HW version can be configured for 80pS synchronization.

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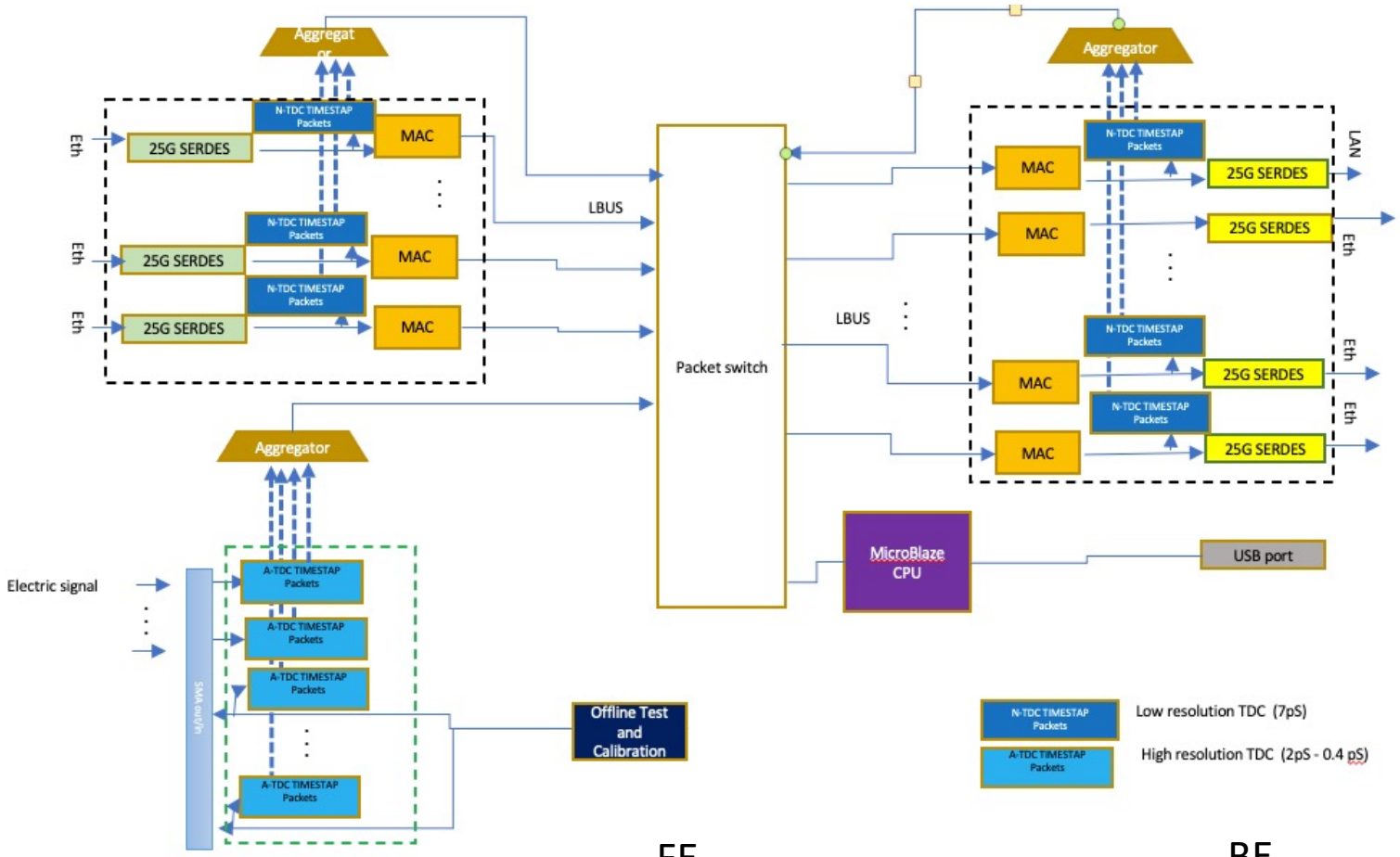
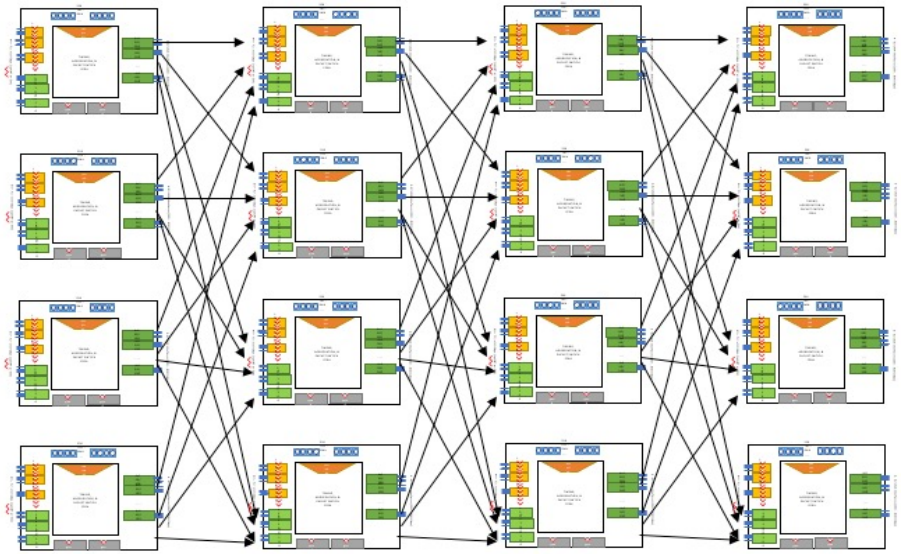
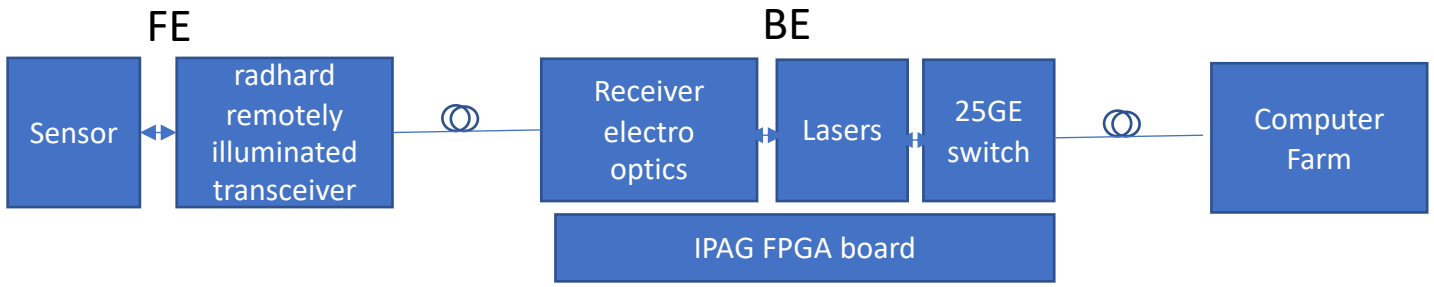
IPAG FPGA Functional Block Diagram
Implements most of HW functionality



Distributed switch and time synchronized optical network based on IPAG FPGA boards





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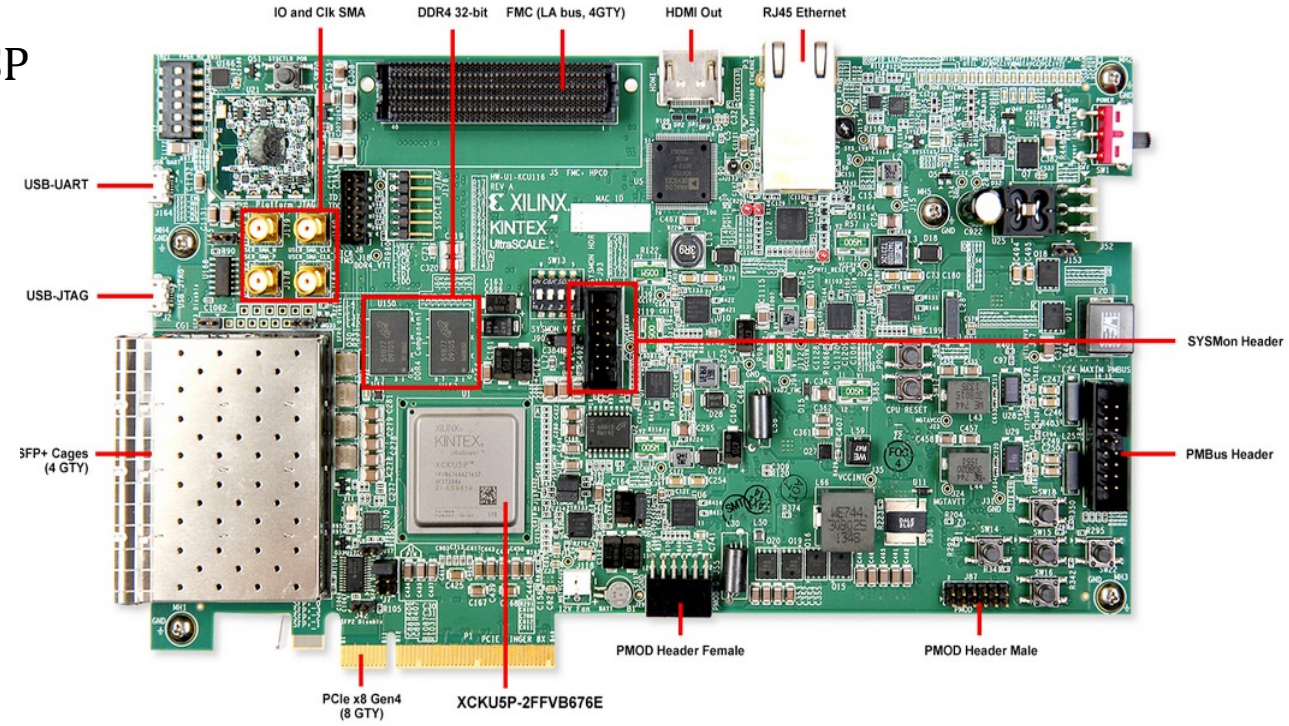
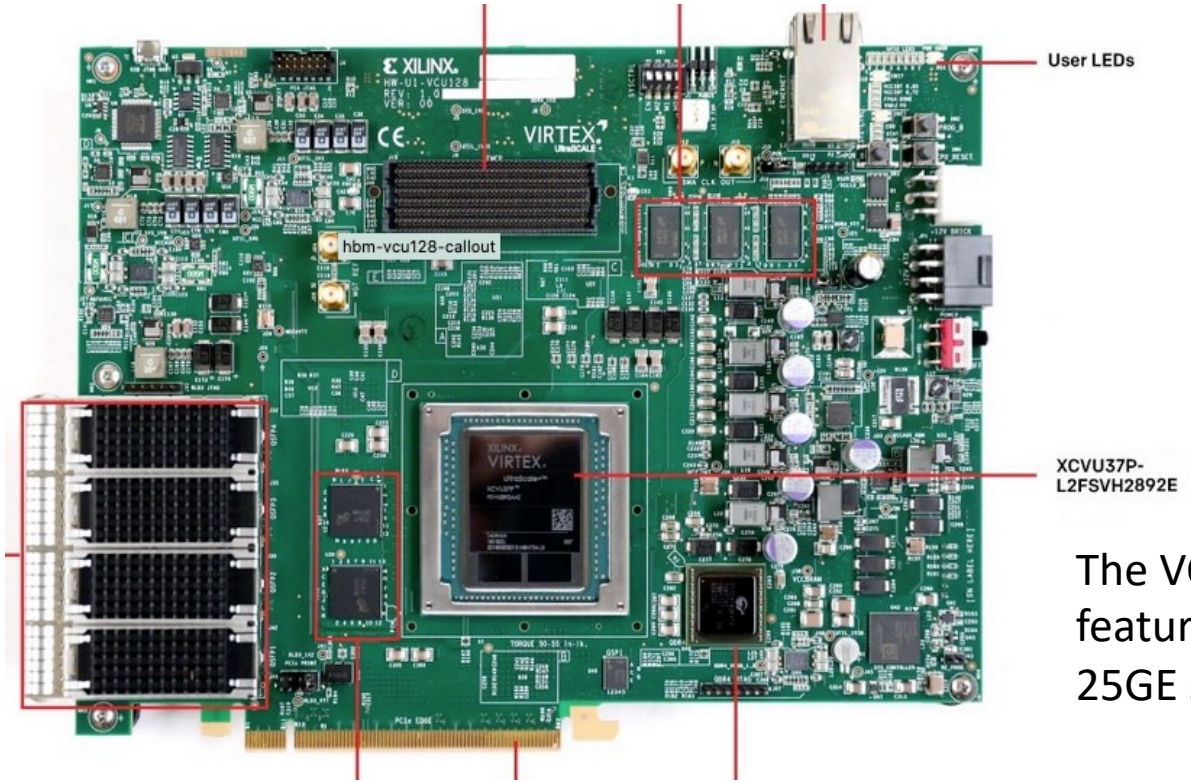
COTS FPGA boards used for IPAG development and evaluation

The low cost KVU116 featuring the KU5P Kintex USP FPGA used for development of the ETDC.





The VCU128 board with a more powerful VU37P FPGA featuring 96 GTY ports used for development of distributed 25GE switching and synchronization system.

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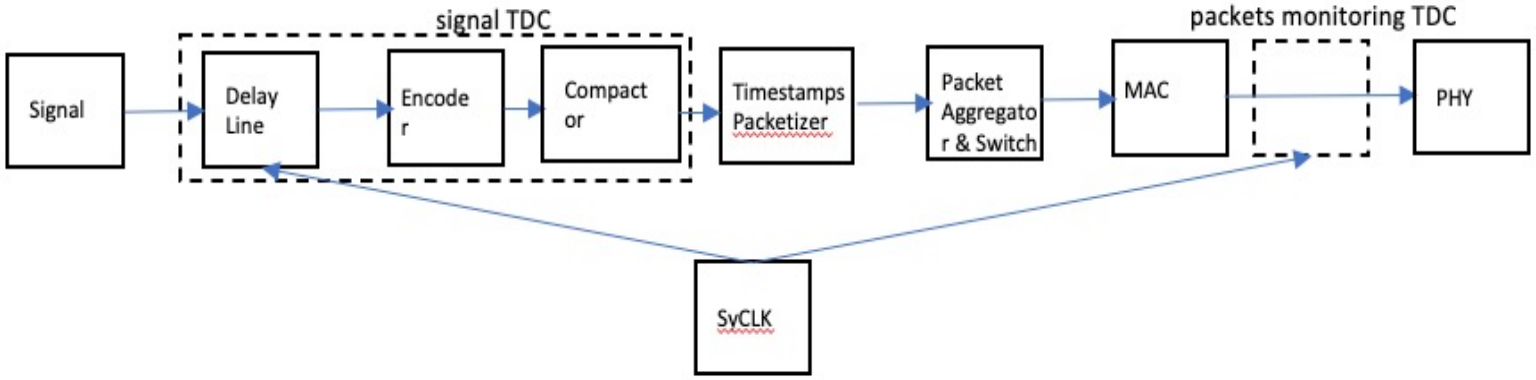
Event signal processing flow diagram



The signal to be timestamped by the ETDC enters a Delay Line implemented with a high-speed Carry Chain (CC) of an FPGA (or ASIC). A system clock (SyCK) with a known frequency of 600MHz takes continuous snapshots of the signal traveling through the CC. The snapshot pattern is further analyzed by the encoder block, to generate up to four transitions. The estimated positions of the taps where either positive or negative transitions happen are encoded into binary numbers. Noisy transitions are interpreted probabilistically. Linearity and phase corrections are added for the tap of the transition, at the Encoder module. The piped encoder has 12 or more stages matching the overall system accuracy.
The accuracy requires the use of the low jitter global clock (GC) pins and distribution lines. Regular IO pins generate higher jitter.

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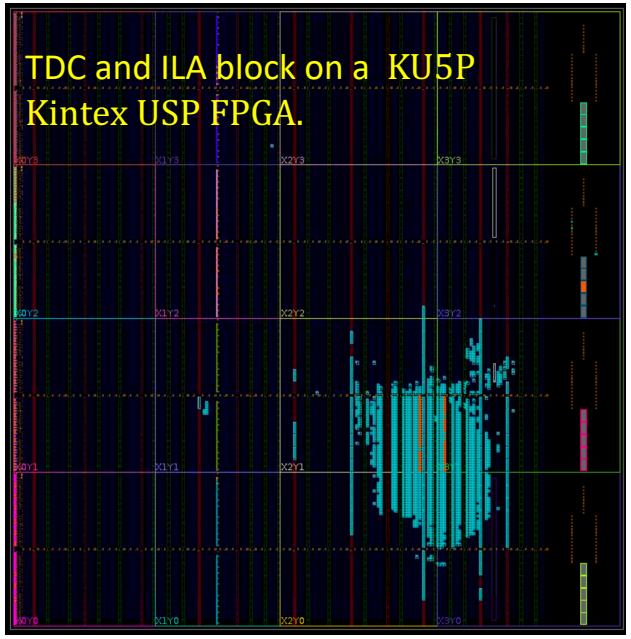
The TDC is the HW building block of timing and synchronization subsystem



The parallel architecture is simple, performant, and takes less resources.

Simple TDC – Kintex KU5P resource utilization

Name	CLB LUTs (216960)	CLB Registers (433920)	CARRY8 (27120)	F7 Muxes (108480)	F8 Muxes (54240)	CLB (27120)	LUT as Logic (216960)	LUT as Memory (99840)	Block RAM Tile (480)	DSPs (1824)
N etdc_rtl	4915	9556	203	165	21	1472	3723	1192	78	6
> dbg_hub (dbg_hub)	441	741	7	0	0	138	421	20	0	0
> dsp_pipe_top (dsp_pipe_top)	704	1383	0	0	0	281	697	7	2	6
> fifo_gen_64x8__UART (fifo_generator_uart)	0	0	0	0	0	0	0	0	1	0
> fifo_generator_256x64out__dsp (fifo_generator_0)	0	0	0	0	0	0	0	0	8	0
flop_comp_data_buf (flop__parameterized10)	0	160	0	0	0	57	0	0	0	0
flop_push4_reg (flop2__parameterized1)	0	3	0	0	0	3	0	0	0	0
flop_trig_out (flop__parameterized6)	1	1	0	0	0	1	1	0	0	0
> genblk1[1].dl_120_pn_inst (dl_120_top)	114	480	60	0	0	127	114	0	0	0
> ila_0 (ila_0)	3617	6419	134	165	21	1050	2452	1165	67	0
> uart_0 (uart)	18	29	2	0	0	6	18	0	0	0

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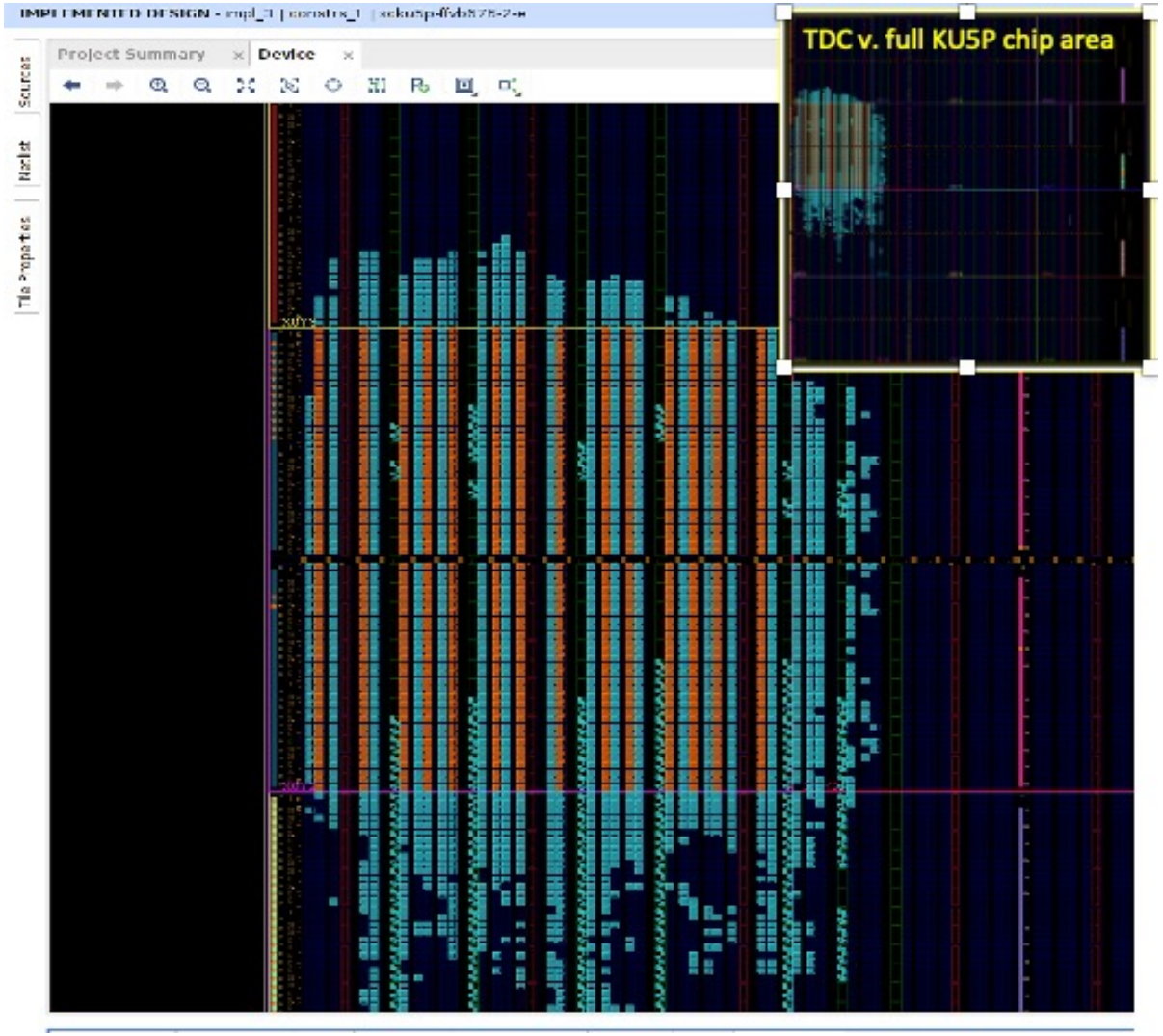
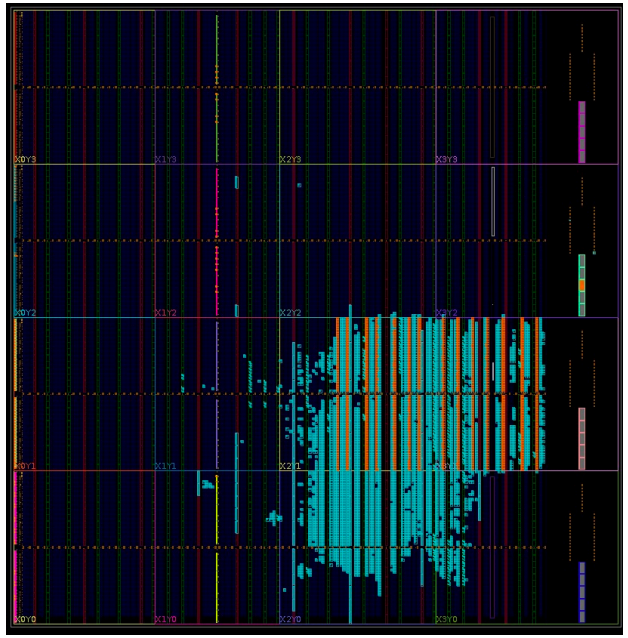
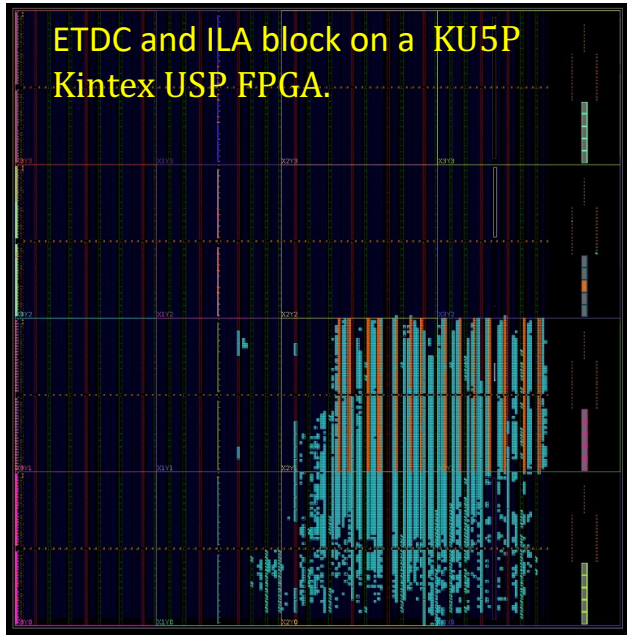
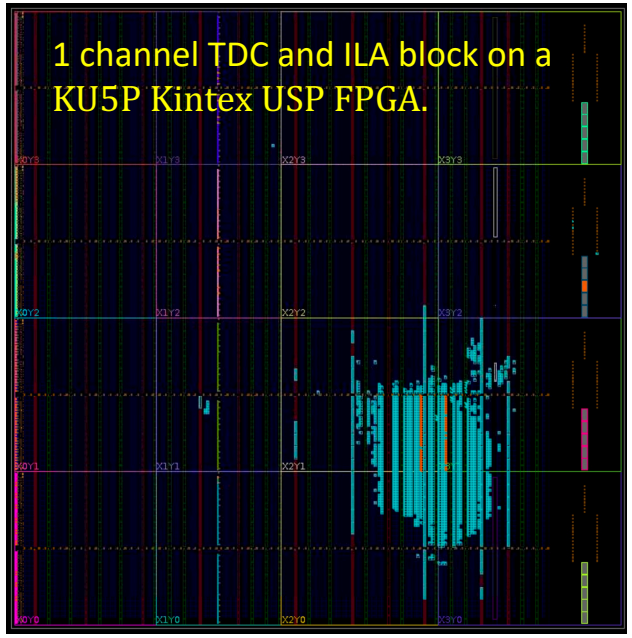






Top:
Several outcomes of ETDC place and route. The 600fS ETDC and ILA block used automatic, unconstrained routing. The logic design considered from inception the outcome of synthesis for the specific architecture of the FPGA device, resulting in predictable results and minimal manual constraints of the VIVADO tool.



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ETDC – Kintex KU5P resource utilization

Name	CLB LUTs (216960)	CLB Registers (433920)	CARRY8 (27120)	F7 Muxes (108480)	F8 Muxes (54240)	CLB (27120)	LUT as Logic (216960)	LUT as Memory (99840)	Block RAM Tile (480)	DSPs (1824)	Bonded IOB (280)	HPIOB_M (96)	HPIOB_S (96)	HDIOB_M (36)	HDIOB_S (36)	HPIOB_SNGL (16)	H
N etdc_rtl	14391	26324	987	229	53	3712	13066	1325	82	131	105	40	40	9	11	5	
dbg_hub (dbg_hub)	444	741	7	0	0	129	412	32	0	0	0	0	0	0	0	0	
dsp_pipe_top (dsp_pipe_top)	8602	11833	0	0	0	1821	8500	102	2	131	0	0	0	0	0	0	
fifo_gen_64x8__UART (fifo_generator_uart)	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	
fifo_generator_256x64out__dsp (fifo_generator_0)	0	0	0	0	0	0	0	0	8	0	0	0	0	0	0	0	
flop_comp_data_buf (flop__parameterized10)	0	160	0	0	0	56	0	0	0	0	0	0	0	0	0	0	
flop_push4_reg (flop2__parameterized3)	0	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	
flop_trig_out (flop__parameterized6)	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	
genblk1[1].dl_120_pn_inst (dl_120_top)	0	480	60	0	0	129	0	0	0	0	0	0	0	0	0	0	
genblk1[2].dl_120_pn_inst (dl_120_top__parameterized0)	240	480	60	0	0	131	240	0	0	0	0	0	0	0	0	0	
genblk1[3].dl_120_pn_inst (dl_120_top__parameterized1)	0	480	60	0	0	117	0	0	0	0	0	0	0	0	0	0	
genblk1[4].dl_120_pn_inst (dl_120_top__parameterized2)	240	480	60	0	0	127	240	0	0	0	0	0	0	0	0	0	
genblk1[5].dl_120_pn_inst (dl_120_top__parameterized3)	0	480	60	0	0	118	0	0	0	0	0	0	0	0	0	0	
genblk1[6].dl_120_pn_inst (dl_120_top__parameterized4)	240	480	60	0	0	121	240	0	0	0	0	0	0	0	0	0	
genblk1[7].dl_120_pn_inst (dl_120_top__parameterized5)	0	480	60	0	0	111	0	0	0	0	0	0	0	0	0	0	
genblk1[8].dl_120_pn_inst (dl_120_top__parameterized6)	240	480	60	0	0	120	240	0	0	0	0	0	0	0	0	0	
genblk1[9].dl_120_pn_inst (dl_120_top__parameterized7)	0	480	60	0	0	131	0	0	0	0	0	0	0	0	0	0	
genblk1[10].dl_120_pn_inst (dl_120_top__parameterized8)	239	480	60	0	0	117	239	0	0	0	0	0	0	0	0	0	
genblk1[11].dl_120_pn_inst (dl_120_top__parameterized9)	0	480	60	0	0	118	0	0	0	0	0	0	0	0	0	0	
genblk1[12].dl_120_pn_inst (dl_120_top__parameterized10)	240	480	60	0	0	121	240	0	0	0	0	0	0	0	0	0	
genblk1[13].dl_120_pn_inst (dl_120_top__parameterized11)	0	480	60	0	0	118	0	0	0	0	0	0	0	0	0	0	
genblk1[14].dl_120_pn_inst (dl_120_top__parameterized12)	240	480	60	0	0	124	240	0	0	0	0	0	0	0	0	0	
ila_0 (ila_0)	3615	6500	138	229	53	1049	2424	1191	70	0	0	0	0	0	0	0	
uart_0 (uart)	25	27	2	0	0	9	25	0	0	0	0	0	0	0	0	0	

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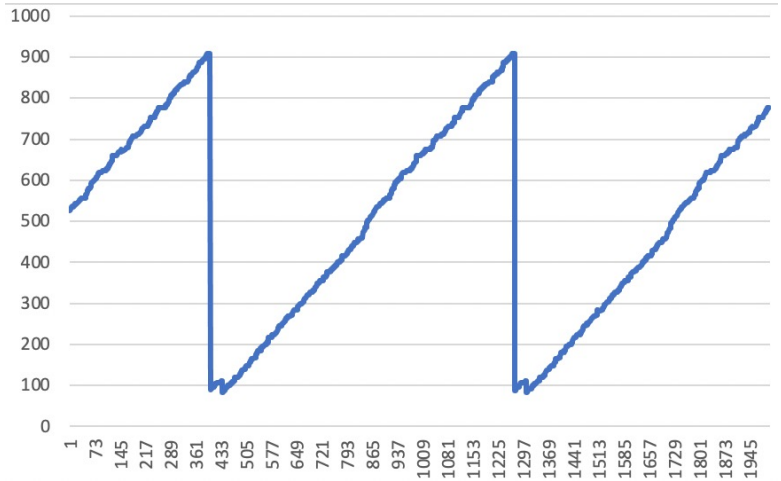
Single TDC (raw HW data, without linearity corrections)

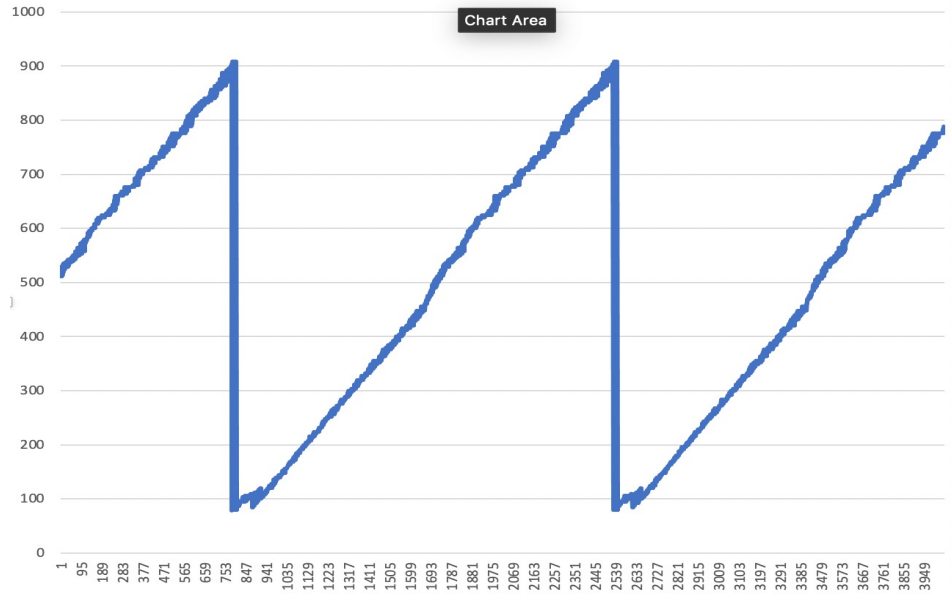
The figure at right illustrates continuous timestamping of both positive and negative edges of a ~300MHz event signal (600 M timestamps per second without linearity corrections). Here the timestamps of the positive and negative edge are slightly shifted due to uneven duty cycle.

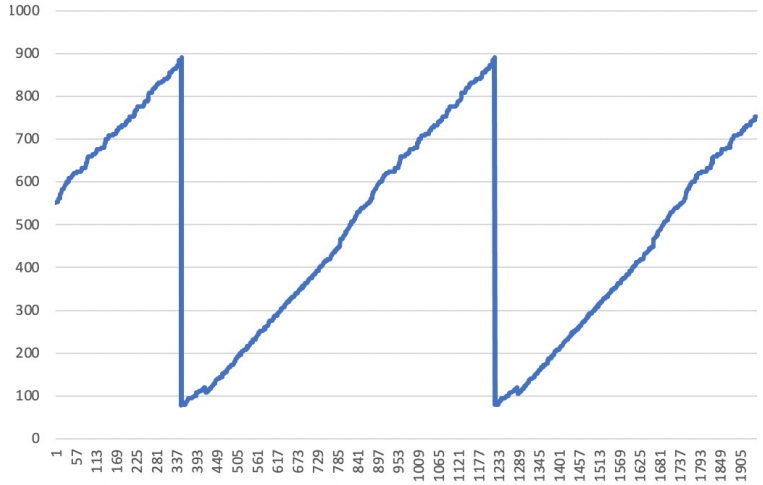
Period corresponds to 600MHz sampling clock (T=1666pS). The slope is the tap count of the delay lines as the event signal propagates through.

Vertical scale = fractional timestamp (2pS per unit)
Horizontal: clock count



Extracted timestamps for positive transitions events





Extracted timestamps for negative transitions events

TDC FPGA generated timestamps

Four timestamps per clock parallel encoder data:
600MHz Clock Counter, fractional tap encoder, flags

5442	80	1	1	5442	0	0	0	5442	0	0	0	5442	0	0	1
5443	0	0	0	5443	0	0	0	5443	0	0	0	5443	908	1	0
5444	80	1	1	5444	0	0	0	5444	0	0	0	5444	0	0	1
5445	0	0	0	5445	0	0	0	5445	0	0	0	5445	908	1	0
5446	80	1	1	5446	0	0	0	5446	0	0	0	5446	0	0	1
5447	0	0	0	5447	0	0	0	5447	0	0	0	5447	916	1	0
5448	84	1	1	5448	0	0	0	5448	0	0	0	5448	0	0	1

Example 1: events are captured at the first and last section

4751	0	0	0	4751	561	1	1	4751	580	1	0	4751	0	0
4752	0	0	0	4752	0	0	0	4752	0	0	1	4752	0	0
4753	0	0	0	4753	561	1	1	4753	580	1	0	4753	0	0
4754	0	0	0	4754	0	0	0	4754	0	0	1	4754	0	0
4755	0	0	0	4755	561	1	1	4755	580	1	0	4755	0	0
4756	0	0	0	4756	0	0	0	4756	576	1	1	4756	0	0
4757	0	0	0	4757	0	0	0	4757	580	1	0	4757	0	0

Example 2: events are captured at the mid two sections
Note: data on this page was captured on a one TDC engine.

Packetized TS Output

6578	828	1	1
6586	828	1	1
6594	832	1	1
6602	832	1	1
6610	836	1	1
6618	840	1	1
6626	840	1	1
6634	840	1	1
6642	844	1	1
6650	856	1	1
6658	856	1	1
6666	860	1	1
6674	864	1	1
6682	864	1	1
6690	872	1	1

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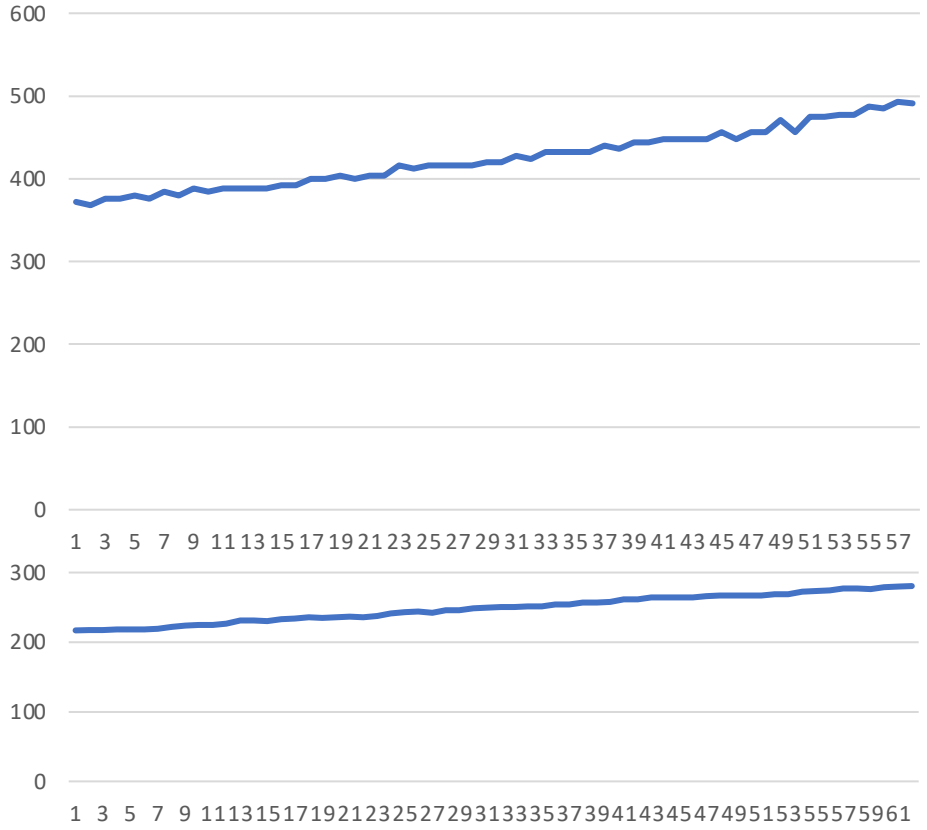
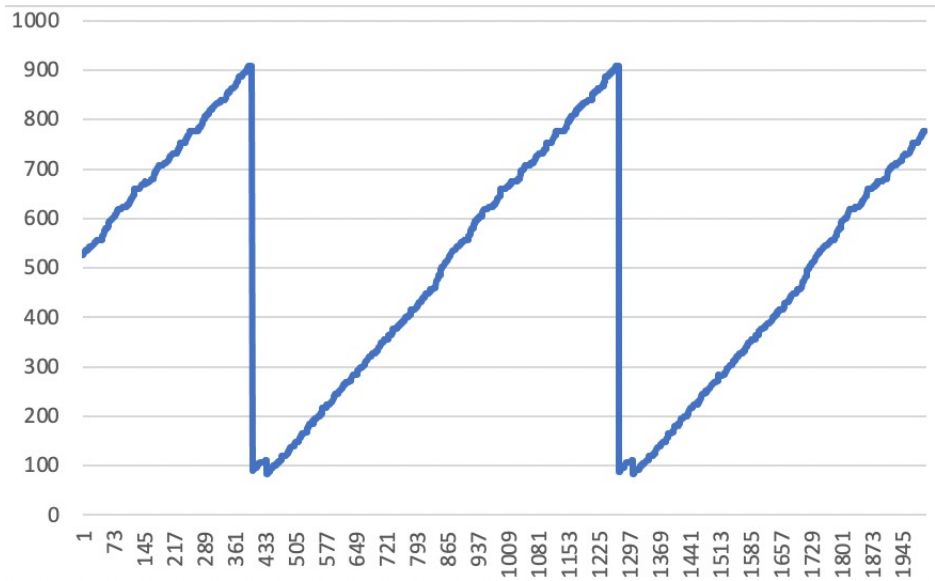
Single TDC (before calibration and without on chip processing for linearity)



Top :Sequence of timestamps generated by a single TDC (for 300MHz signal)
Bottom: the smoothing effect of parallelism in ETDC for identical conditions

Vertical scale = 2pS per unit
Horizontal: system clock number (at 600MHz)



Continuous timestamping of positive and negative edges of a 300MHz event signal (600,000,000 timestamps per second).
Period corresponds to 600MHz raw counter clock. The slope is the factional part
Vertical scale = 2pS per unit
Horizontal: clock number

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Thank you !

For more information contact us

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BACKUP SLIDES
APPLICATIONS

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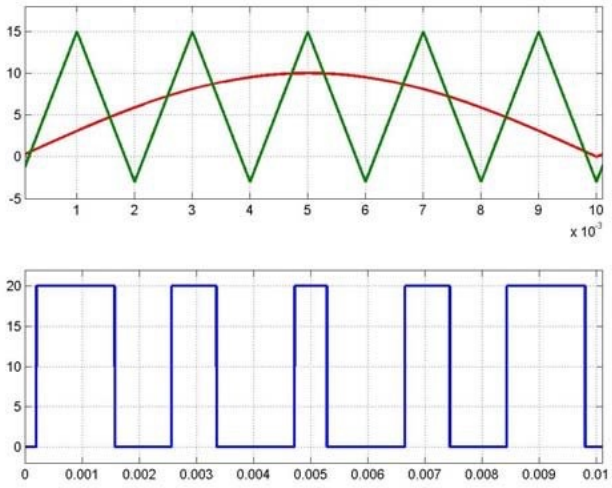
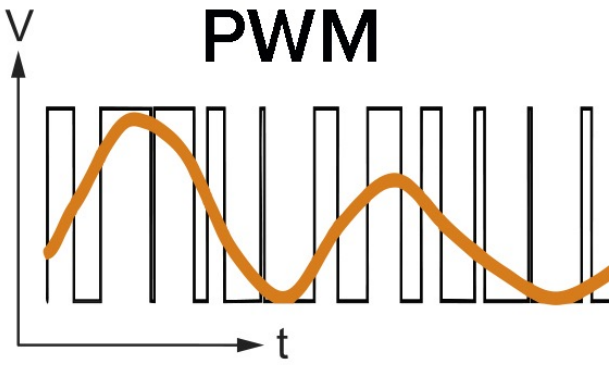
Application Example
PWM Timestamped ADC

ADC – ETDC reciprocity
Numerical average of PWM timestamps provides signal amplitude.
IPAG FPGA provides both timing, and fast ADC in multiple combinations.
FMC mezzanine VITA cards provide HW adaptation for PWM.





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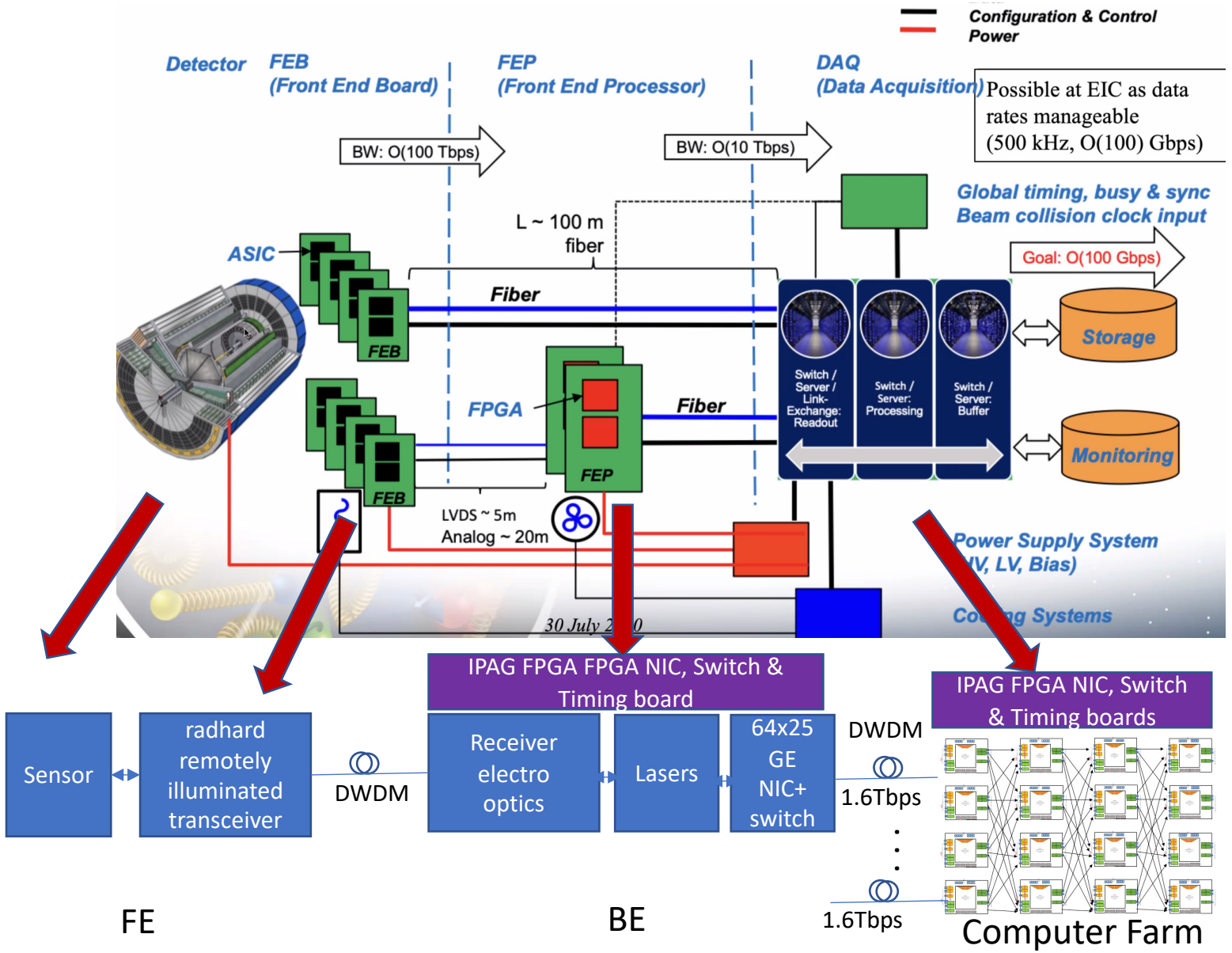
Application Example
Triggerless, in-band Synchronized DAQ for BNL EIC



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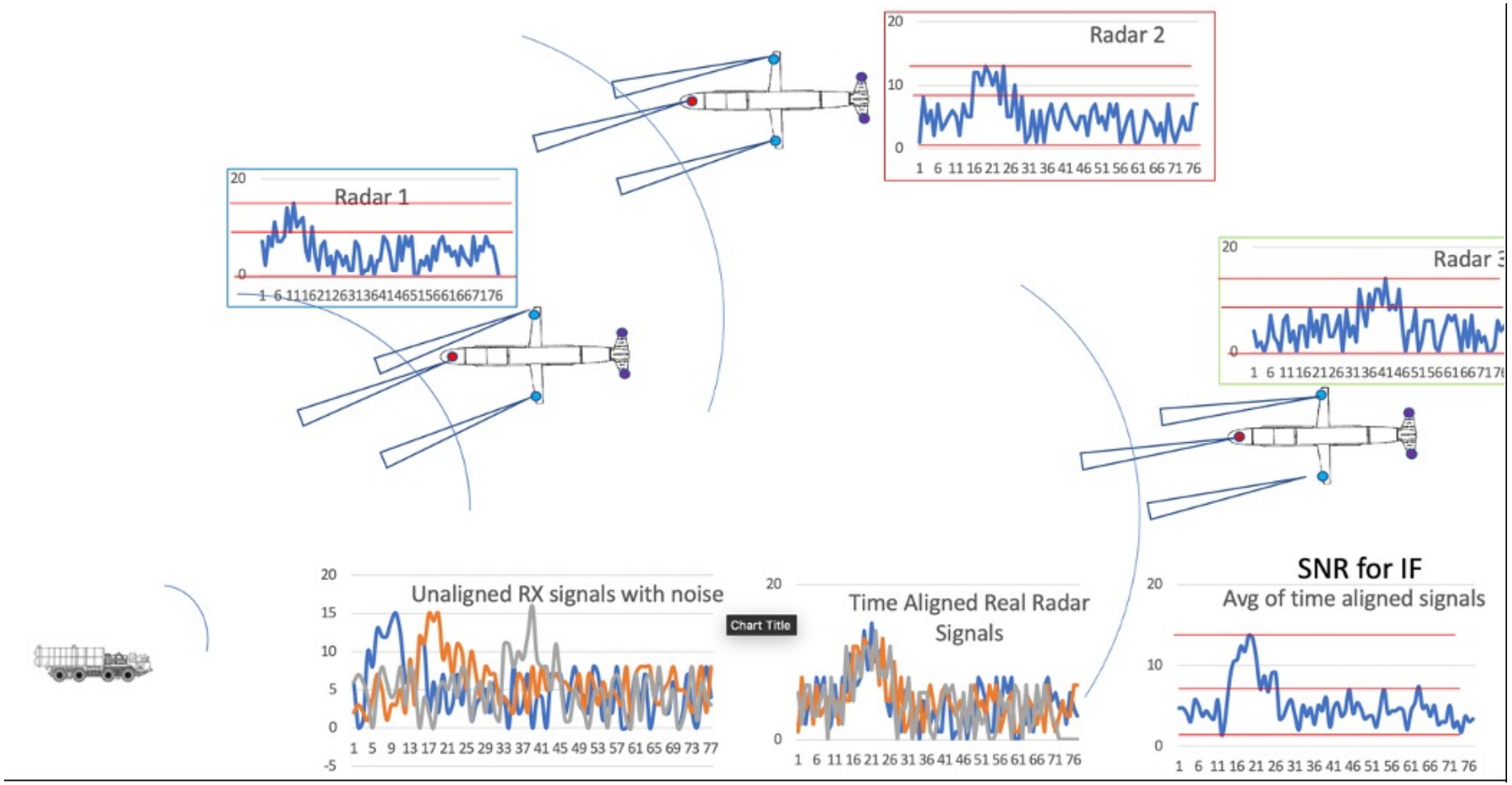
Application Example

Position Navigation and Timing (PNT)

Collaborative Radar range extension



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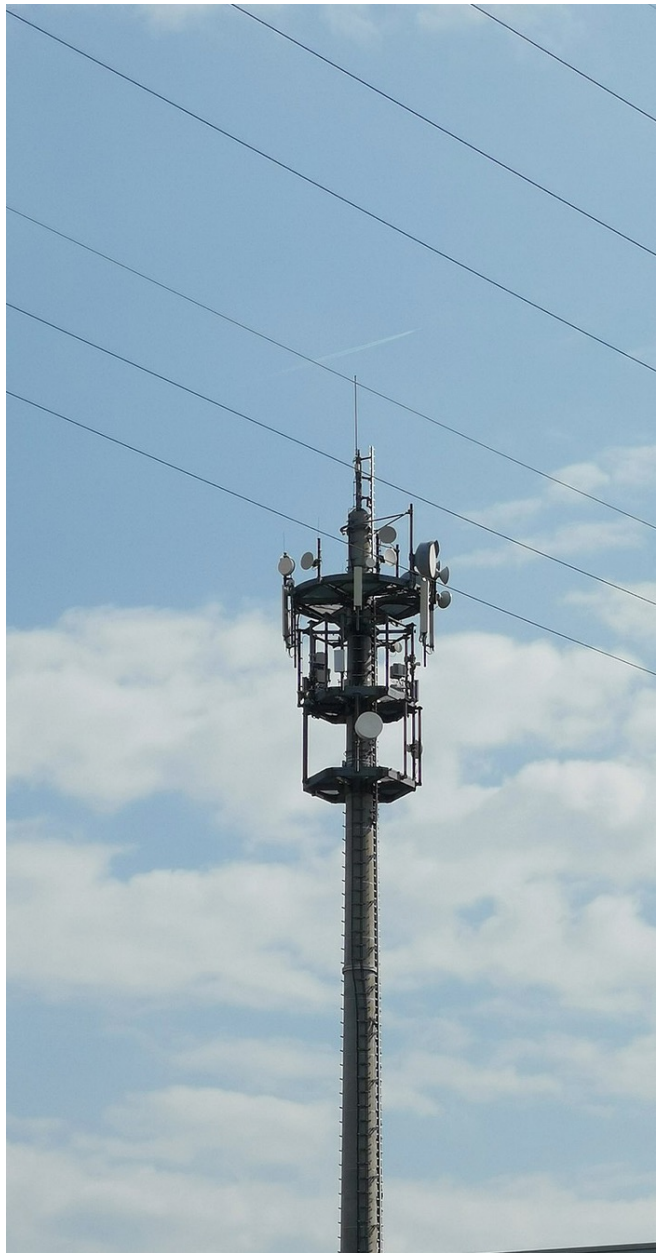

5G