DOE SBIR/STTR Tech Exchange

STTR Phase 2 Topic 28b

A multi-channel radiation-tolerant, low-power, high-speed and resolution analog-to-digital converter for nuclear physics detectors

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Outline

- Company Overview
- Multi-Gs/s, Radiation-Tolerant Analog-to-Digital Converter
- Measured performance
- Radiation resiliency tests (TID and SEE)
- Summary and Plans

About Our Company

- **Focused on Power and Analog rad-hard IC design and process development**
- **Developed TalRad™ rad-hard IC design process (available now at TSI Semiconductors)**
  - **Significantly reduces development time**
- **Growing portfolio**
  - **17 products available now**
- **Expanded office space 2020 in Plano, TX (Dallas area)**
  - **Established an electronics lab/test facility**
  - **NIST-800-171 compliant infrastructure to handle confidential Government data**

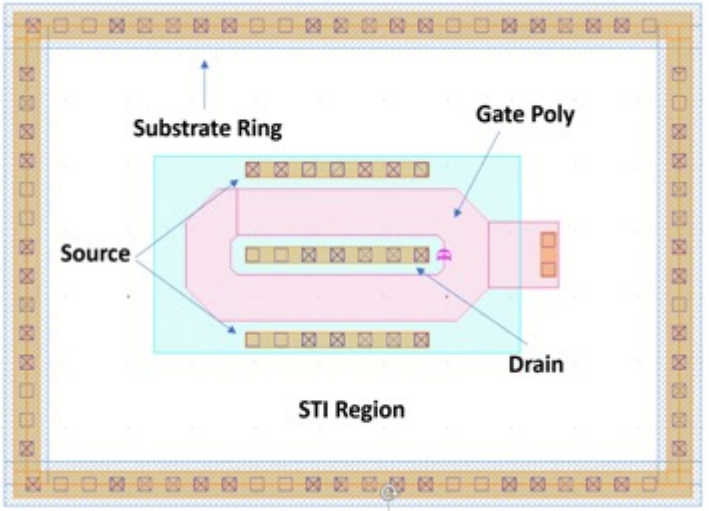
Enabling small satellite applications by:

- **Bridging the technology gap between commercial and high reliability components**
- **Significantly lowering the cost of rad-hard integrated circuits (ICs) by enabling modern computer aided verification tools and commercial processes**

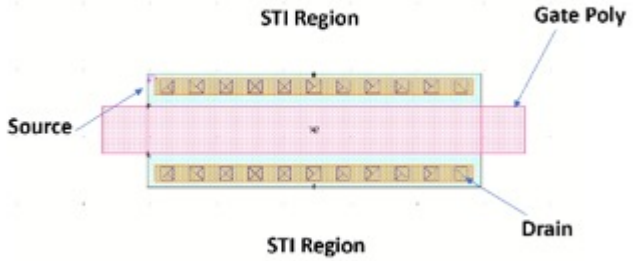
The TalRad™ Process Design Kit

- **Partnered with TSI Semiconductors, the only Trusted 180 nm HV CMOS foundry on US soil**

- **Annular 1.8V and 5V Transistor**
  - **Suitable for applications requiring greater than 300krad(Si) TID**
- **TalRad™ 1.8V and 5V Transistors**
  - **Reduced size and capacitance and improved performance compared to annular transistors**
  - **Great for precision analog applications**
  - **Lower quiescent current**
- **TalRad™ ESD Cells**
  - **Class II 4kV ESD, 300krad(Si) radiation tolerance**
- **Rad-Hard 1.8V Digital Cell Library**



Annular



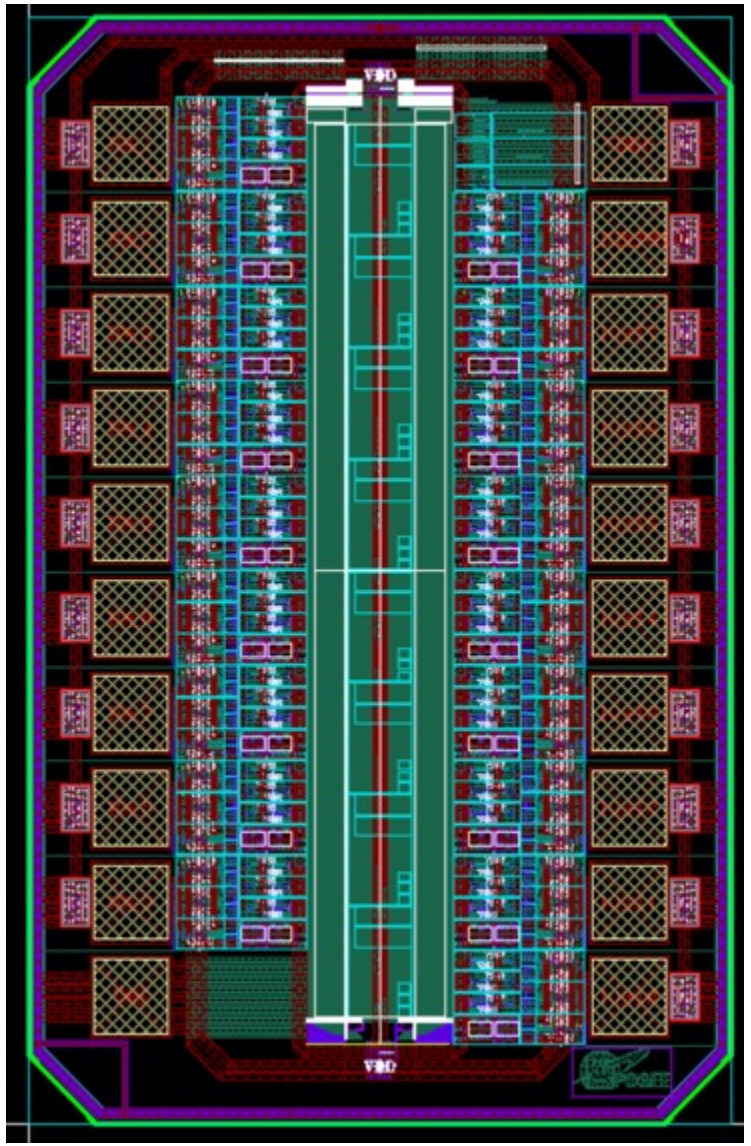
TalRad™

AP54RHCXXX Family

Flight units available now! MOUSER ELECTRONICS

A family of radiation hardened logic gates in plastic packages built with the TalRad™ PDK at TSI Semiconductor:

- **Industry standard pinout includes a:**
  - **Two supply level shifter**
  - **Single supply transceiver**
  - **Voter with daisy chain error detect**
  - **Other 7400 series logic functions**
- **TID/SEL hardened up to 30krad (Si) and 80 MeV-cm^2/mg**
  - **300krad (Si) versions are sampling now!**
- **Latches are DICE (SEU hardened)**
- **All parts have cold-spare capability**
  - **Fail-safe inputs and outputs with no static power penalty**
- **Designed for Class 2 ESD**
- **TSSOP package, 14 pin package**
- **Specified over -55°C to +125°C, 1.6V to 5.5V V_{DD}**
- **View portfolio at: https://apogeesemi.com/products/**
- **Single die can release 40+ devices in 14 and 20 pin configurations**



Products

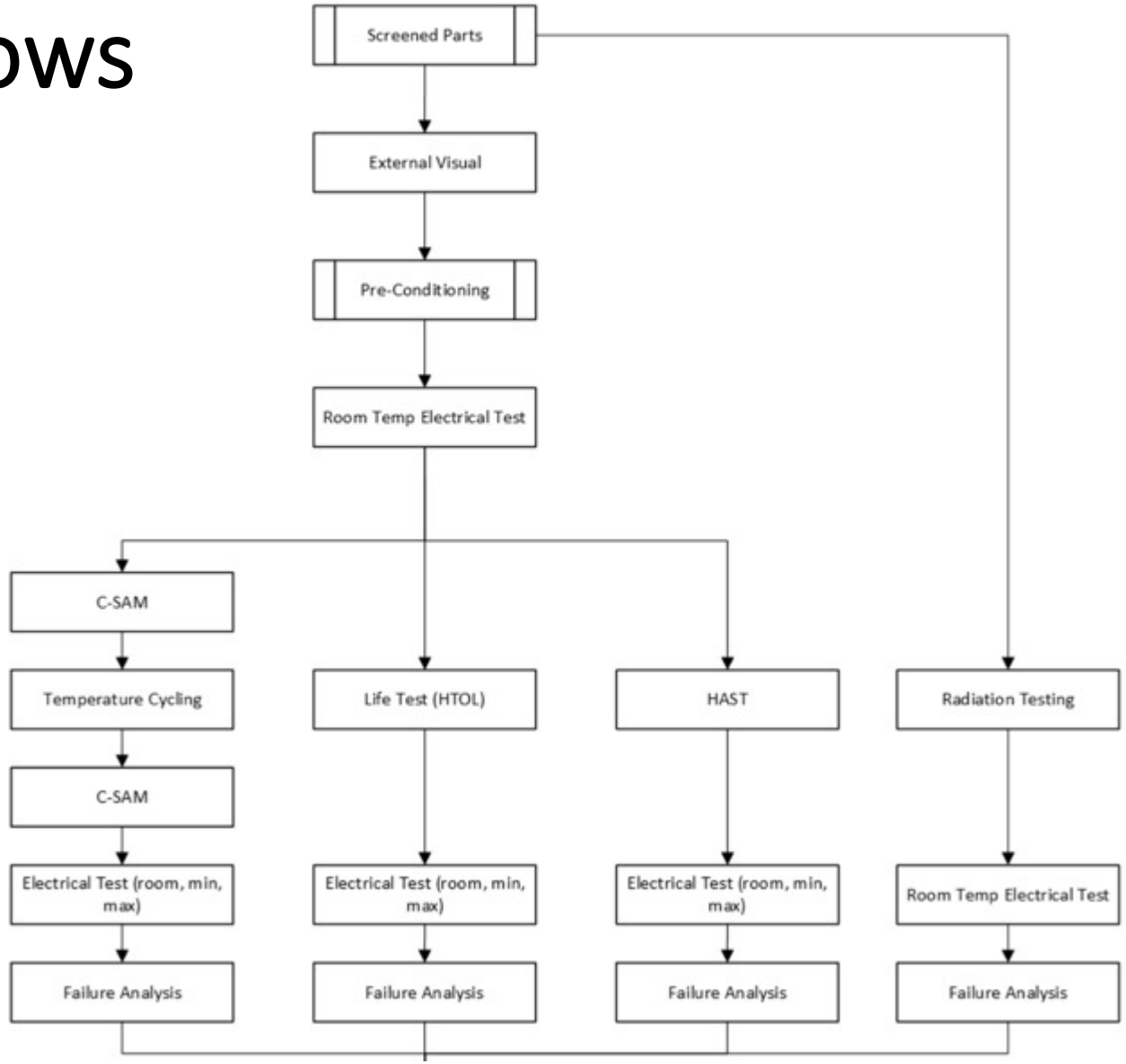
Radiation Hardened Products

All our rad-hard products are built with cold-sparing capabilities and triple-redundancy providing maximum reliability and area savings.

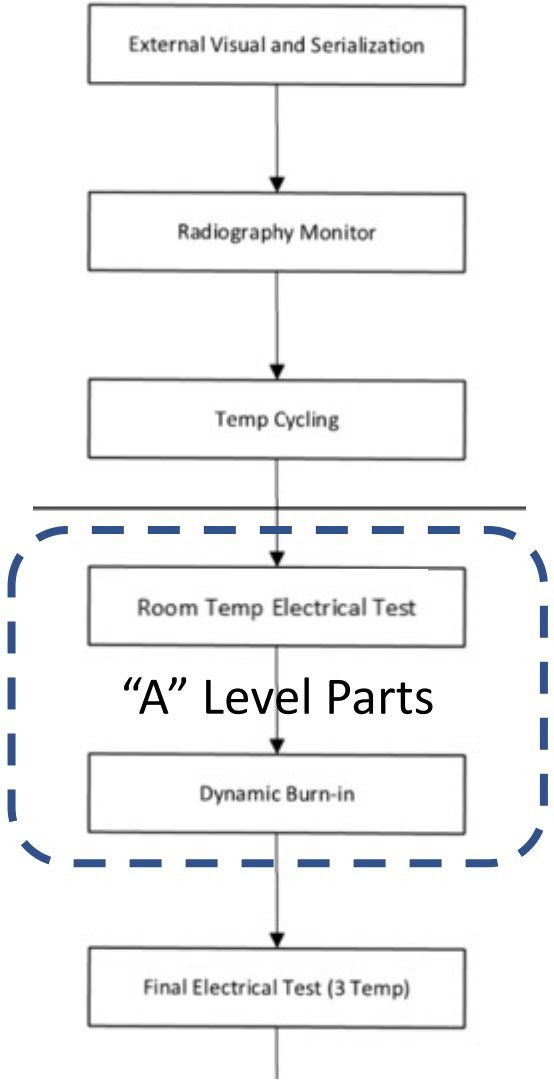
Logic Functions

Qual Flows

Lot Acceptance Flow



Screening Flow

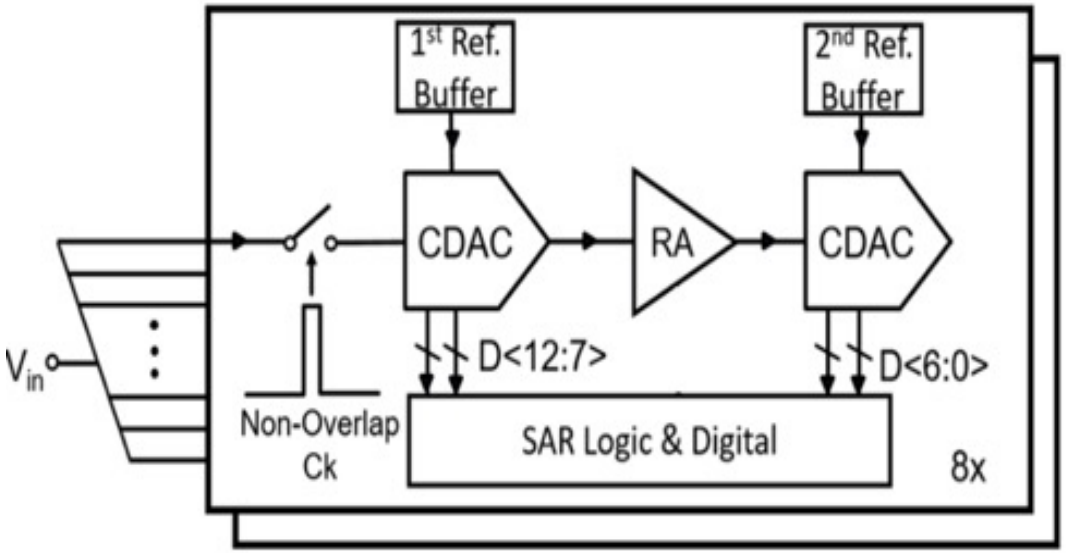


Multi-Gs/s Radiation-Tolerant Analog-to-Digital Converters (ADC)

12-bit ADC - Main Features and Applications

Features

- Sample rate: ≥ 1GS/s in CMOS
- 12 bit resolution (~10b ENOB)
- Power consumption: 50mW per 1GSps



Radiation Tolerance

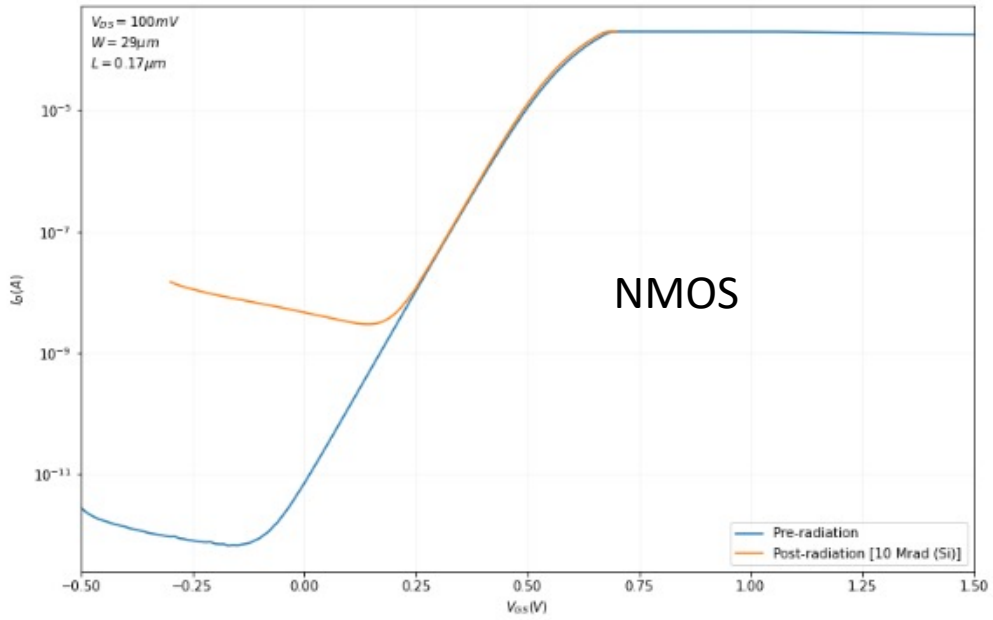
- TID immunity > 10 Mrad (Si)
- SEL up to 86 MeV·cm^2 /mg

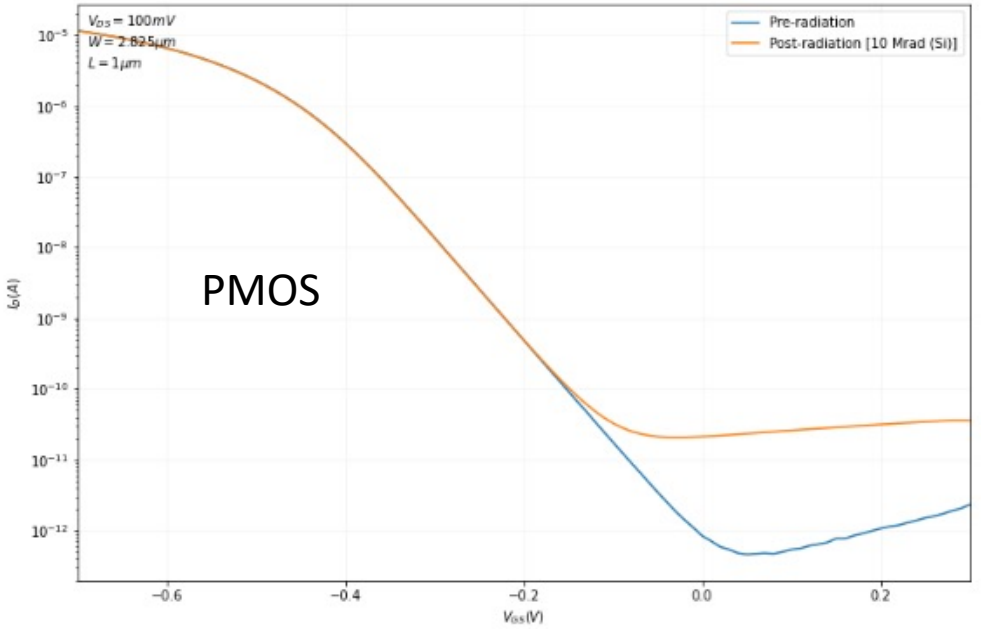
Applications

- Pixelated detectors
- Waveform sampler
- Real time oscilloscope

TID Radiation Testing for TSMC 28nm CMOS Process

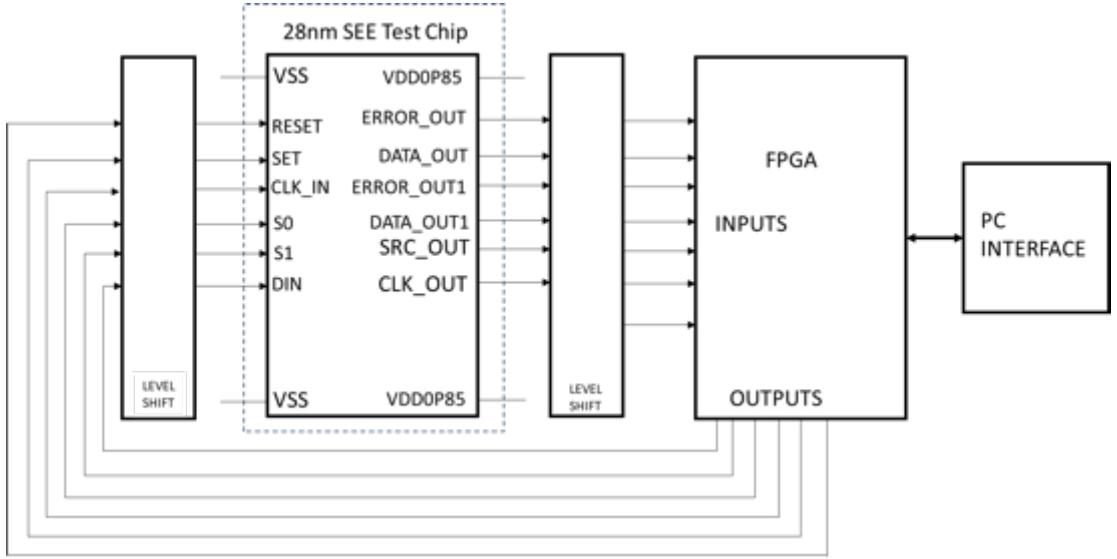
- Test-chips were fabricated with structures for **TID** evaluation, which included NMOS and PMOS devices, as well as diodes.
- TID irradiation was performed at VPT Rad and devices (shipped in dry ice) were characterized in an automated setup at Apogee Semiconductor
- Below are examples of I_D vs. V_{GS} curves for NMOS and PMOS devices before and after radiation (showing low leakage current for subthreshold conditions even after 10Mrad TID).



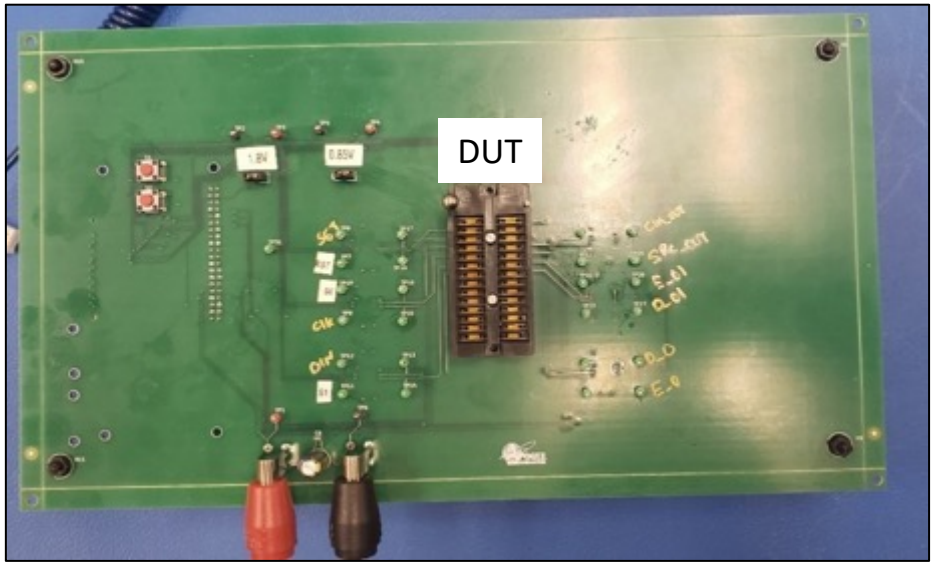


SEE testing on test-chip in 28nm CMOS process

- Test-chip for **SEE** testing based on a chain of over 8000 flip-flops (shift register) and a system for error counting were built and prepared for testing at Texas A&M particle accelerator.
- Testing delayed (Oct. 2021) due to COVID and availability of PXI testing instrument.



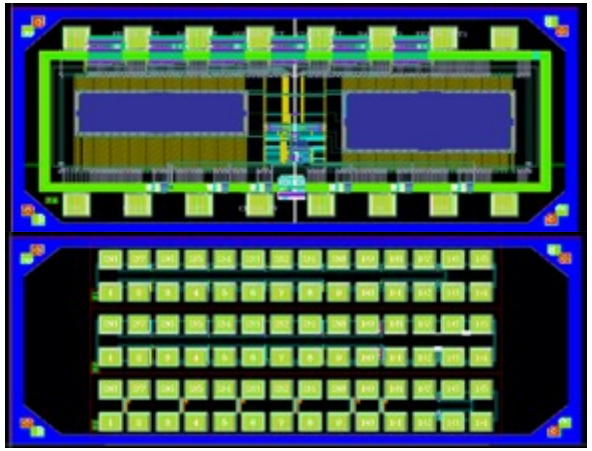
Block diagram of system built around test-chip for evaluation of SEE performance

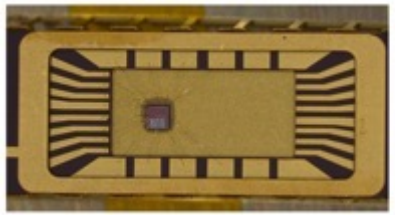


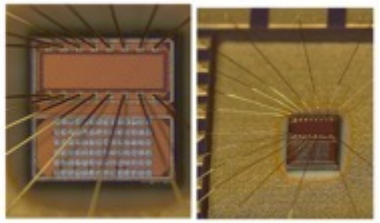
Socketed test board for SEE testing of 28nm DUT (FPGA board that interfaces between the DUT and PC is on bottom)

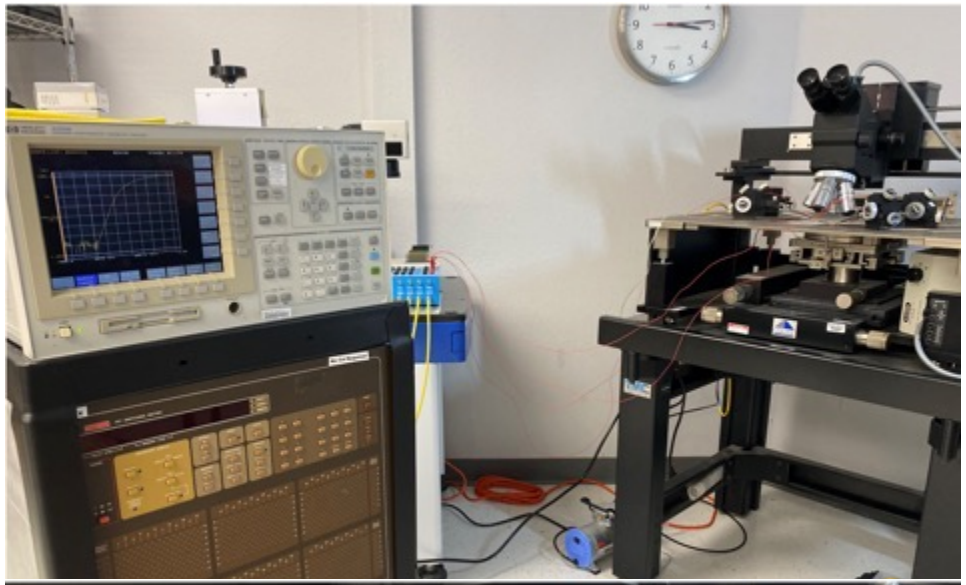
Probing of 28nm Test Chip

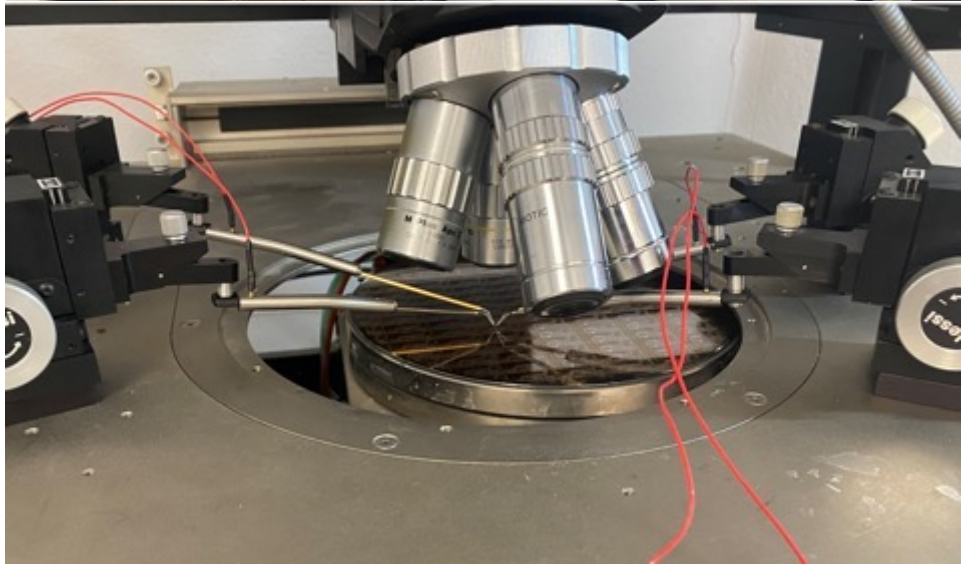
- 28nm individual transistors were probed to verify functionality
- Probing showed positive results
- Packaging may have induced ESD failures of structures (individual transistors are small and extremely sensitive)







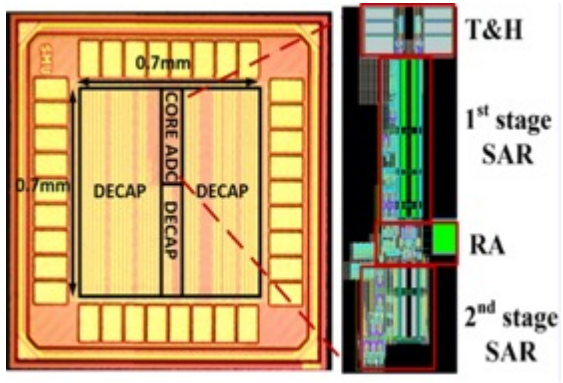


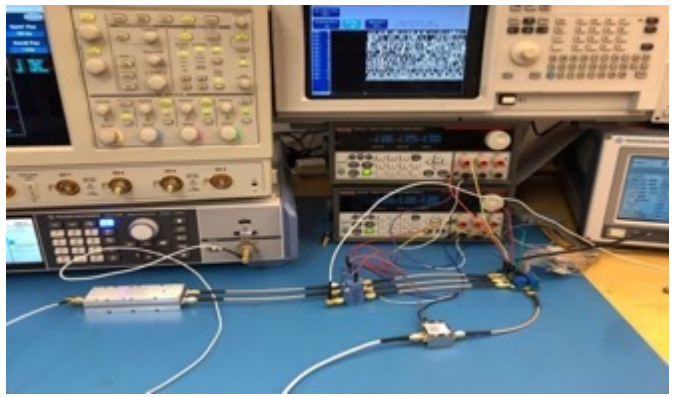


Multi-GS/s 12-bit ADCs Developed During this Project

- Two 12-bit GS/s ADCs have been developed and measured on silicon
  - 2.56GS/s 8-channel interleaved ADC in 65nm
  - 1GS/s single-channel ADC in 28nm
- Total Ionization Dose (TID) radiation tolerance tested up to 2 MRad

12-bit Single-Channel 350MS/s ADC



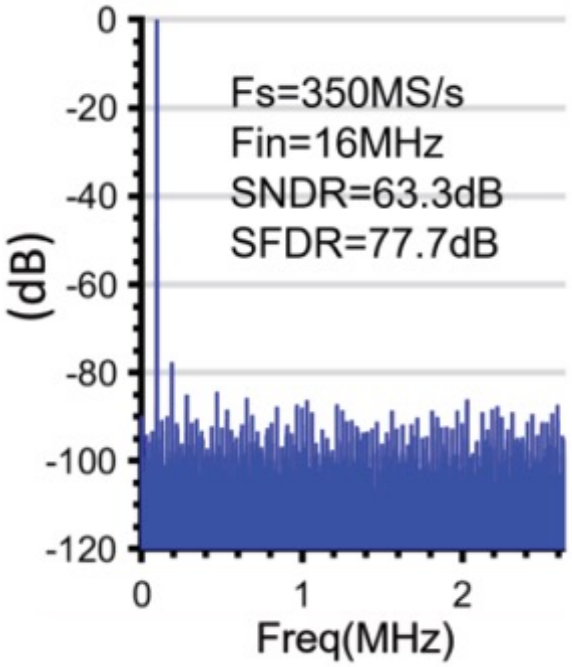


- **Pipelined-SAR architecture implemented in 65nm CMOS**

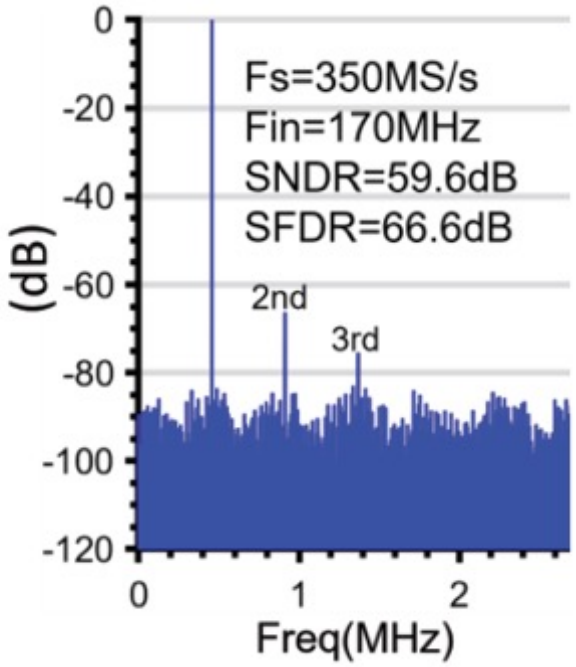
Specs	Measurement Results
Sampling Rate	Up to 350 MS/s
ENOB (Effective Number of Bits)	10.2 bits ENOB @ 30MHz and 9.6 bit ENOB at @170MHz
Power Consumption	2.86mW
Core area	0.05mm x 0.3mm
Topology	Pipelined-SAR
Technology	65nm CMOS

Measurement Results of the 12-bit Single-Channel ADC

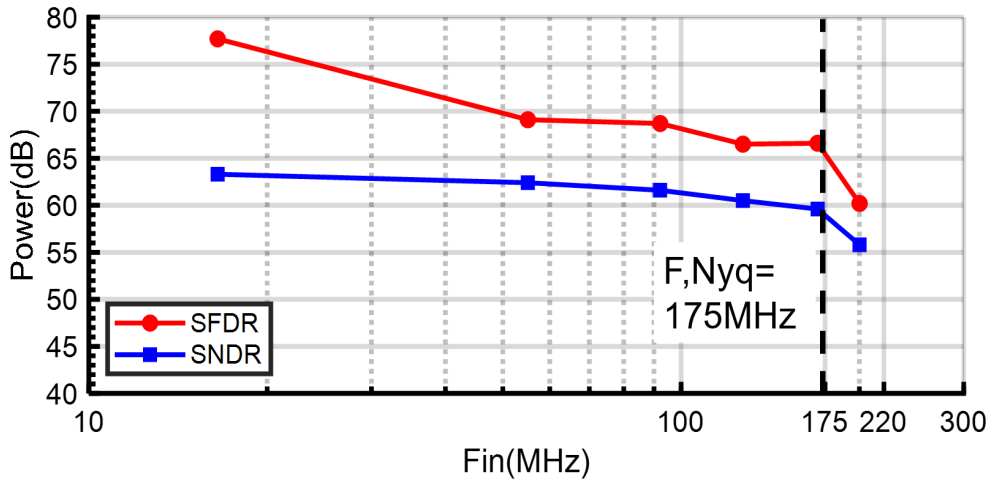
- **Measured SNDR & SFDR**
- **SNDR ⇔ ENOB = (SNDR -1.76dB) / 6.02**



- f_{in}=16 MHz, f_s=350MS/s
- SNDR = 63.3 dB
- ENOB = 10.2 bit

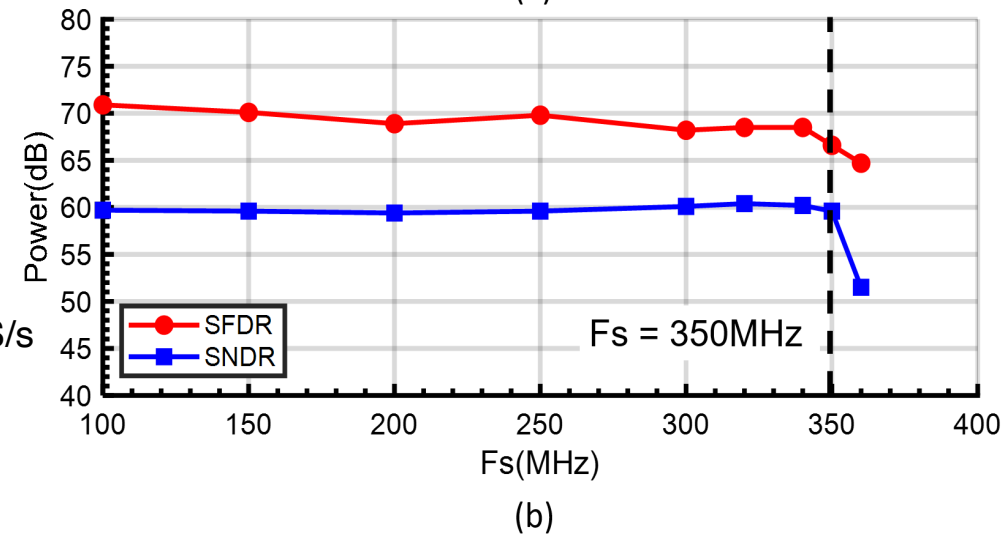


- f_{in}=170.11MHz, f_s=350MS/s
- SNDR = 59.6 dB
- ENOB = 9.6 bit



SNDR v.s. f_{in} up to f_{in} =175 MHz with f_s =350MS/s

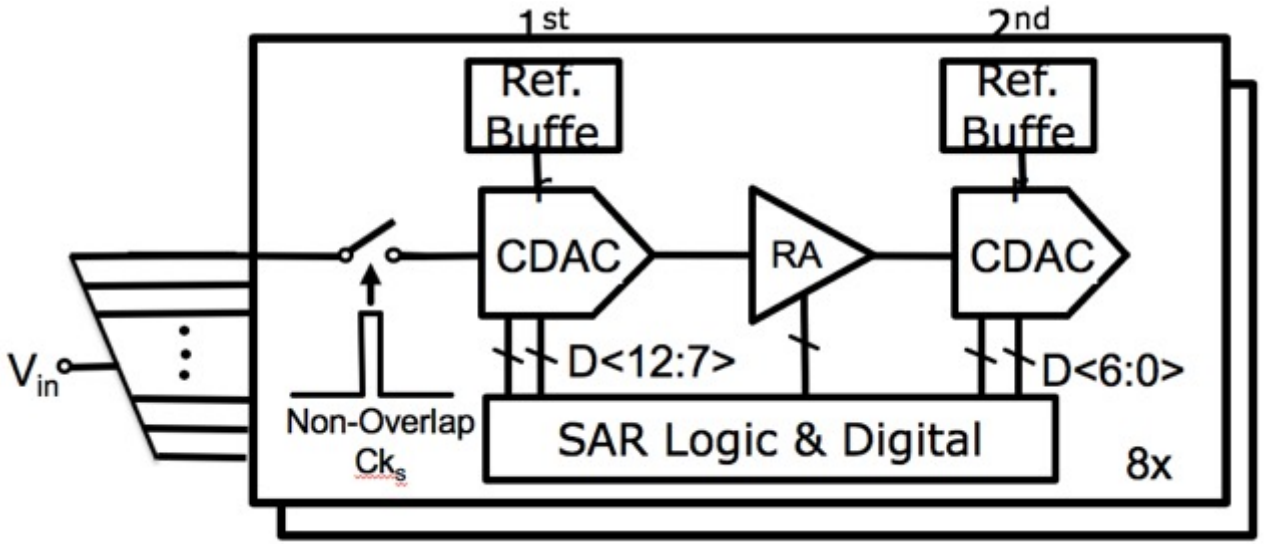
ENOB: 10.2-bit to 9.6-bit



SNDR v.s. f_s up to f_s=350MS/s (f_{in} = 0.5 f_s)

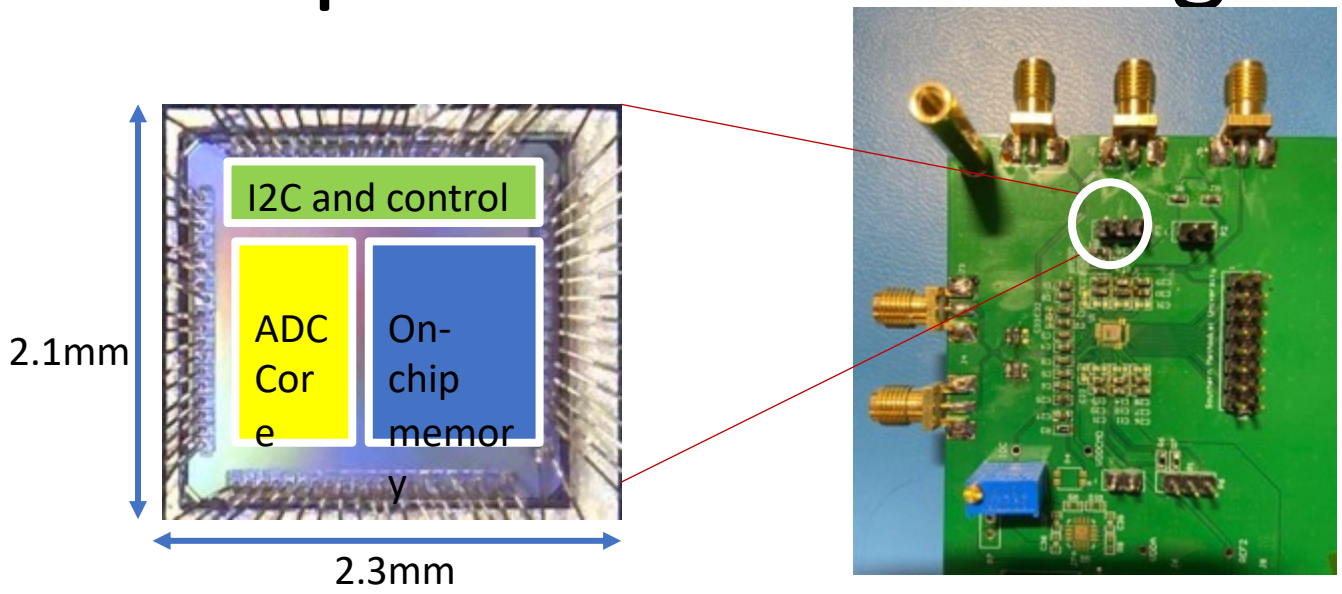
ENOB = 9.6-bit

2.56GS/s 12-bit ADC
Interleaving 8 Single-Channel SubADCs in 65nm CMOS



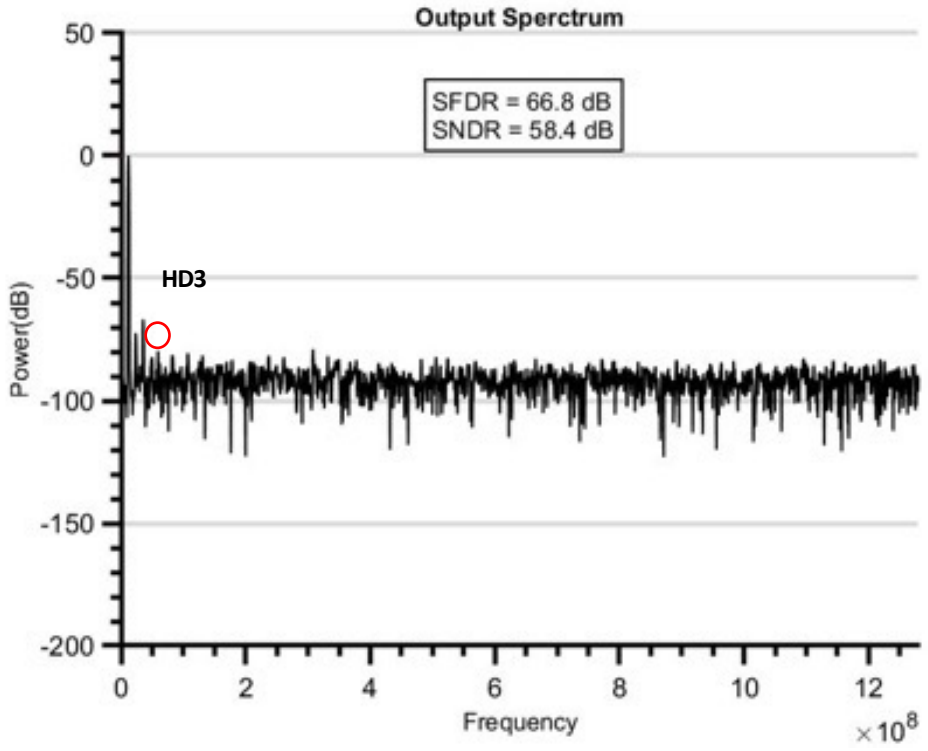
- Design challenges:
  - High sampling rate while still maintaining high resolution
- Interleaving 8 channels in time-domain to get overall sampling rate of 2.56GS/s
  - Timing skew Inter-channel mismatches
  - Intra-channel mismatches
- Various calibrations to minimize mismatches

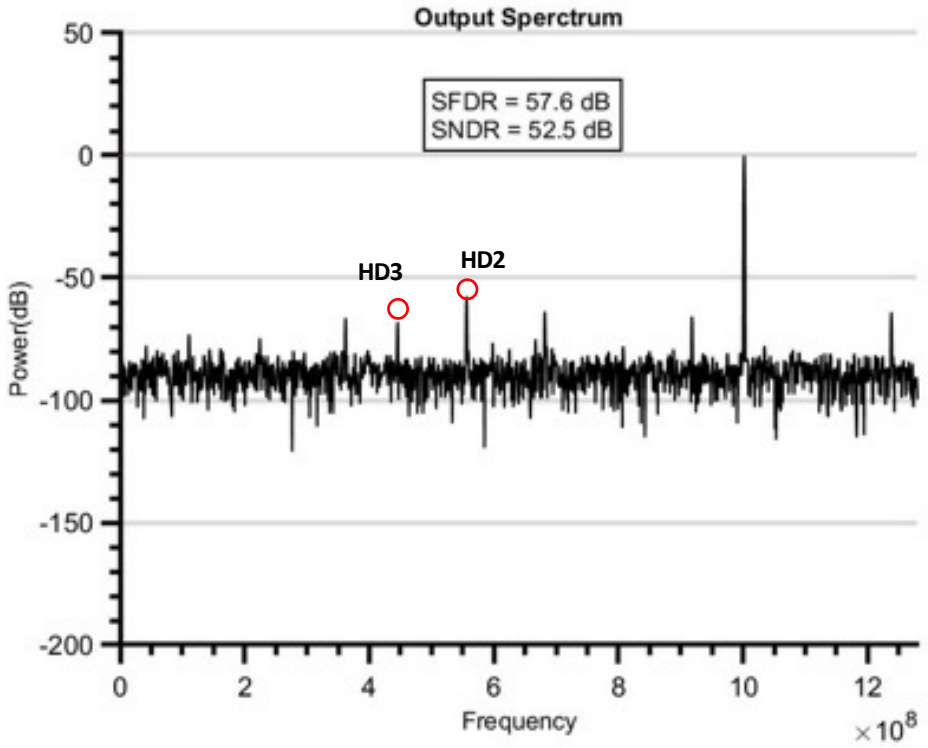
12-bit 2.56Gbps ADC Interleaving 8 Channels



Specs	Measurement Results
Sampling Rate	Up to 2.56 GS/s
ENOB (Effective Number of Bits)	9.4 bits @ 13MHz and 8.4 bit at @1GHz input
Power Consumption	92 mW (when continuous operating)
Core area	1mm x 0.8mm
Topology	Pipelined-SAR
Technology	65nm CMOS

2.56GS/s 12-bit ADC Measurement Results: Frequency Spectrum to Evaluate SNDR/SFDR





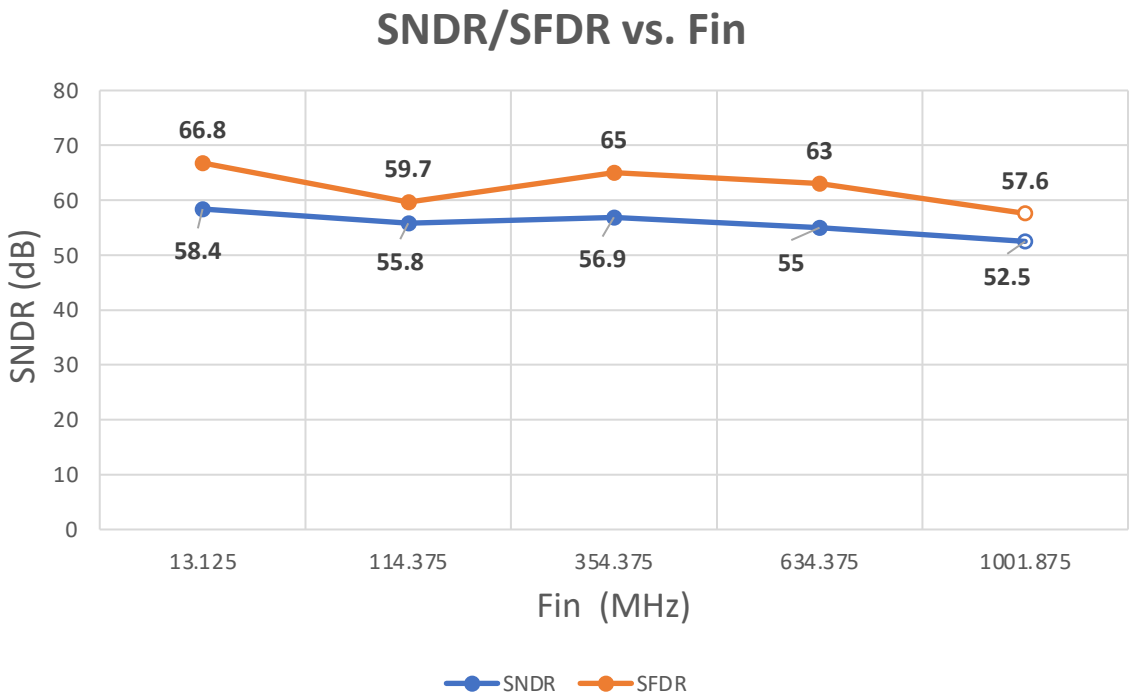
Tones other than HD2/HD3 are caused by the time skew and can be compressed by fine tuning the delay tuner(skew calibration)

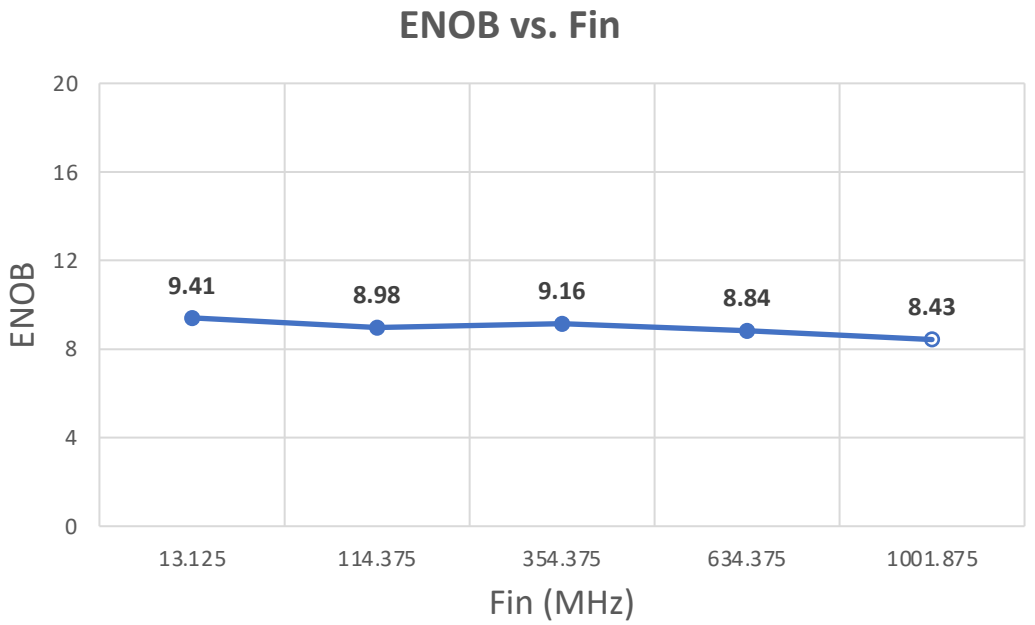
- Fin=13.125 MHz, Fs=2.56GS/s
- SNDR=58.4dB
- ENOB=9.41 bit

- Fin=1001.875MHz, Fs=2.56GS/s
- SNDR=52.5dB
- ENOB=8.43 bit

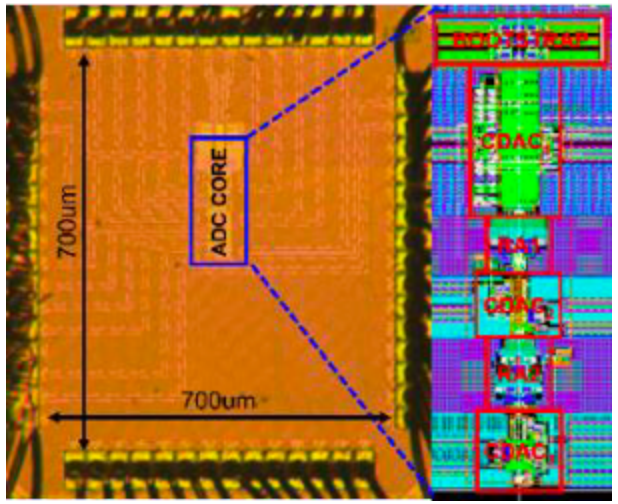
2.56GS/s 12-bit ADC Measurement Results: Dynamic Performance vs. Fin (Sampling Rate = 2.56GS/s)

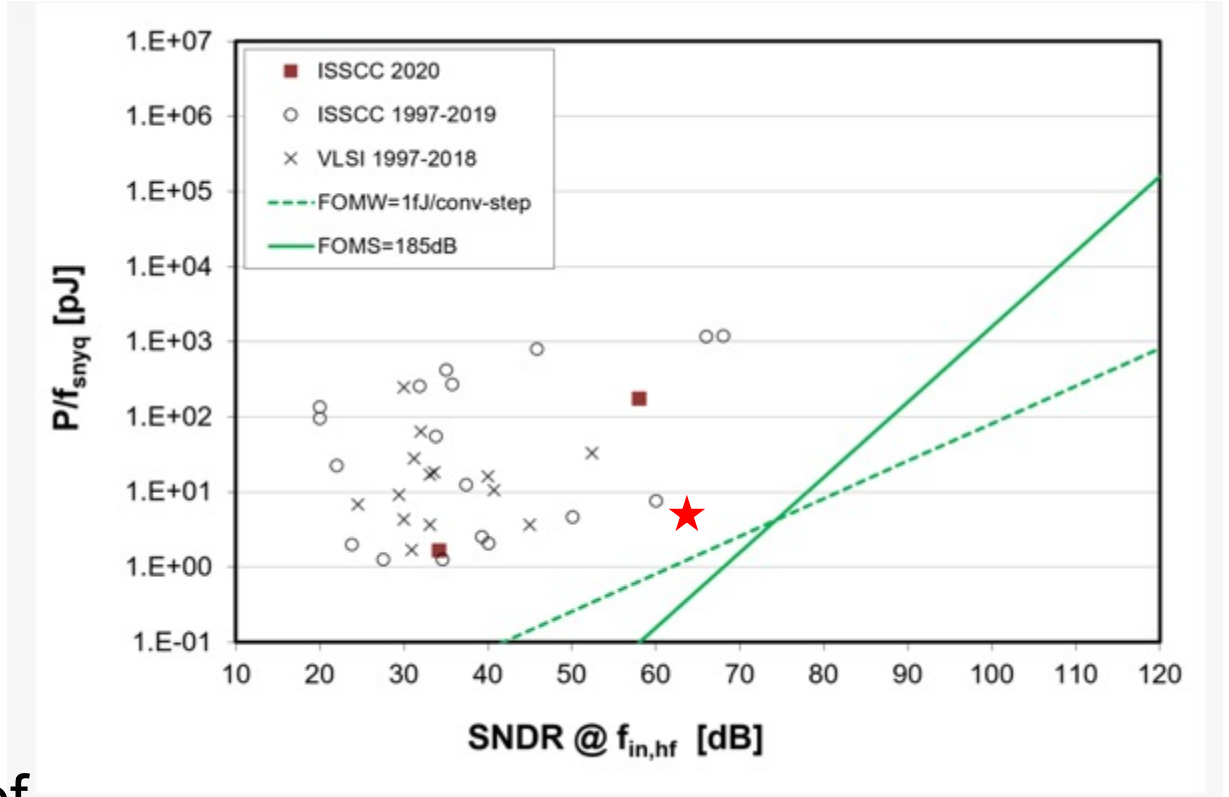
- SNDR: Signal to Noise and Distortion Ratio
- SFDR: Spurious Free Dyanmic Range
- ENOB: Effective number of bits; ENOB = (SNDR-1.76dB) / 6.02





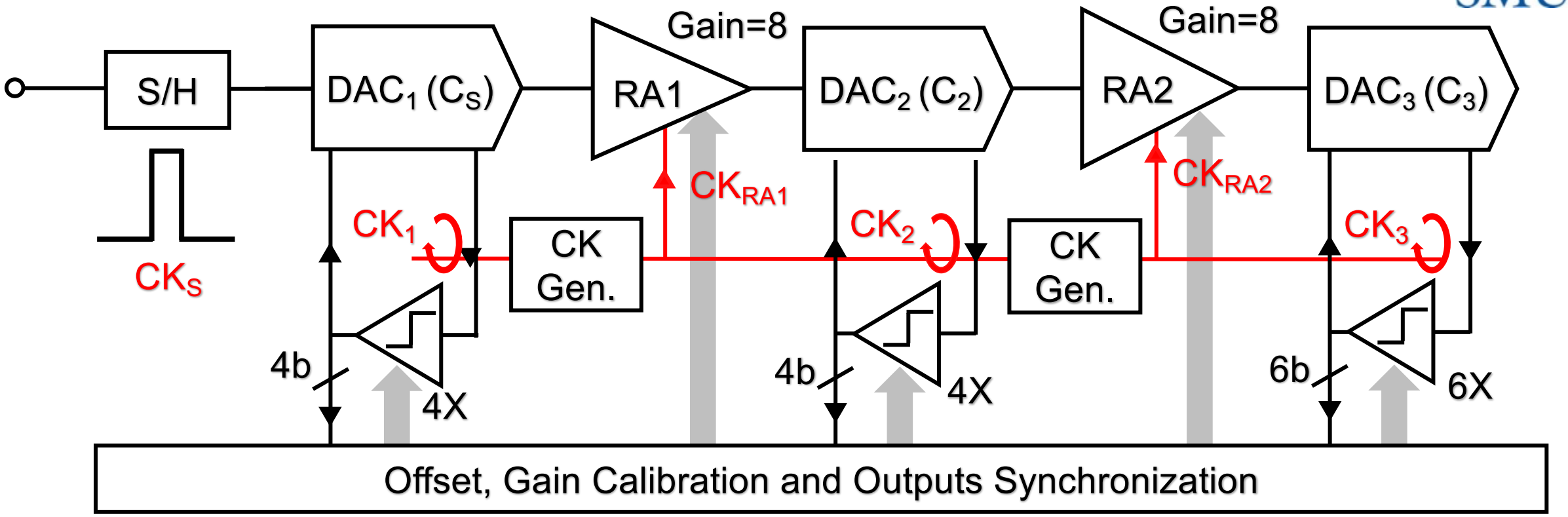
12-bit 1GS/s Single-Channel ADC in 28nm CMOS





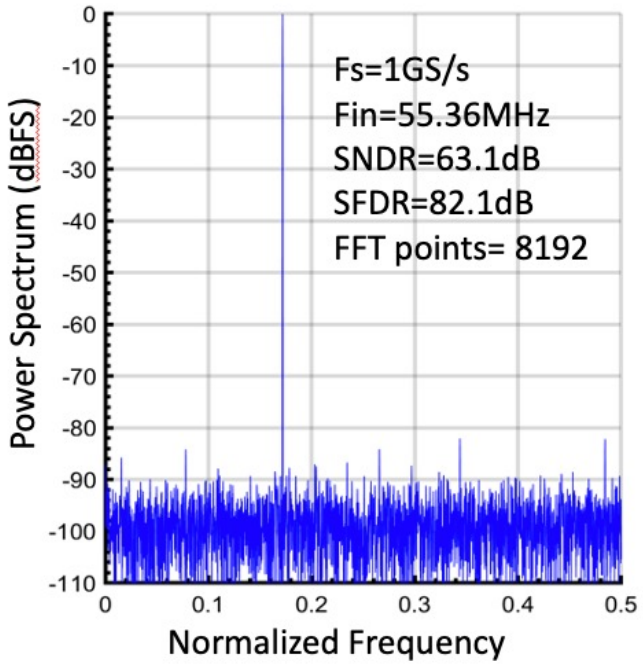
- 3-stage pipelined SAR architecture to achieve the targeting sampling rate and resolution with excellent power efficiency
- At Nyquist input, 1GS/s, SFDR ≥ 73dB, SNDR=61dB, ENOB=9.8 bits total power of 6.7mW, area of 0.12mm^2

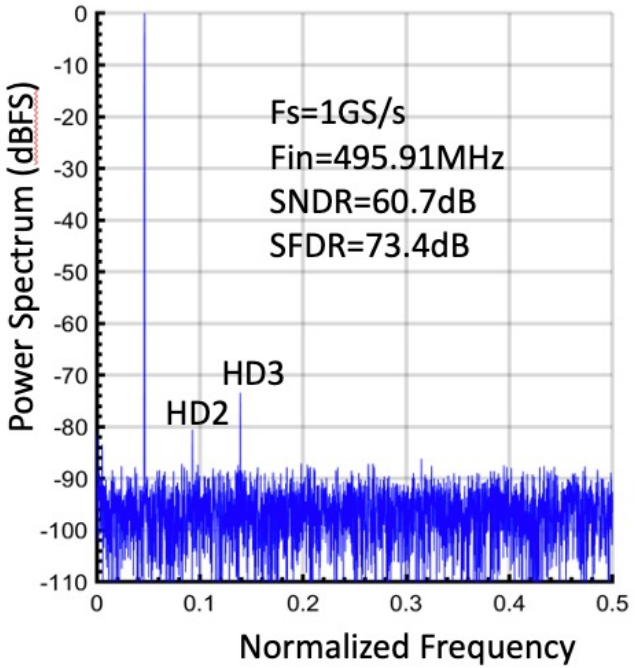
1GS/s 12-bit Pipelined SAR ADC Architecture

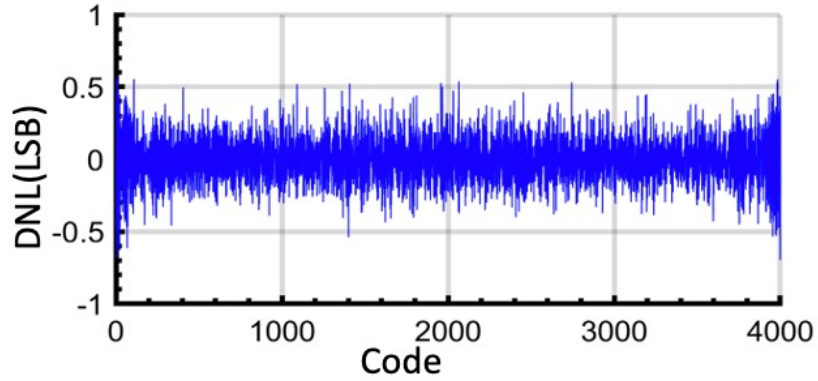


- Three stage asynchronous pipeline SAR ADC
- CDAC1/2/3: 4b/4b/6b (1b interstage redundancy)

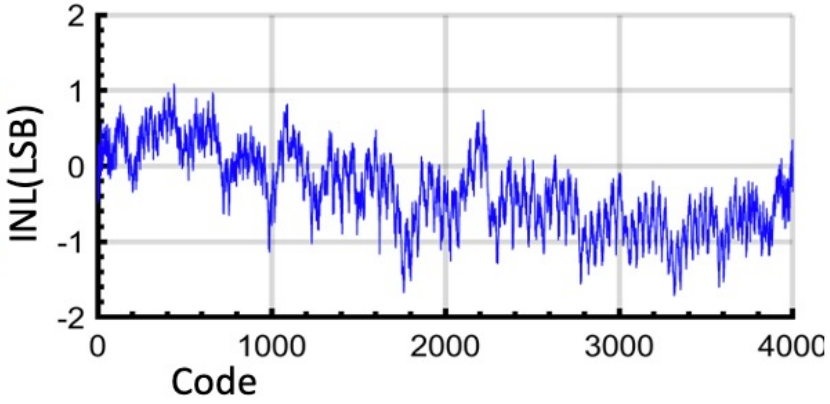
12-bit 1GS/s ADC in 28nm CMOS Measurement – Frequency Spectrum and DNL/INL







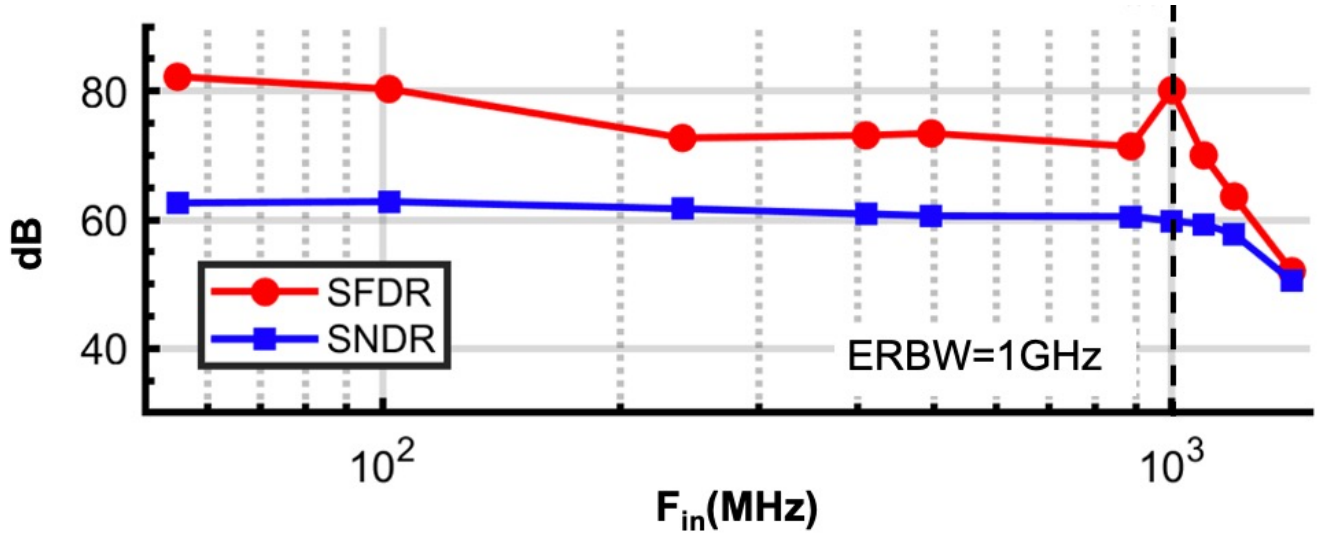
DNL=+0.56/-0.67LSB

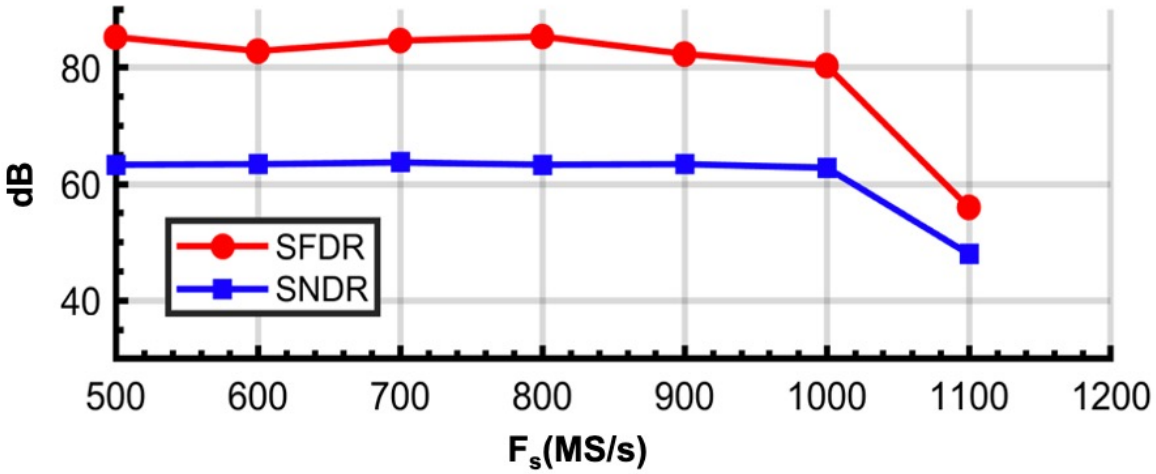


INL=+1.09/-1.72LSB

- @low Fin, SNDR=63dB, SFDR =82dB, ENOB =10.1bits
- @Nyquist input, SNDR=61dB, SFDR =73dB, ENOB =9.8bits

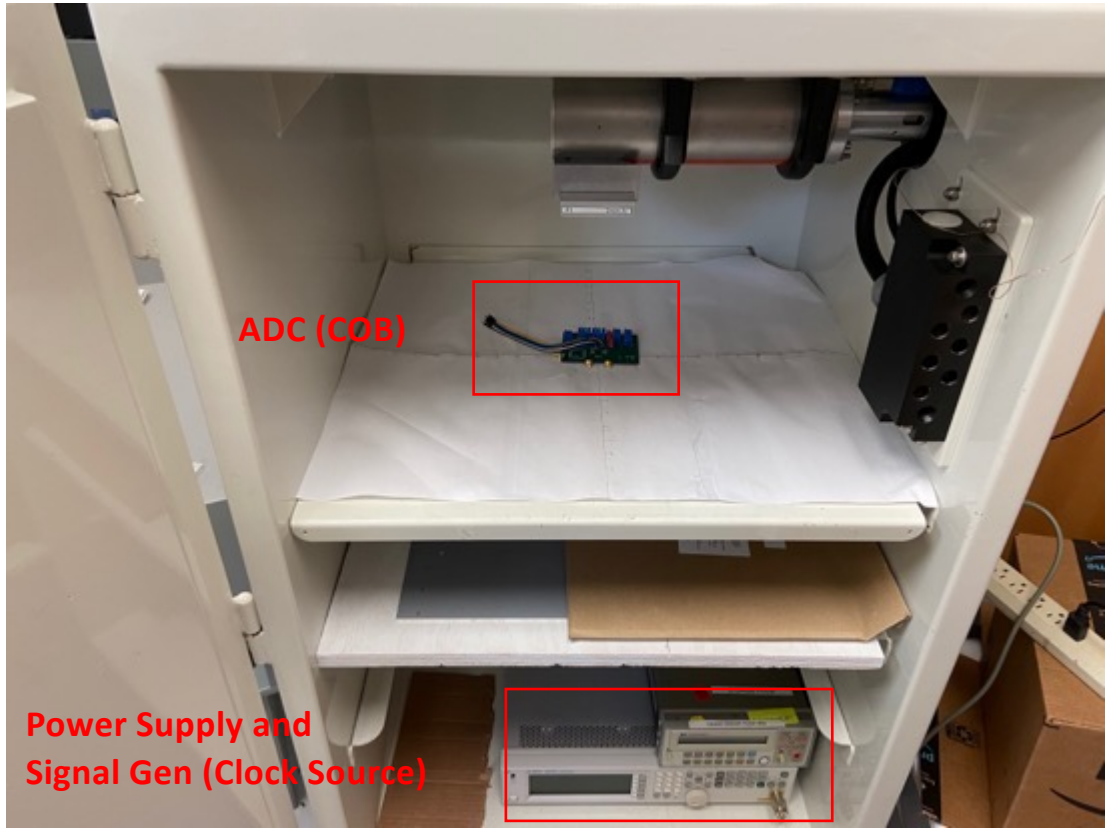
12-bit 1GS/s ADC in 28nm CMOS Measurement
- Sweep Input Frequency F_{in} and Sampling Frequency F_s





- @Nyquist, SFDR=73dB, SNDR=61dB, ENOB =9.8 bits

Total Ionization Dose (TID) Testing Setup

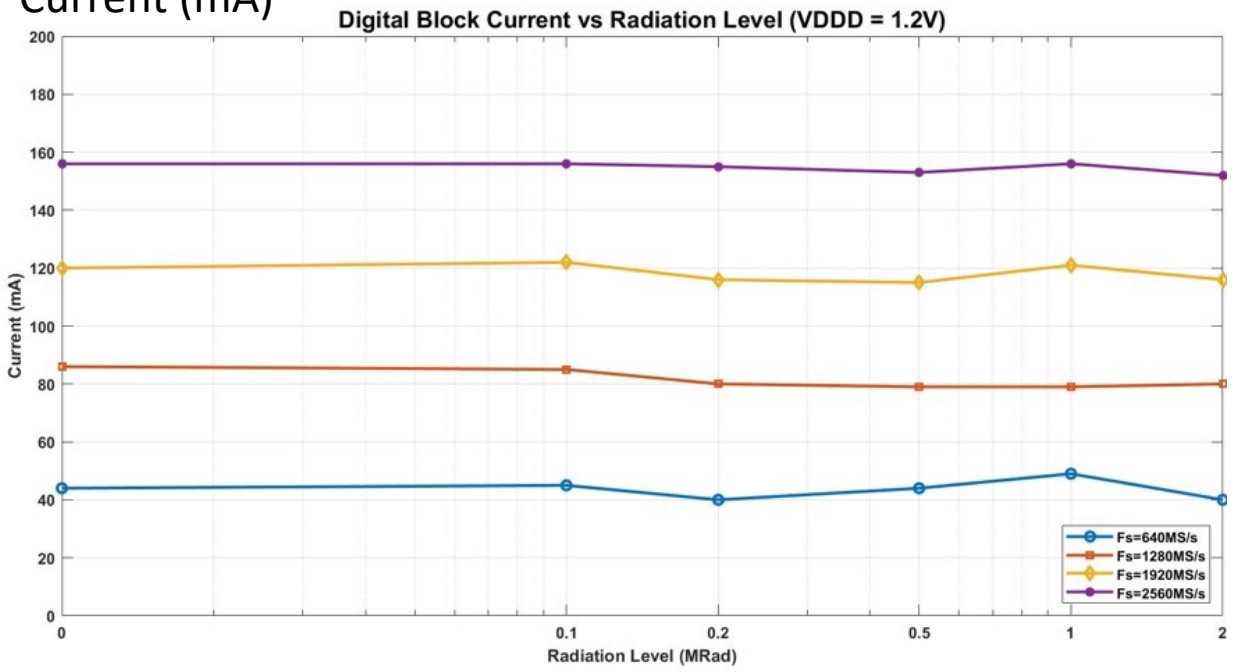


- The ADC COBs were put in the X-ray radiation chamber at SMU with maximum dose rate (18Rad/s).
- The ADC chips were powered on and a fast sampling clock was provided during the radiation test
  - Power supply for DC biasing of the chips was put in the radiation chamber.
  - The signal generator that provides the fastest sampling clock was put in the radiation chamber.
  - Other power supply for the ADC was put outside of the chamber for current monitoring.
- Radiation Test points:
  100krad, 200krad, 500krad, 1Mrad, 2Mrad

65nm 2.56GS/s ADC: Current vs. Radiation Level

Digital Power Domain with VDDD = 1.2V, 1,08V and 1.32V

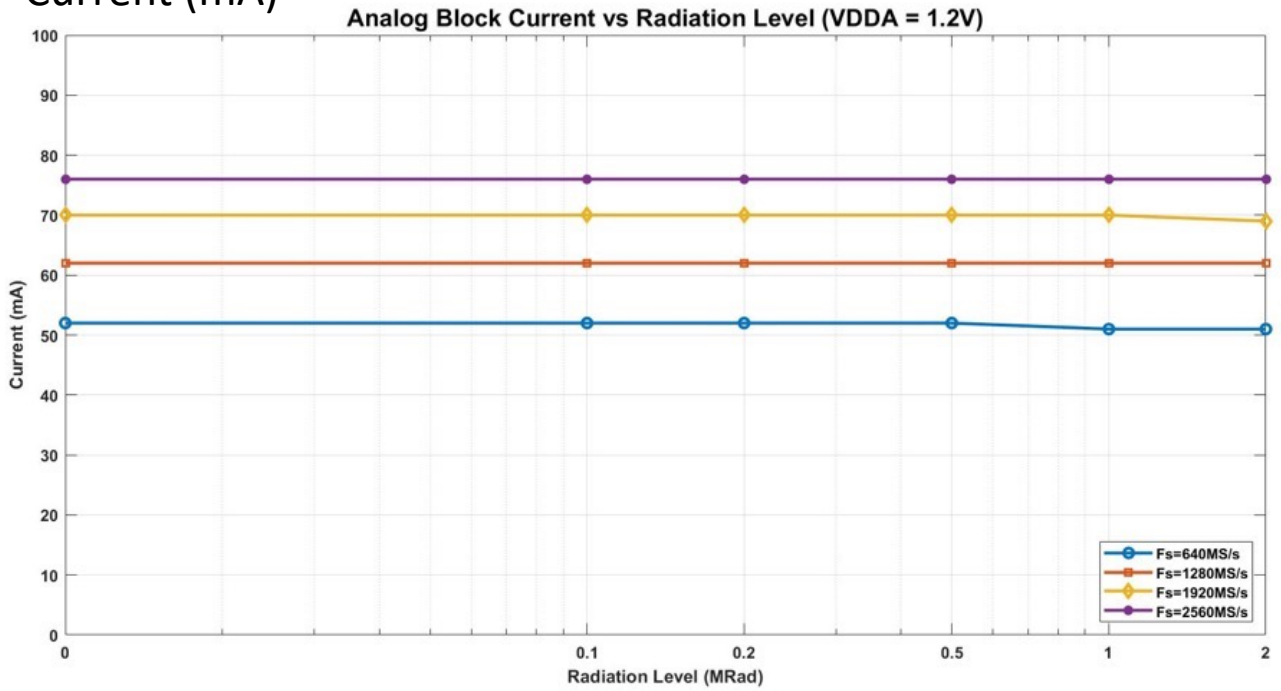
Current (mA)



TID (Mrad)

Analog Domain with VDDA = 1.2V, 1,08V and 1.32V

Current (mA)

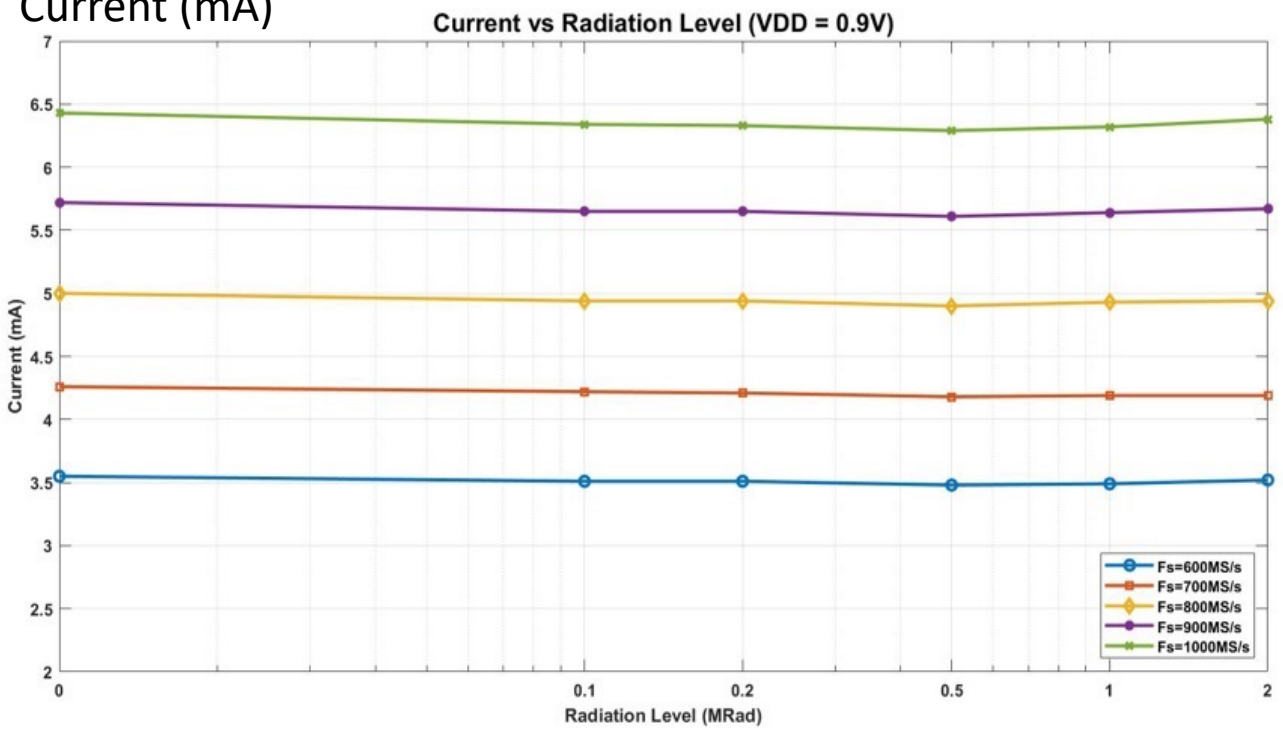


TID (Mrad)

Negligible variation on the current drawn from either the digital domain or analog domain from pre-rad to 2MRad

28nm 1GS/s ADC TID Measurement

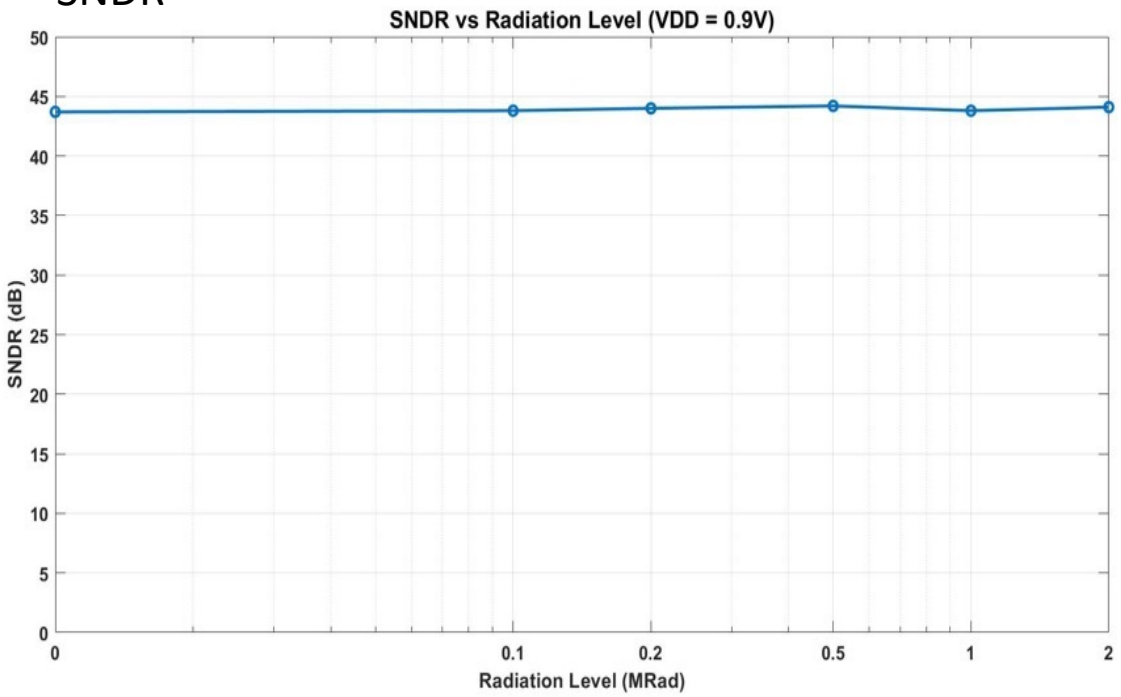
Current (mA)



TID (Mrad)

Negligible variation on the total current drawn from the chip with TID radiation tested up to 2Mrad (also tested at various sampling clock frequencies

SNDR



TID (Mrad)

No degradation on the SNDR performance (without calibration) with TID tested up to 2MRad

Summary

- Project progressed as per the plan, with some impact from COVID-19 lockdowns at SMU.
- Two GS/s 12-bit ADCs have been developed and measured on silicon
  - 2.56GS/s ADC interleaving 8 channels in 65nm
  - 1GS/s ADC in 28nm
- 1-year NCE was granted which allowed us to conduct the radiation test of the chips
- The two ADCs chips have also been tested under TID using X-ray up to 2MRad
  - Both chips were radiation tolerant with no noticeable leakage current increase or performance degradation
  - SEE testing delayed and will take place before the end of the year.
- Certain targets may not be realizable within the budget/schedule, such as the extension to 16 channels and the implementation of a high-speed interface, but the proposed core technology is being proven successfully.
- Company will seek additional funding to productize the technology.