Low Cost Data Acquisition Synchronization for Nuclear Physics Applications

Wojtek Skulski

Principal Investigator

DE-SC0018467

Performed in collaboration with Argonne National Laboratory

SBIR Exchange, August 18, 2021, 16:40pm

SkuTek Instrumentation
SkuTek.com

Outline

- Outline
  - The company and its capabilities.
    - Customers.
    - Success Story: LUX-Zeplin DAQ deployment.
  - Description of the Phase I project: Proof of principle.
  - Description of the Phase II project: The goal.
  - Phase II progress and achievements.
  - Highlights of the final products.
  - Plans.

The company and its capabilities

- The team: three physicists, a senior software engineer, a part time engineering associate, and a manager. We regularly work with a local EE consultant.
- We worked with several interns listed on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, DM search, etc.

Our capabilities: Development of cutting edge instruments.

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, especially Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in the FPGA (VHDL, Verilog) and in embedded processors (Pascal, Python, C).
- Processing data from nuclear detectors of any kind.
- Development of simple detector assemblies using scintillators, PMTs, or SiPMs.

Our customers

University of Rochester

Houghton College

The University of Tennessee Knoxville

SFU Simon Fraser University Engaging the World

Université Laval

Augustana University

上海交通大學 Shanghai Jiao Tong University

Los Alamos National Laboratory

Fermilab

Brookhaven National Laboratory

Added last week!

NSCL National Superconducting Cyclotron Laboratory

Albert Einstein Center for Fundamental Physics

Universität Bern

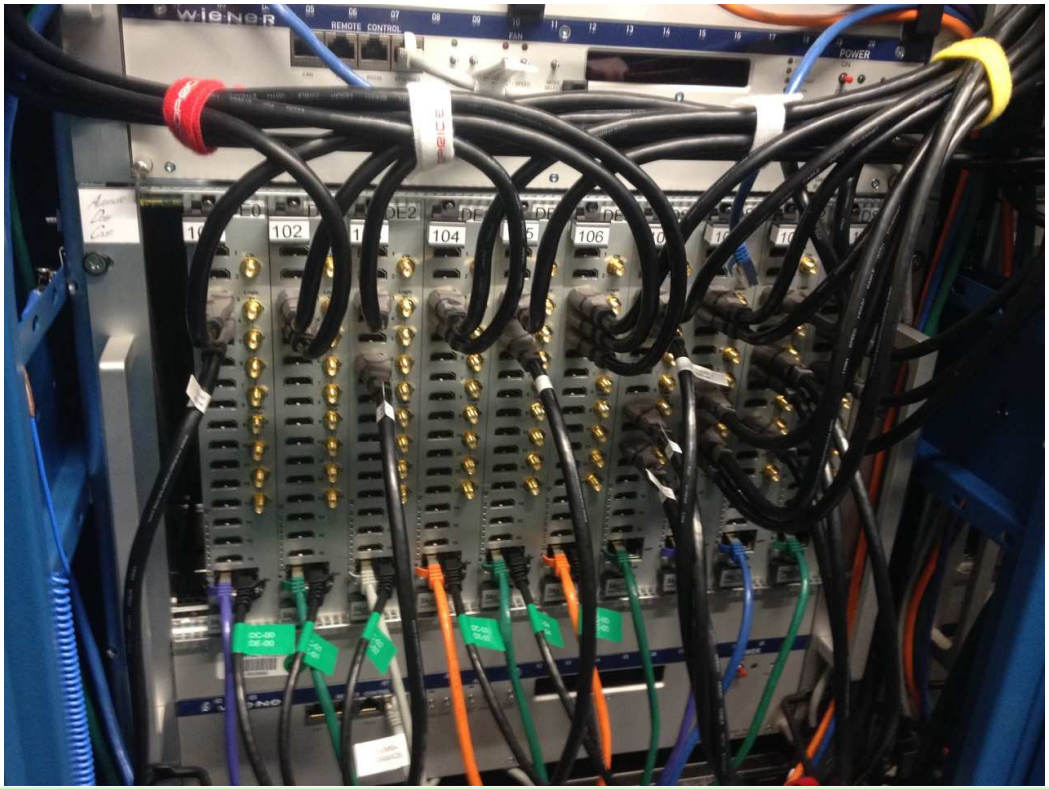
Brown University

Wiener Plein & Baus, Corp.

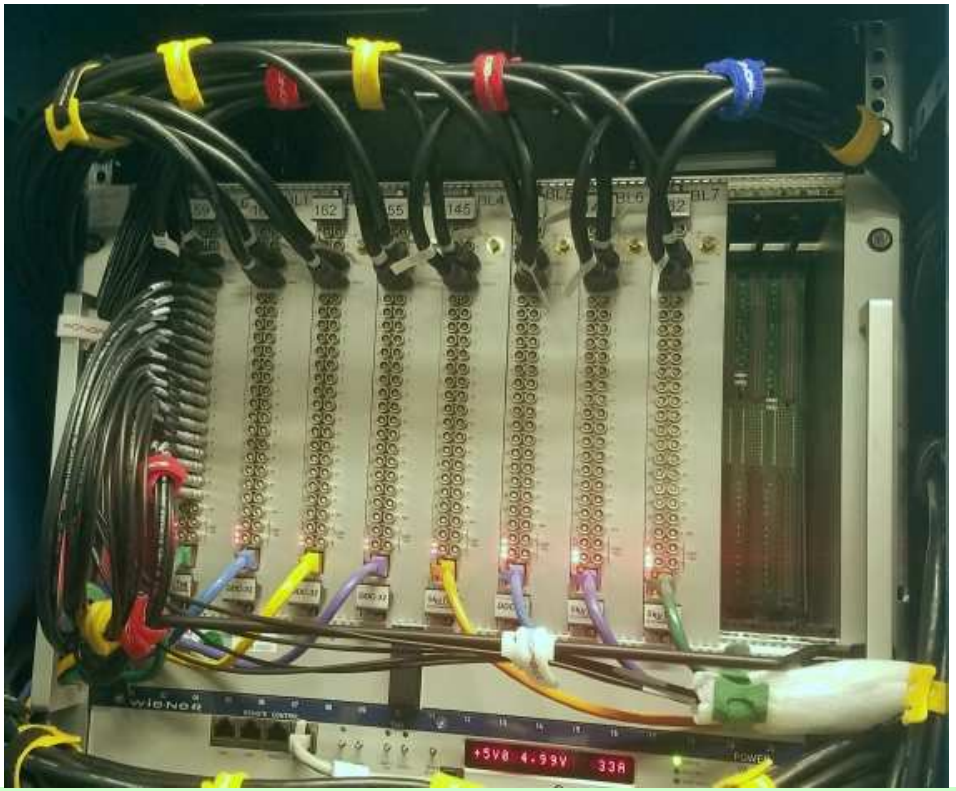
Success Story: LUX-Zeplin Data Acquisition

- LUX-Zeplin is the world's largest Dark Matter Search liquid xenon two-phase TPC (10 ton LXe).
- We delivered **1,632 channels** of the DAQ electronics to the LZ Collaboration.
- No bad channels.
- The DAQ was deployed in Sanford Underground Research Facility at -4850' in Summer 2019.
- No problems were found with the DAQ while collecting signals since November 2019.
    - Continuous operation since deployment without any failures.

26 Logic Boards, sixteen 4 Gbps links each



51 Digitizers, 32 channels each



The Goal of the SBIR Project

The Goal of the SBIR Project

Problem or situation that is addressed.

GRETINA and Digital Gammasphere (DGS) both use LBNL 10-channel digitizers. Although the hardware units are still in good shape, the legacy VME interface is limiting the data throughput . Additionally, the Spartan-3 FPGAs are filled with the present firmware to about 90%. It makes the new firmware developments rather difficult.

How this problem or situation is addressed.

We proposed new digital DAQ modules with a ***new FPGA*** generation and on-board ***Linux*** for setup & control. The *readout* and the *setup & control* paths will be ***optimized*** for their respective tasks. The digitizers will be ***backward compatible*** with the GRETINA & DGS and ***forward compatible*** with GRETA.

Phase I provided a proof of principle.

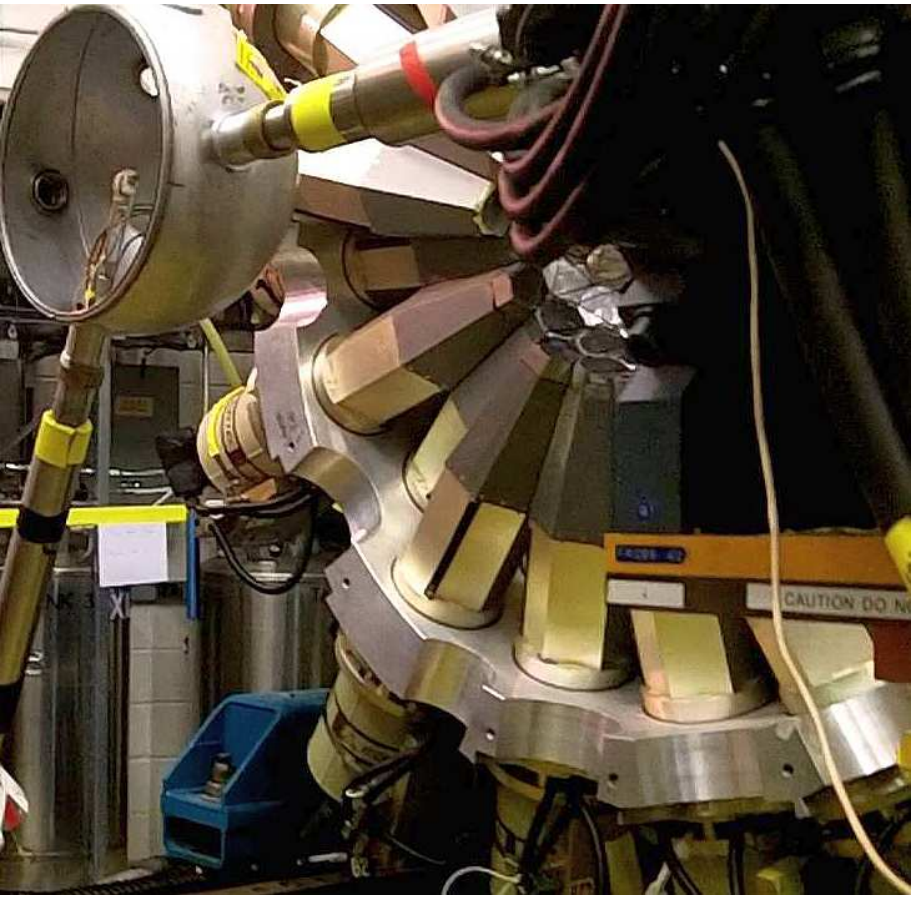
In Phase I we performed measurements with Gammasphere, using our hardware prototypes in parallel with the present LBNL DAQ electronics. The goal was to evaluate whether or not our prototypes would perform on par with the established LBNL units.

Digital Gammasphere (DGS)

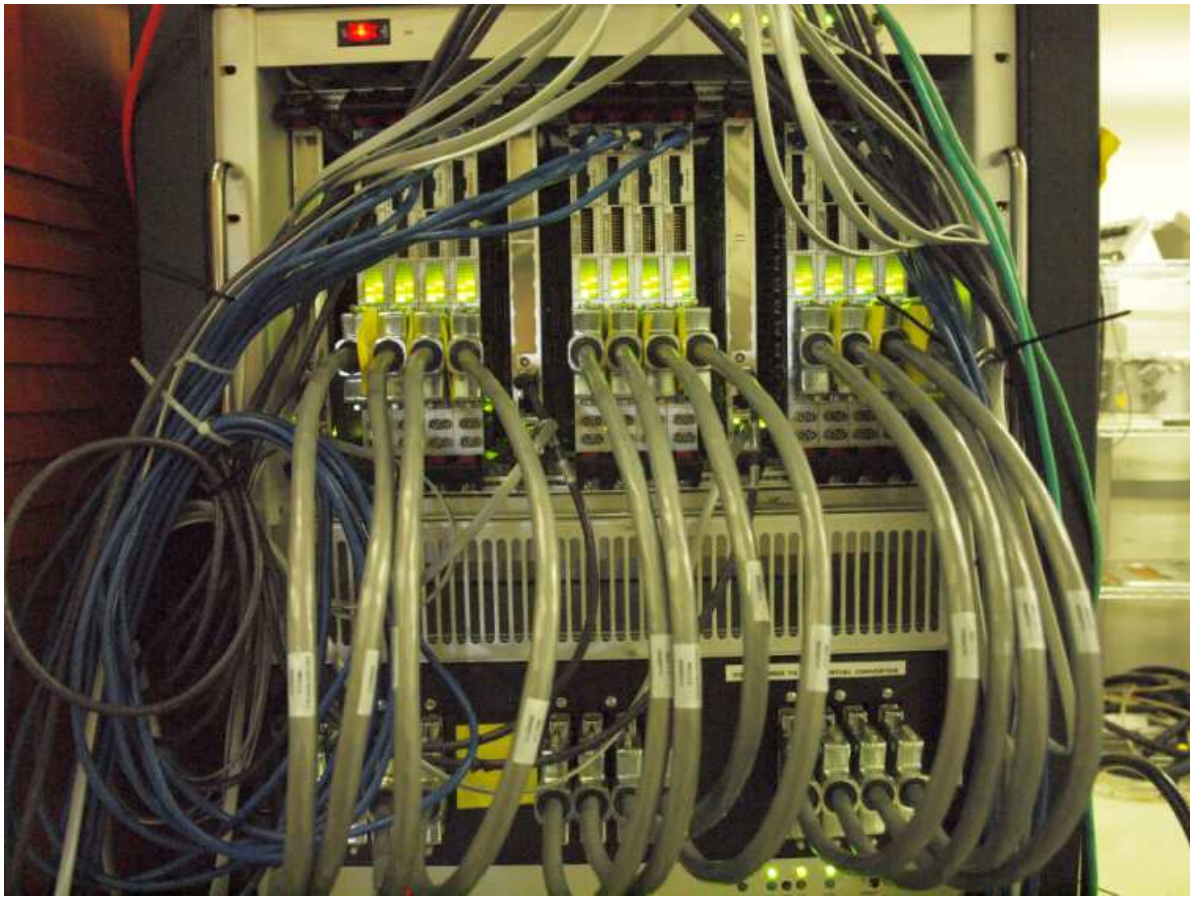
Gammasphere consists of 108 Compton-suppressed high-purity germanium (HPGe) detectors surrounded by the BGO anti-Compton shields.

The Digital Gammasphere is equipped with the digital electronics originally developed by LBNL for GRETINA. Each LBNL digitizer provides 10 channels, 14 bits @ 100 MSPS.

Gammasphere Detector Array



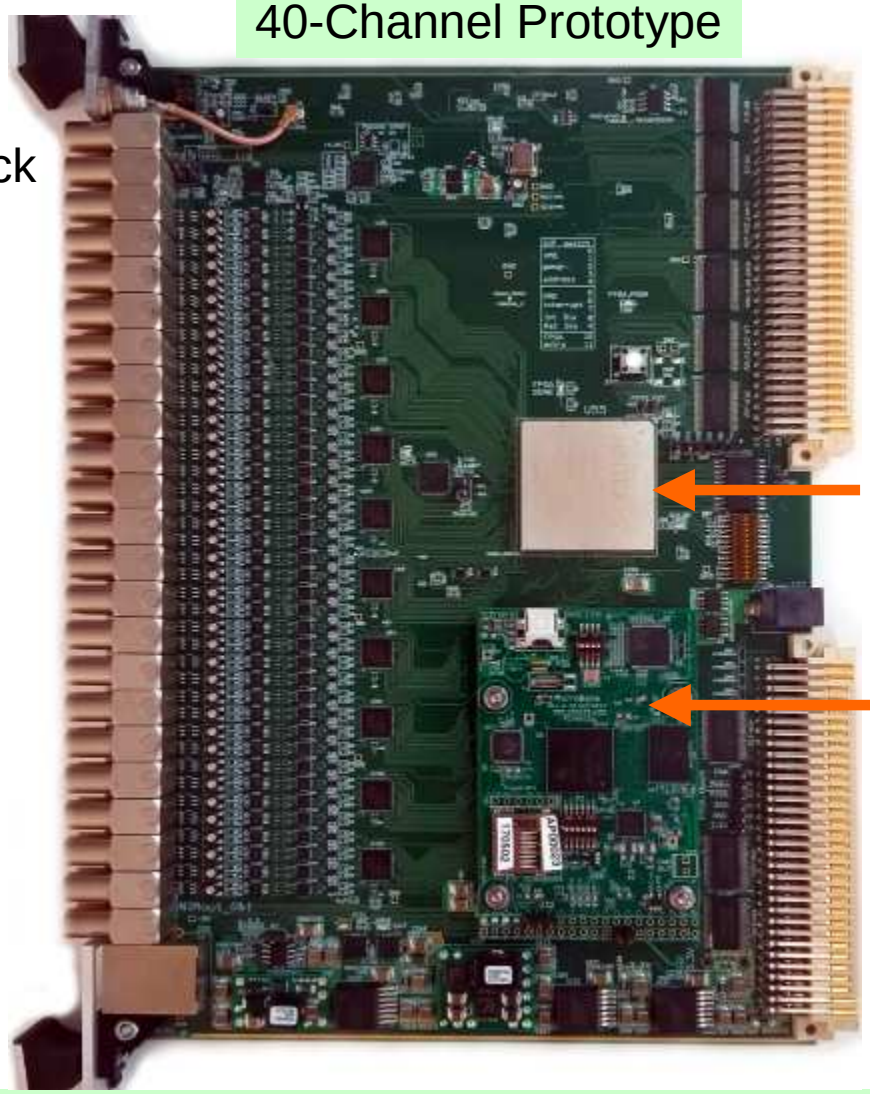
Digital Gammasphere LBNL Electronics



We Used 40-Channel Prototype by SkuTek

- In **Phase I** we used the 40-channel prototype, 14 bits @ 100 MSPS.
- We used the on-board Linux to setup the digitizer and to collect the waveforms.

40-Channel Prototype



Optional external clock
Four NIM in
Four NIM out

40 analog inputs

GbE over RJ-45

VME interface. We never used it as VME! Only for power…
Time to retire the VME bus?

Kintex-7

ARM processor running Linux
1GHz clock, 512 MB of RAM
Parallel memory interface to FPGA
GbE interface to front panel
Event readout at ~10 MB/s

Prototype Installation at ATLAS Counting House

In **Phase I**, we installed our 40-channel prototype DDC-40 alongside the current DGS system. The clock, trigger, and trigger validation were shared between the DGS and DDC-40, using LEMO cables. The two systems collected **the same events** with synchronized time stamps.

SkuTek 40-channel prototype digitizer

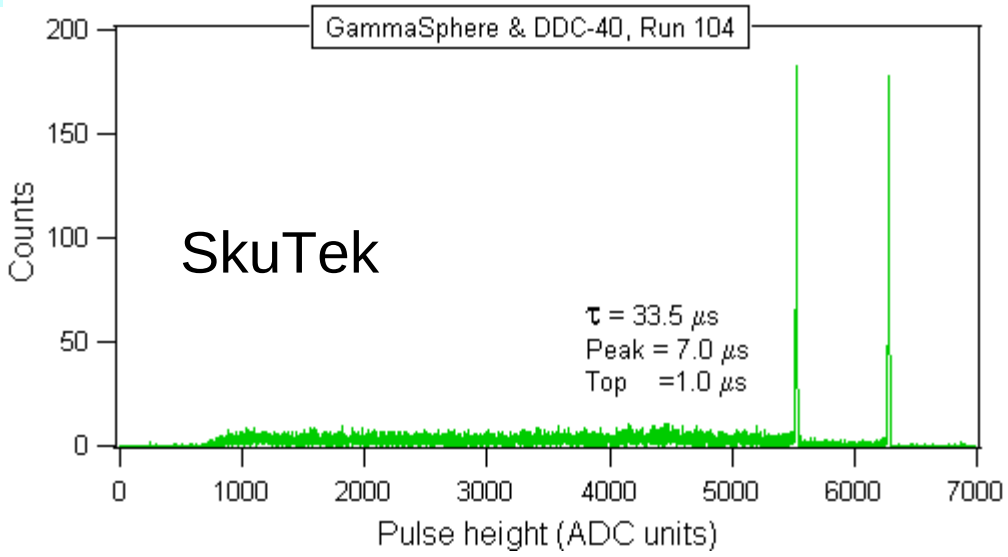
LEMO cables to SkuTek prototype

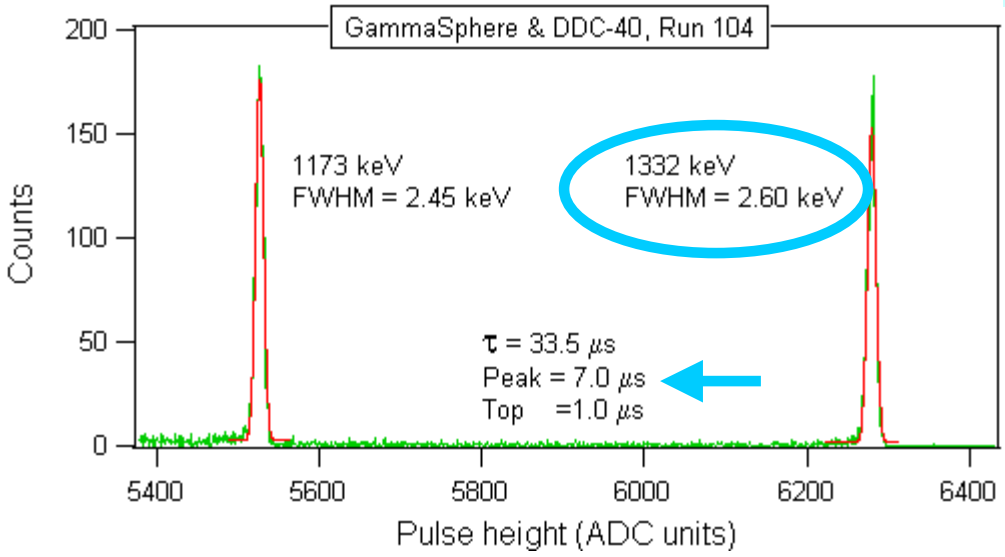
DGS digitizers

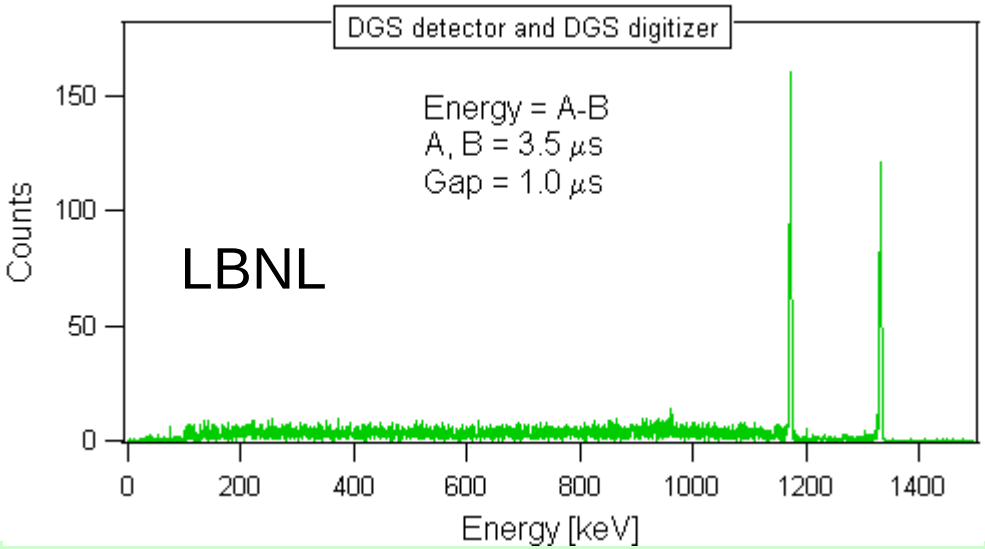
DGS signal cables

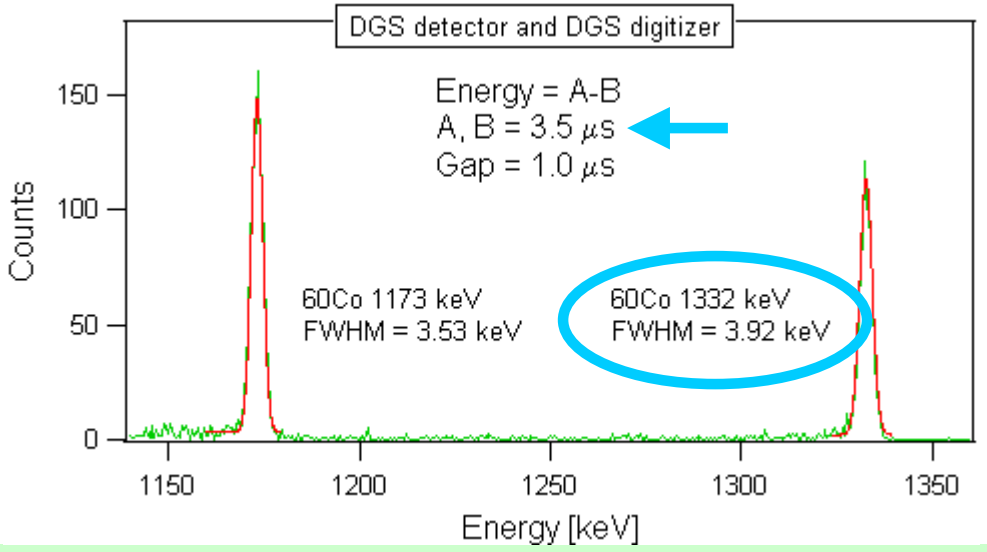
Phase I Was a Great Success

- Comparing the energy resolution with Co-60 and Gammasphere --> **PASS**!
- The resolution achieved with both devices was the same with equal running sums. We achieved a SQRT(2) better resolution when we applied 2 * *longer running sums*.









Phase II Project

Phase II Project

The challenge:

How can the digitizers be **interfaced with** and **integrated into** the established GRETINA or DGS environments which are providing clock, trigger, and time stamp synchronization among many digitizers and logic modules?

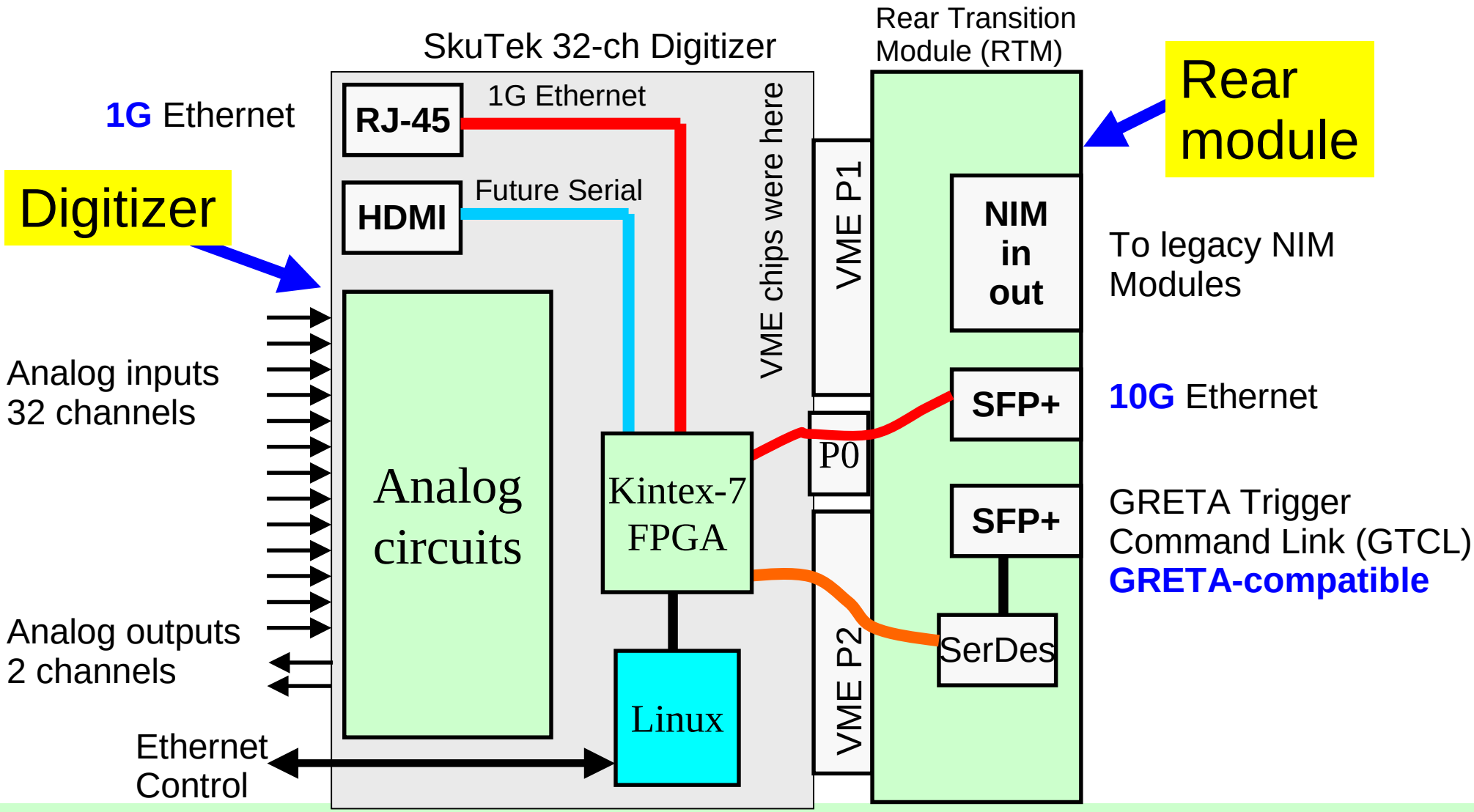
How this problem or situation was addressed:

We proposed a **modification** of the digitizer used in Phase I, replacing the VME interface with **gigabit Ethernet** of two variants: 1G and 10G. The on-board Linux will serve for setup and control over Ethernet. The modules will be linked with the GRETINA / DGS using the Optical GRETA Trigger Command Link (GTCL), forward-compatible with **GRETA**.

The development is performed **in collaboration** with the ANL Physics Division.

Conceptual Hardware Diagram

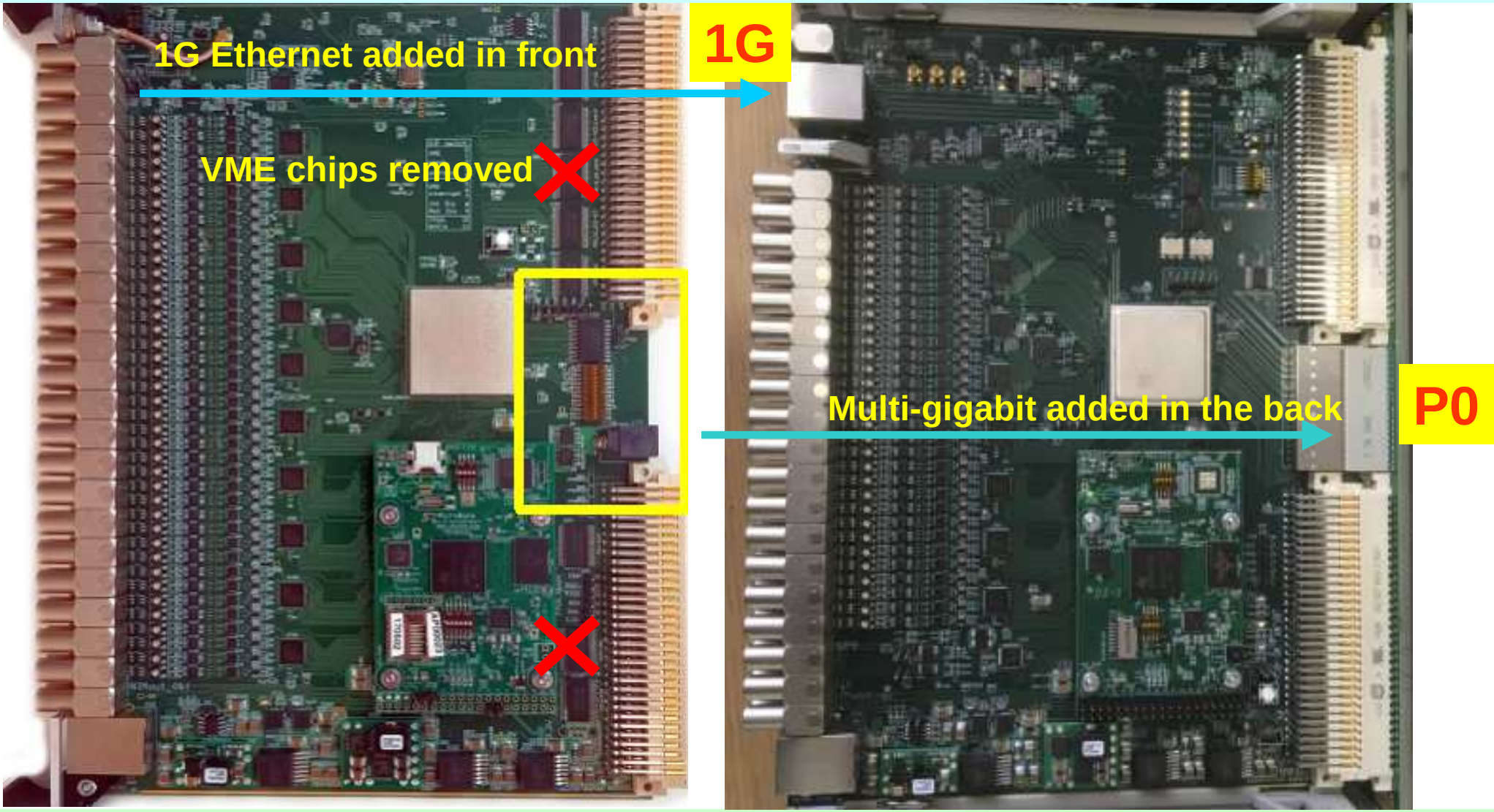
- VME interface to be removed. Setup and control will be performed over Ethernet with Linux.
- **1G** readout implemented in the front (up to ~110 MB/s). **10G** in the back (10x faster).
- Heavy duty (and possibly noisy!) interfaces moved to the Rear Transition Module: 10G Ethernet and GRETA Trigger Command Link (GTCL).



SkuTek Adding the Fast Data Transfer to the Digitizer

We **removed** the legacy VME chips (marked **X**). We **added** the Hard Metric P0 multi-gigabit connector in the space between P1 and P2. We **also added 1G** Ethernet to the front.

The digitizers can be operated in the legacy plain VME crates, and still deliver ~ 110 Mbytes/s per digitizer. The back panel 10G will work in VME64x crates. It will deliver ~ gigabyte per second from every digitizer.

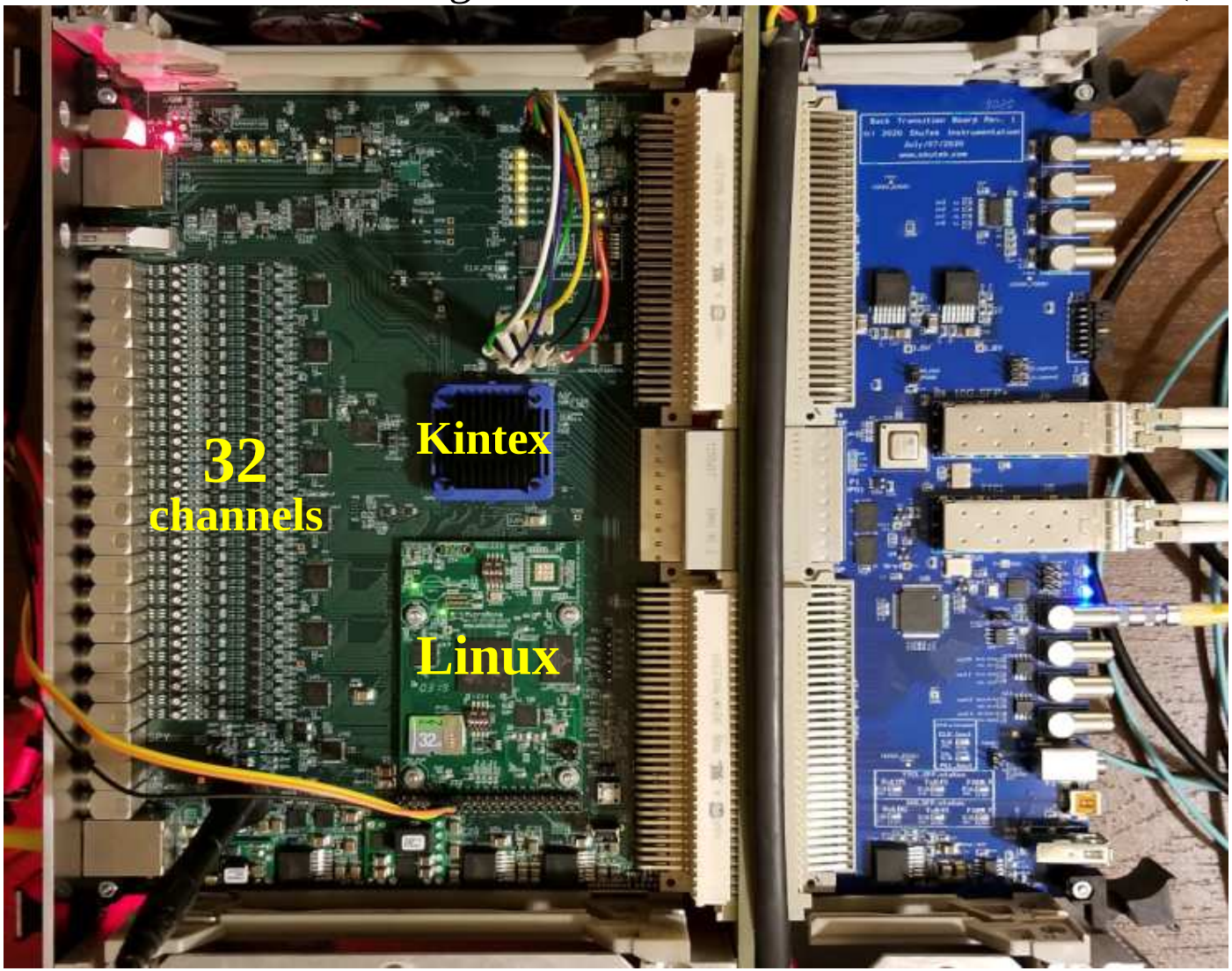


32-Channel Digitizer With the Rear Transition Module

We **achieved** the design goals: 4 Gbps over the GTCL optical link (in the 1st RTM iteration), and **10 Gbps** over the Ethernet link (in the 2nd RTM iteration).

32-Channel Digitizer

Rear Transition Module (RTM)



1 GbE (FPGA)

Digital HDMI

32 Analog inputs

2 Analog outputs

1 GbE (Linux)

4 * NIM in

10 G Ethernet

Optical GTCL **Compatible with GRETA**

4 * NIM out

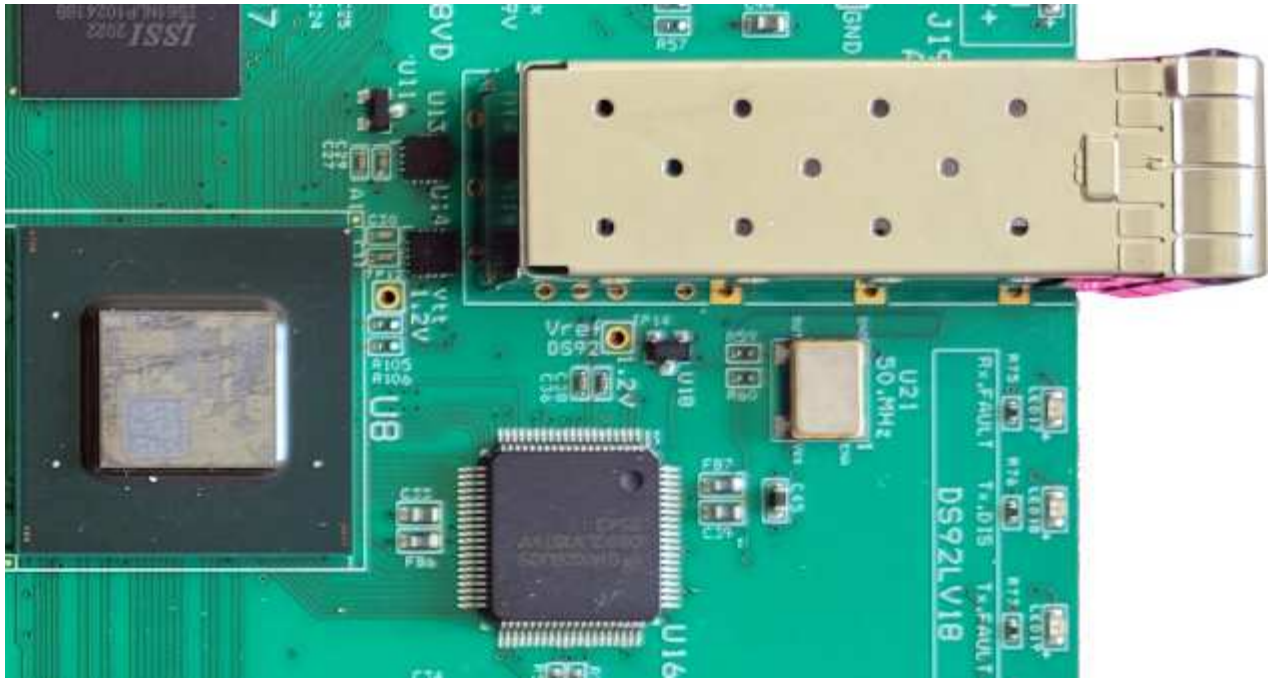
Serial UART (Linux)

Tying it All Together: System Integration

How to connect hundreds of digitizers into a single, coherent DAQ system?

The answer: GRETA Trigger Command Link (GTCL)

GTCL was designed by John Anderson, Argonne National Laboratory



Board layout by WS, SkuTek Instrumentation

GRETA Trigger Command Link (GTCL)

GTCL is back-compatible with the previous GRETINA / DGS *Time and Trigger Control Link* (TTCL).

GTCL provides **clock, timestamp, trigger, and control** to the digitizer modules. A hierarchical distribution tree can be expanded to **hundreds of devices** with a hierarchical **fixed-latency** tree of fan-outs.

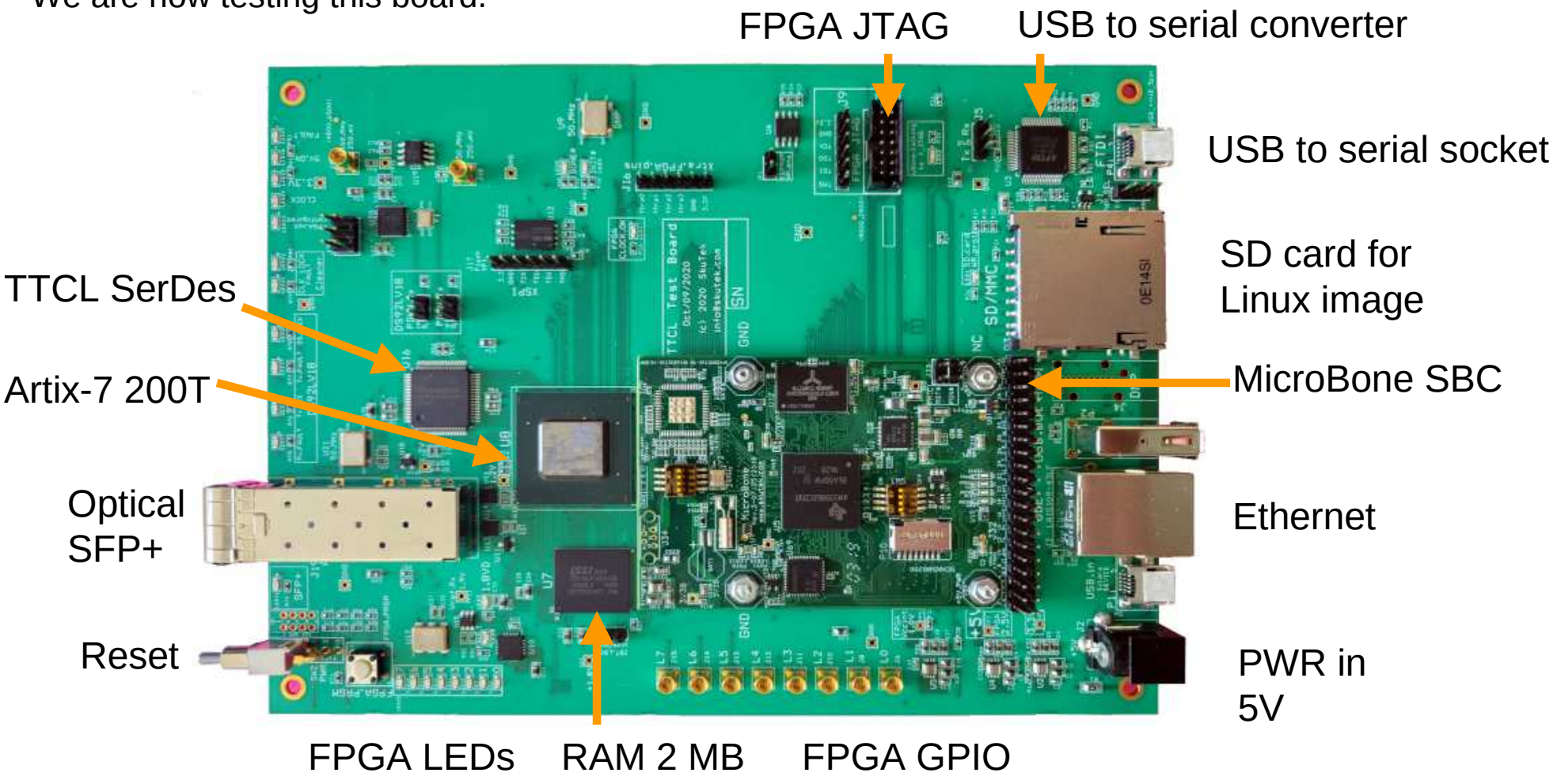
In addition to distributing the trigger, GTCL is also providing the functionality of the Precision Time Protocol (either PTP or White Rabbit), but in a **much simpler way**.

1. GTCL is distributing the **reference 50 MHz clock** to all the digitizers, to synchronize all the ADCs.
2. All the **timestamps** in the entire system can be reset, using a single GTCL command.
3. The **trigger condition** is distributed among all digitizers in all auxiliary detectors.
4. GTCL can also distribute other Run Control messages embedded in its frames (start, stop, etc.).
5. GTCL **does not require extensive programming**. All the GTCL specifics are implemented either in the SerDes hardware, or in the VHDL which is driving the SerDes data pins.
6. TTCL (the GTCL predecessor) **was proven sufficient** in dozens of experiments at ATLAS.
7. GTCL **does not rely on any third parties**, consortiums, or external bodies which could suddenly change the specs, impose new requirements, or render the entire protocol obsolete behind our back.
8. GTCL hardware implementation is both **simple** and **frugal** (as shown in the previous slide).

Progress With GTCL at SkuTek

GTCL is crucial for the project. We faced a tough question over the last year:

- What can we do, if GTCL is implemented at ANL, and we cannot travel because of COVID?
- We developed our own GTCL Test Board with the MicroBone Single Board Computer.
- It will let us implement a variety of tests, using the environment which we fully understand.
- We are now testing this board.

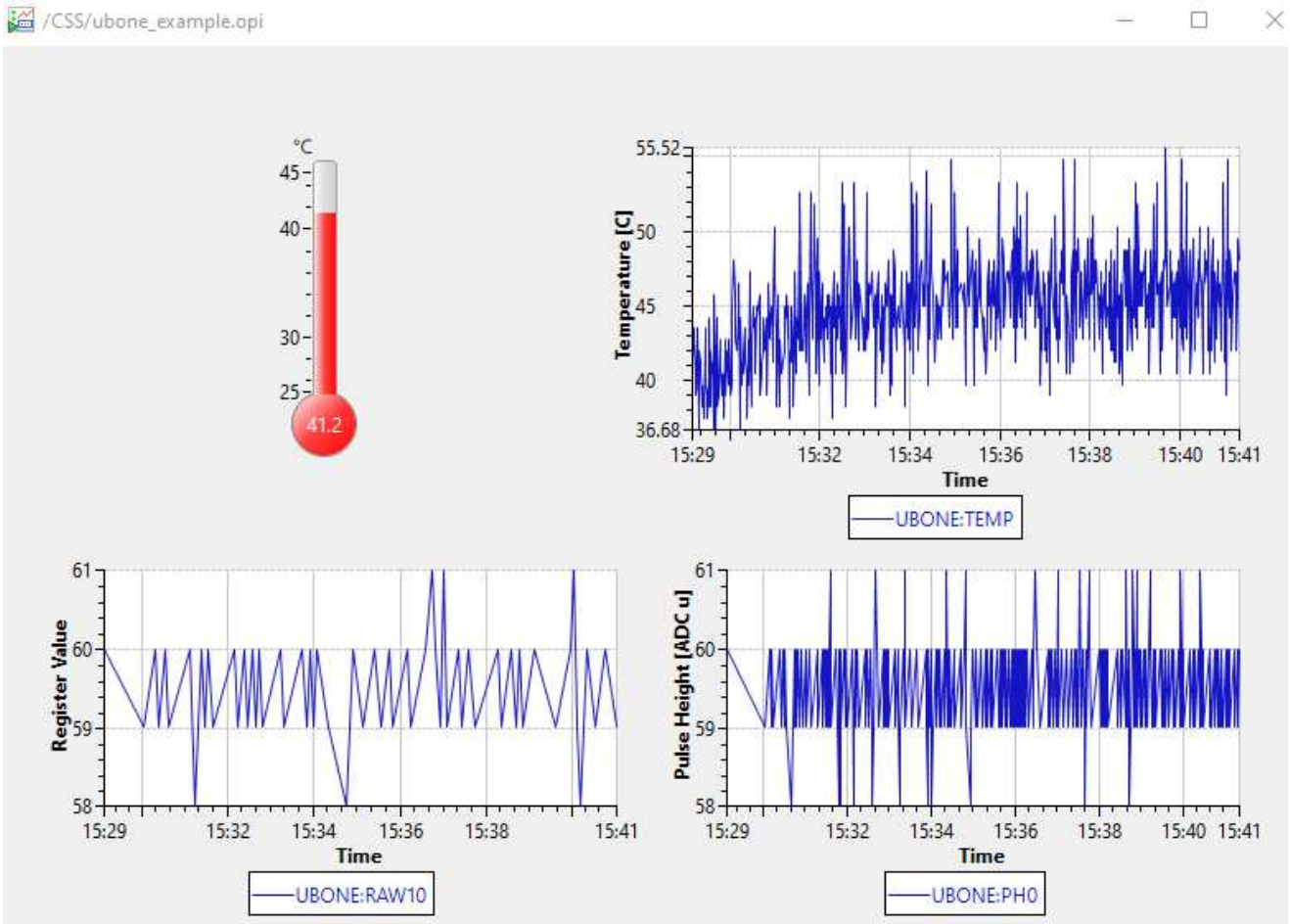


Progress With Control Software

Progress With Control Software at SkuTek

- *Experimental Physics and Industrial Control System* (EPICS) [1] is used at ATLAS to control the detectors.
- We implemented a simple EPICS application running on the MicroBone. It is showing how either we or the ANL personnel can integrate the MicroBone-based electronics into ATLAS control infrastructure.

[1] EPICS is documented at https://epics.anl.gov/



Temperature shown as thermometer
Temperature vs time
Pulse height via raw register access
Pulse height via explicit state variable

Summary

Summary of Technical Achievements

- **Phase I:** We tested our 40-channel prototype digitizer with HPGe Gammasphere detectors.
  - Pulse height resolution was equivalent to LBNL digitizers.
  - The success led to the Phase **II** collaboration with the ANL.
- The goals of **Phase II:**
  - *Integration* of the digitizers into the digital ATLAS DAQ, using the GRETA Timing and Command Link (GTCL), *back compatible with previous TTCL*.
  - *Fast readout* using 1G or 10G Ethernet links directly from the digitizers.
  - Setup and *monitoring* using the on-board *Linux*, separate from the fast readout.
  - *Achieve operation* of our prototypes in the ATLAS environment (after the pandemic).
- Achievements:
  - *Redesigned* the digitizer to provide 1G Ethernet in front, and P0 connector for the back.
  - *Developed* the Rear Transition Module with the GTCL and 10G optical links.
  - *Met* the GTCL design throughput @ 4 Gbps, using the optical SFP+ module.
  - *Redesigned* the Rear Transition Module to reach the 10G Ethernet data rate.
  - *Implemented* the GTCL Test Board allowing us to continue work despite travel restrictions.
  - *Implemented* an EPICS application paving the way towards full integration with ATLAS.

Future Plans

- Continue development of *firmware* and *software* for our digitizers.
- Develop *readout* over 1G and 10G Gigabit Ethernet.
- Develop *protocols and interfaces* compatible with the ATLAS environment.
  - We are now *working with the ANL* on firmware and software.
- Port the extant *ANL firmware* from the LBNL digitizers to our digitizers.
  - This portion of the project will be performed by ANL ATLAS personnel.
- Develop *software interfaces* for setup, control, and monitoring using the on board Linux.
  - *Low-latency* detector and signal *monitoring* with on-board Linux.
  - Continue development of EPICS interfaces.
- *Achieve operation* of our prototype digitizers in ATLAS environment (after the pandemic).

Acknowledgements

Joanna Klima, Gregory Kick, David Miller, James Vitkus
New hires: Jeffrey Maggio and Robert Cross

Dev Ashish Khaitan and Frank Wolfs helped in Phase I

John Anderson and Michael Carpenter (ANL ATLAS)

Consultant: Eryk Druszkiewicz

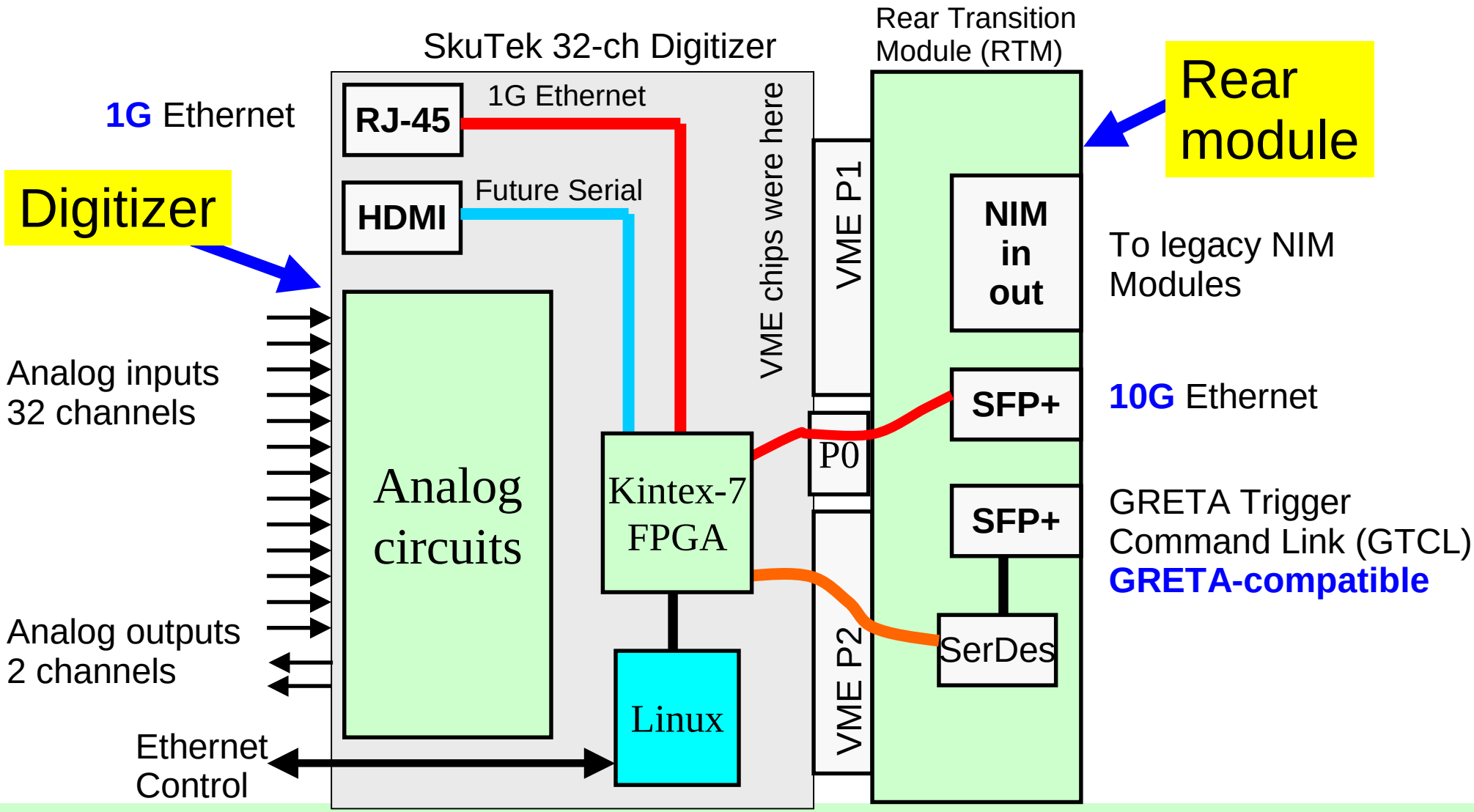
Interns:

Mandy Nevins, Jeffrey Sylor, Dinesh Anand Bashkaran,
Brian Kroetz, Vedant Karia.

Special thanks to Michelle Shinn and Manouchehr Farkhondeh

Conceptual Hardware Diagram

- VME interface was removed. Setup and control will be performed over Ethernet with Linux.
- **1G** readout implemented in the front (up to ~110 MB/s). **10G** in the back (10x faster).
- Heavy duty (and possibly noisy!) interfaces moved to the Rear Transition Module: 10G Ethernet and GRETA Trigger Command Link (GTCL).



Kintex-7 Provides More Resources Than Legacy Spartan-3

Kintex-7: **5x** more logic and memory

- **Spartan-3** was the best tradeoff between price and performance circa fifteen years ago.
- The new **Kintex-7** FPGAs now offers more digital resources at a reasonable cost.

Feature	LBNL digitizer XC3S5000 Spartan-3 a)	New SkuTek digitizer XC7K410T Kintex-7 b)	Improvement relative to XC3S5000
Equivalent logic cells from Data Sheet	74,880	406,720	5.4
Equivalent logic cells per channel	7.5 k	12.7 k	1.7
Multiply-accumulate units	104 c)	1540	14.8
Waveform memory (k samples) d)	104 k	1,590 k	15.3
Waveform memory per chan (k samples)	10.4 k (10 chan)	49.7 k (32 chan)	4.8
DigiKey price (900 balls) e)	$284	$1,933	6.8
$$ per channel f)	$28 (10 chan)	$60 (32 chan)	2.1

a) XC3S5000 is used in present GRETINA digitizers.

c) These Kintex-7 chips are used in our high density digitizers (both the 32 and 40 channels).

c) XC3S5000 provides multipliers without the built-in accumulate register.

d) Total number of block RAM bits divided by 18.

e) There are some variations of the price depending on the speed grades. We chose the most relevant speed variants, 5C and 2C, respectively. The details are explained in the respective Data Sheets.

f) Approximate FPGA cost per channel for 10 channels (Spartan-3) or 32 channels (Kintex-7).