Microelectronics for nuclear physics experiments

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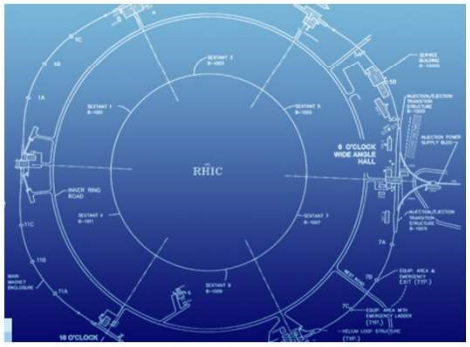
https://www.bnl.gov/instrumentation/

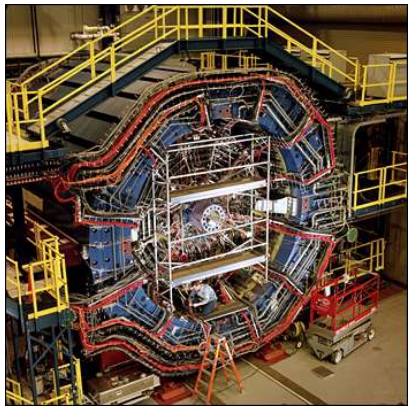
20210819

Nuclear Physics experimental facilities

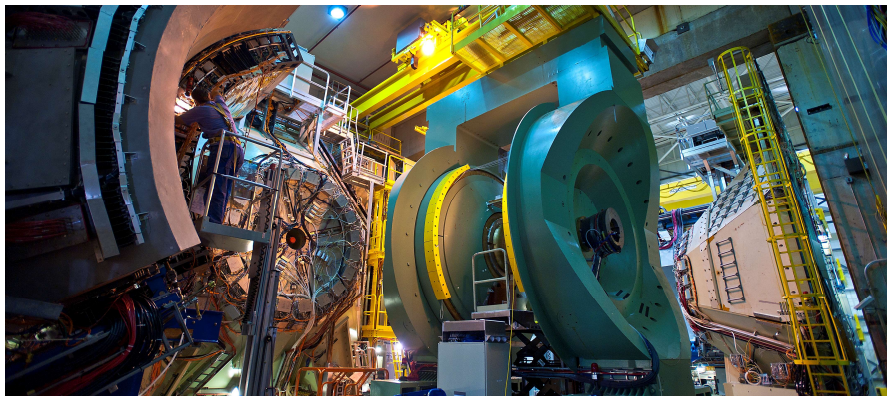
The Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory (BNL)

- **RHIC** is the first machine in the world capable of colliding beams of heavy ions (any atomic nuclei from protons—hydrogen nuclei—to uranium) traveling at relativistic speeds
  - the collision "melts" the protons and neutrons and liberates their constituent quarks and gluons…and thousands more particles form as the area cools off
- **Numbers**: 2.4-mile, 1,740 SC magnets, two-lane "racetrack", six intersections, operating since 2000





Right: STAR detector
Bottom: PHENIX detector



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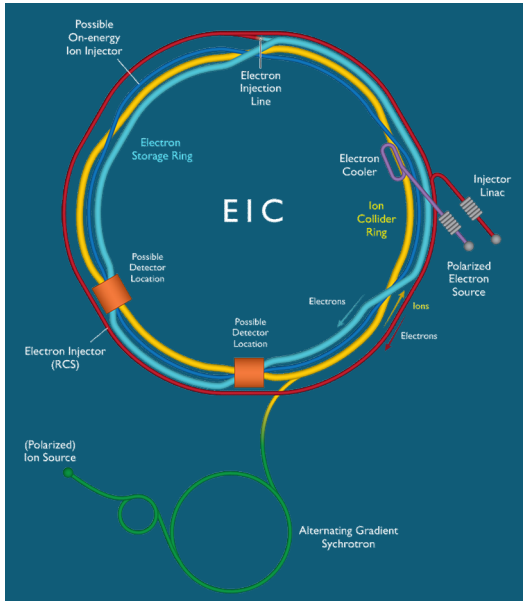
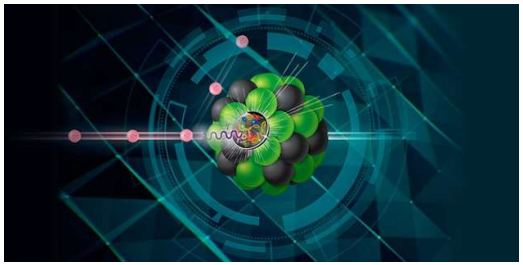
Nuclear Physics experimental facilities

The Electron Ion Collider (EIC) at Brookhaven National Laboratory (BNL)

- One ion accelerator/storage ring plus one electron accelerator ring and one electron storage ring
- One existing ion ring will carry ions (protons or other atomic nuclei) just like RHIC; a new electron storage ring will carry electrons after they have been accelerated by the new electron accelerator ring
- Probes the internal structure of nuclear matter as it exists today





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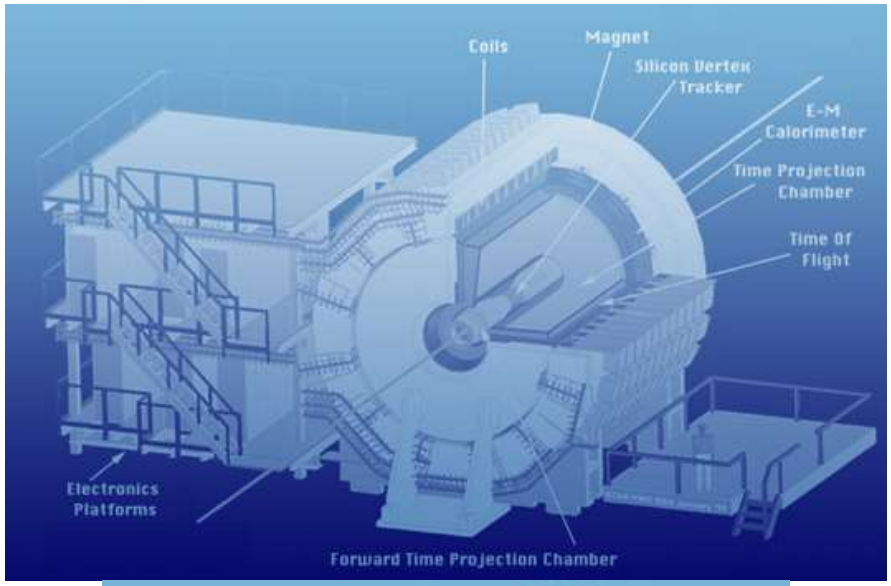
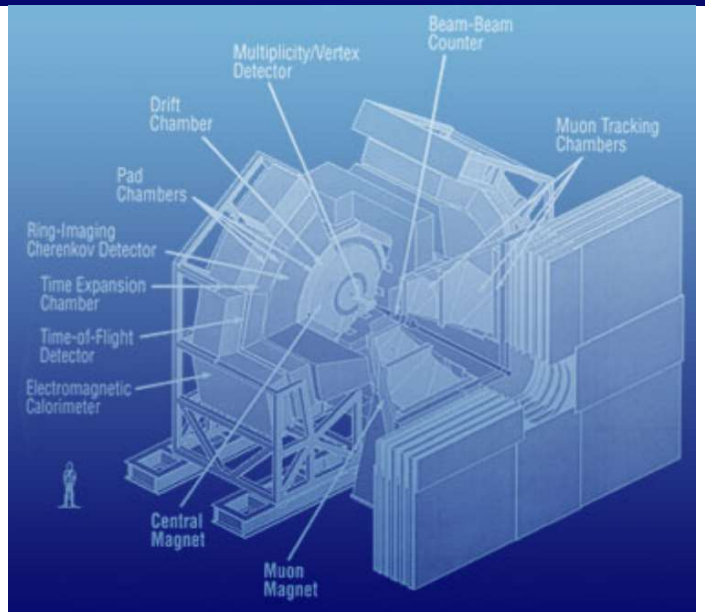
Detectors - RHIC

- STAR: Solenoidal Tracker at RHIC
- (s)PHENIX: Pioneering High Energy Nuclear Interaction eXperiment
  - "s" for its focus on the *strongly* interacting particles and PHENIX for the anticipated use of key detector components and location
- These detectors consist of several types of detectors
  - Each sub-system (detector) is specialized in detecting certain types of particles or characterizing their motion
- They work together in an advanced data acquisition and subsequent physics analysis
- Produce final statements that can be made about the collision





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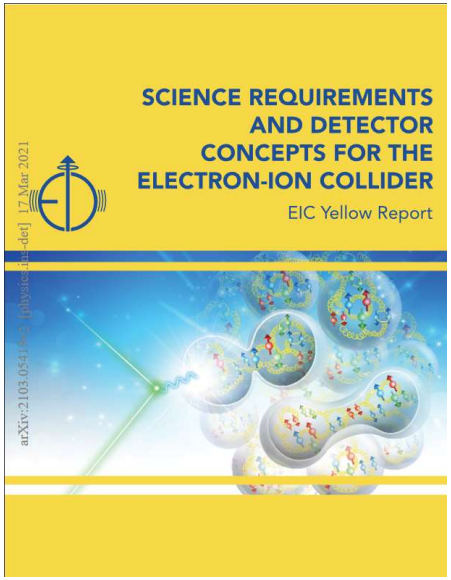
There is a lot of (micro)electronics at RHIC!

Detectors - EIC

- Tracking and Vertexing Detector Systems
  - The tracking and vertexing systems under consideration are based on semiconductor and gaseous tracking detector technologies, with concept detectors combining both technologies
- Particle Identification Detector Systems
  - Using the specific ionization (dE/dx) in time projection chambers with novel gas mixtures allows for improved resolution approaching the limit of Poisson statistics. However, dedicated particle identification detectors, based on Cerenkov light emission and time of flight measurements will be required
- Calorimeter Detector Systems
  - Among possible ECAL technologies discussed are homogeneous detectors and sampling calorimeters. Due to limited space available, short radiation length materials are favored. Silicon photomultipliers (SiPMs) are preferred



..the aim is to combine the best technology for each region in detector concepts that achieve the full set of requirements

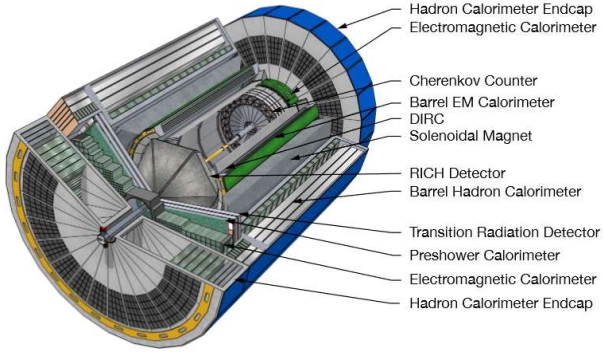


Figure 3.1: CAD model of a particular EIC detector concept, with the artistic rendering of the tracking, particle identification, and calorimetry subsystems.

EIC - Auxiliary Detector Systems

Far-forward region: silicon detectors in roman pots to detect very forward hadrons up to 5 mrad with high timing resolution of low gain avalanche diodes (***LGADs***)

Far-backward region: bremsstrahlung photons detected in an EM 0-deg calorimeter or a pair spectrometer to determine the luminosity

Other sections of the EIC: electron and hadron polarimeters to measure the polarization to a systematic precision better than 1%

Timely feedback to accelerator operators with a statistical precision of similar size will be achieved on short time scales

Electron beam: Compton polarimeter using a diode laser with high repetition frequency and a fiber amplifier to reach powers up to 20 W

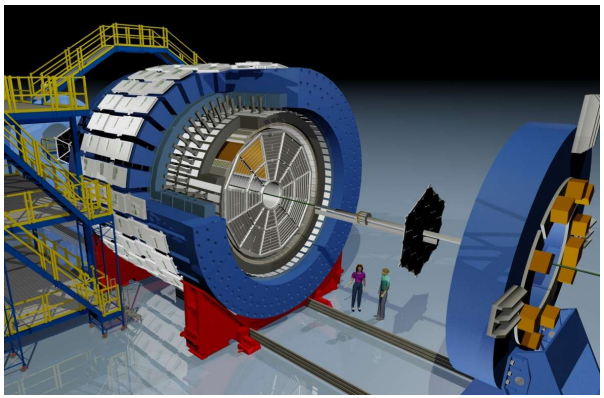
Longitudinal and transverse polarization can be measured with position sensitive detectors such as diamond strip or HV-MAPS detectors

Hadron beam: existing polarimeters at RHIC with additional hydrogen jet detectors and alternative ribbon targets

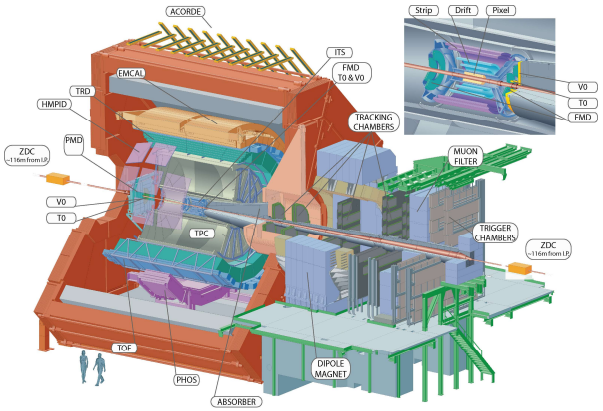
EIC will use a ***streaming readout approach*** without trigger electronics that controls whether or not to record events (similar to the LHCb-U)

New approaches in artificial intelligence are being explored (software)

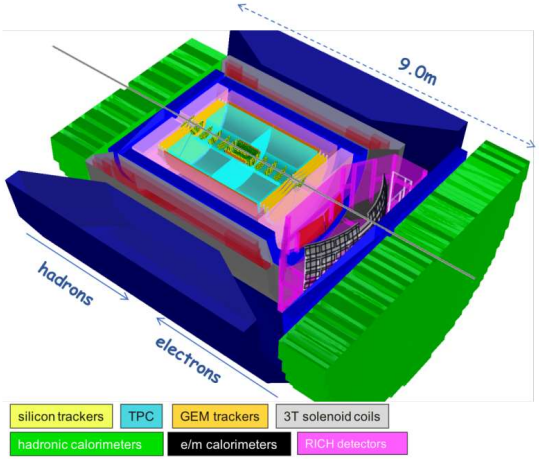
Monolithic Active Pixel Sensors (MAPS) in Heavy Ion Collider Experiments



STAR – MAPS Gen. 1



ALICE – MAPS Gen. 2
+ sPHENIX



EIC Detector – MAPS Gen. 3?

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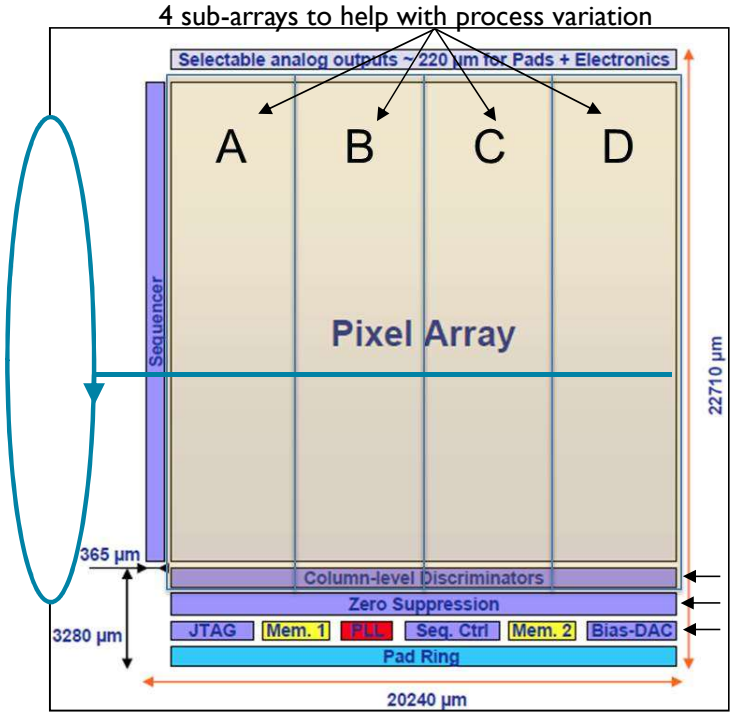
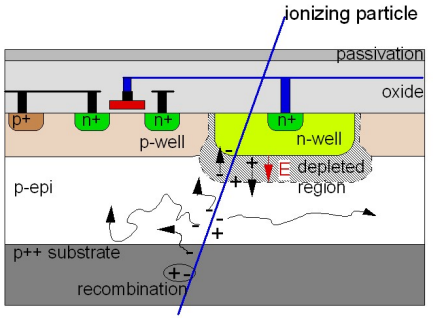
First MAPS in Physics

PXL MAPS sensor

- *Ultimate-2:* third revision sensor developed for PXL by the PICSEL group of IPHC, Strasbourg
- AMS OPTO 0.35 process - Binary readout of hit pixels

- High resistivity p-epi layer
  - Reduced charge collection time
  - Improved radiation hardness
- S/N ~ 30
- MIP Signal ~ 1000 e-
- **Rolling-shutter type readout**
  - A row is selected
  - For each column, a pixel is connected to discriminator
  - Discriminator detects possible hit
  - Move to next row
- 185.6 ms integration time
- ~170 mW/cm² power dissipation





- **Pixel matrix**
  - 20.7 µm x 20.7 µm pixels
  - 928 rows x 960 columns = ~1M pixel
  - In-pixel amplifier
  - In- pixel Correlated Double Sampling (CDS)

- **Digital section**
  - End-of-column discriminators
  - Integrated zero suppression (up to 9 hits/row)
  - Ping-pong memory for frame readout (~1500 W)
  - 2 LVDS data outputs @ 160 MHz

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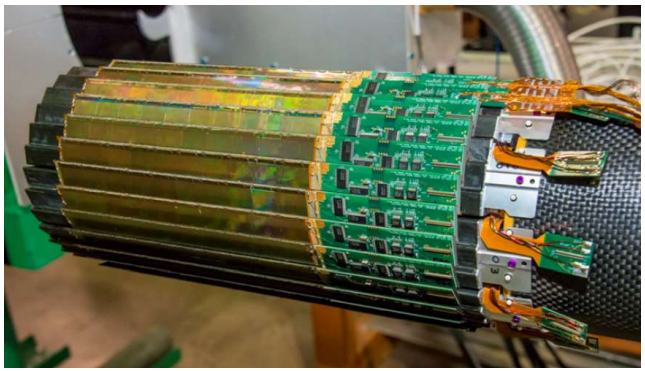
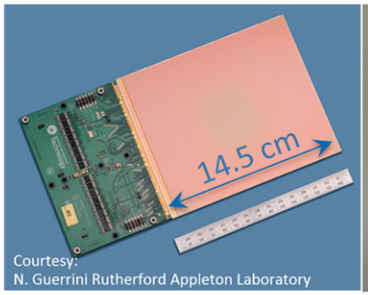
MAPS evolution

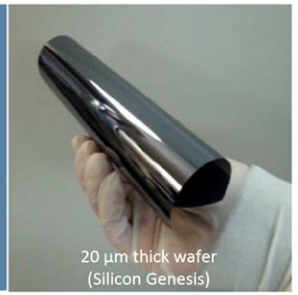


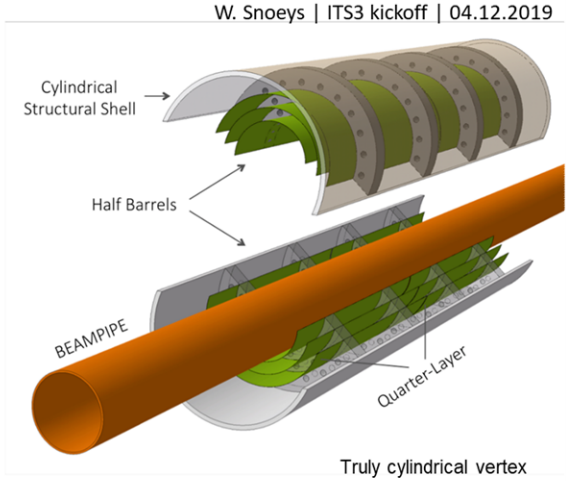
STAR – Heavy Flavor Tracker PXL detector

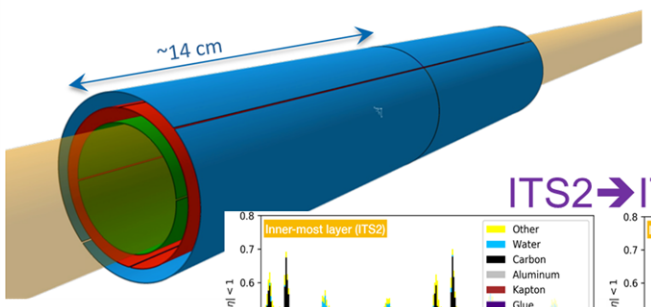
Endorsed by ALICE ITS Upgrade in LS3

Exploiting flexible nature of thin silicon and stitching

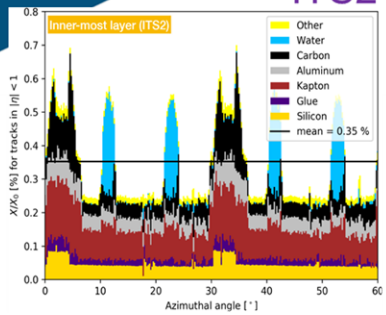


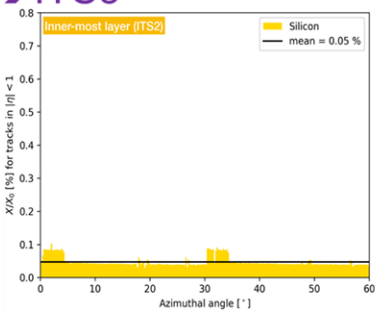






ITS2➔ITS3





Truly cylindrical vertex detector
New ultra light barrel in LS3 0.05% X/X0 per layer
ALICE-PUBLIC-2018-013

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Specification ITS to EIC

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager
ITS3 kickoff
04.12.2019

ITS2➔ITS3

- very wide tracking acceptance from -4<h<4
- vertex layers $X/X_0 \leq 0.3\%$
- disc layers $X/X_0 \leq 0.3\%$
- barrel layers $X/X_0 \leq 0.8\%$
- pixel size ≤ 20x20 um^2
- integration time ≤ 300 ns
- power dissip. ≤ 30mW/cm^2 (air cooling if possible)
- timing resolution ≤ 9 ns (EIC BX)
- Rad tolerance, hit density, etc. are < existing ALPIDE

EIC

	EIC DMAPS Sensor	
Detector	Vertex and Tracking	Added time stamping
Technology	TJ or similar	
Substrate Resistivity [kohm cm]	1	
Collection Electrode	Small	
Detector Capacitance [fF]	<5	
Chip size [cm x cm]	Full reticule	
Pixel size [µm x µm]	20 x 20	max 350 x 350
Integration Time [ns]	2000	
Timing Resolution [ns]	*OPTIONAL* *< 9 (eRHIC)* *< 1 (JLEIC)*	< 9 (eRHIC) < 1 (JLEIC)
Particle Rate [kHz/mm^2]	**TBD**	
Readout Architecture	Asynchronous	**TBD**
Power [mW/cm^2]	<35	<200
NIEL [1MeV neq/cm^2]	10^{10}	
TID [Mrad]	< 10	
Noise [electrons]	< 50	
Fake Hit Rate [hits/s]	< 10^{-5}/evt/pix	
Interface Requirements	**TBD**	

Laura Gonella
EIC Detector R&D Meeting
30.01.2020

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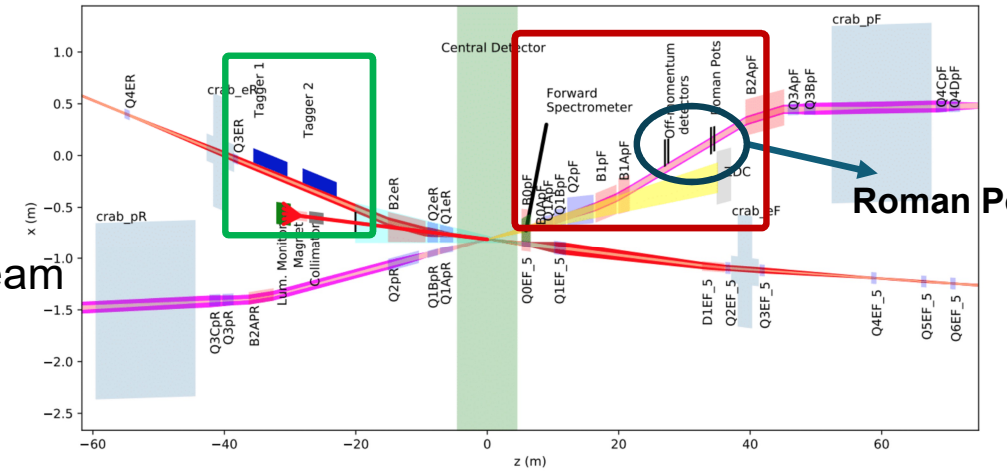
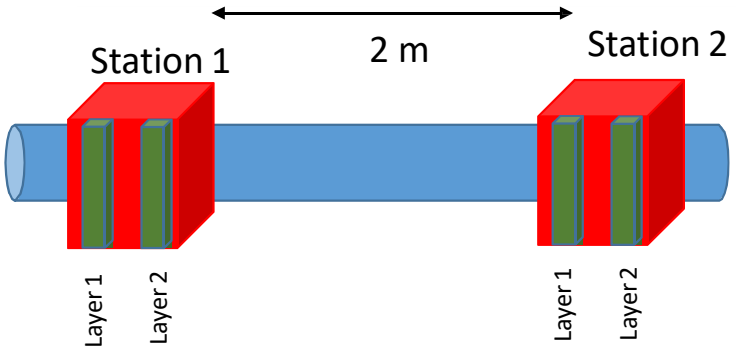
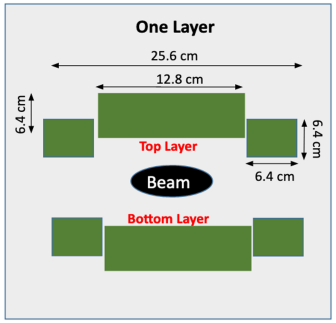
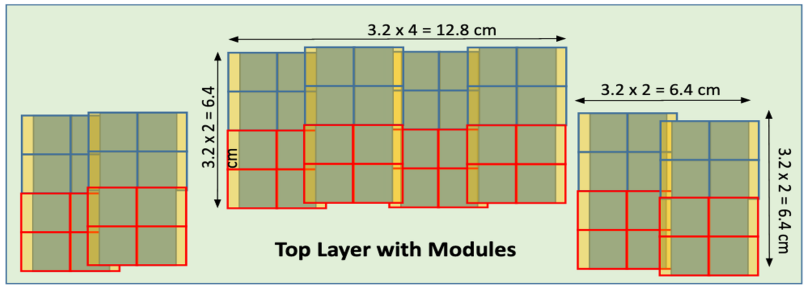
EIC – Roman Pots

- **Physics Goals of Roman Pots**
  - Tag protons and light nuclei close to the beam from coherent processes, protons from nuclear breakup, etc.
    - Crucial for exclusive and diffractive physics
- **Essential requirements from simulations**
  - Large active area (~25cm x 10cm)
  - Time resolution 30-50ps
  - 500μm x 500μm pixels
  - Edgeless (inactive edges ~< 150μm)
- **AC-LGAD technology of choice to meet these requirements**









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Low-Gain Avalanche Detectors

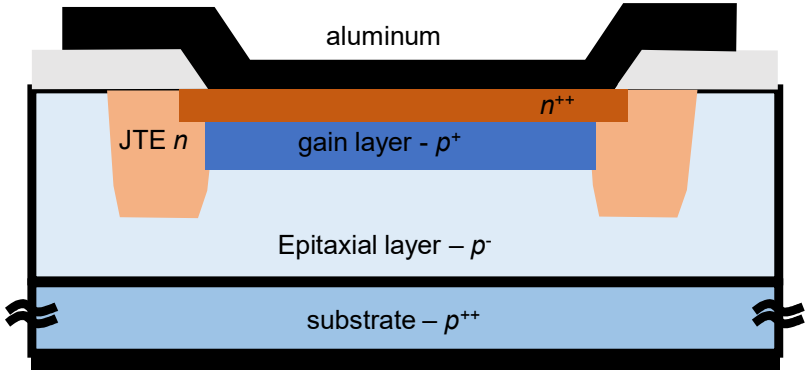
Why Low-Gain?

- Avalanche Photo Diode have gain up to ~ 200 (typically), as they need to detect visible/UV photons, each creating just 1 e^-/h pair in silicon

- mip create > 80 e^-/h pair per micron of silicon traversed and the thickness is a few tens of microns: a gain of 20 is enough to attain a signal that can be read-out by fast (noisy) electronics

Different types of LGADs

LGAD structure



Depletion of the p+ gain layer creates intense electric field, high enough for electron impact ionization to occur

Hole impact ionization ~ 0
→ no breakdown
→ gain ~ few 10s

If the substrate is thin (~ 50 μm) → signal is fast (~30 ps)

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Timing and space with AC-LGADs

LGADs do not allow fine segmentation

Another concept is required – confirmed in lab tests

Novel development: AC-coupling allows fine segmentation

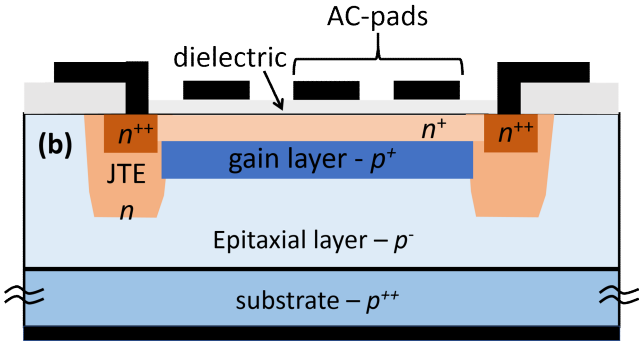
➔ Time & Space measurements

s_x << Pitch/sqrt(12)

s_t as in LGAD, ~ 30ps

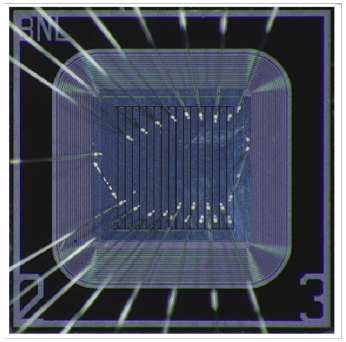
100% fill factor

AC-LGAD structure

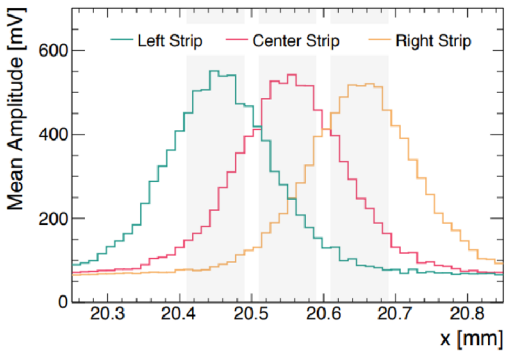


AC-LGAD 2mmx2mm strip sensor

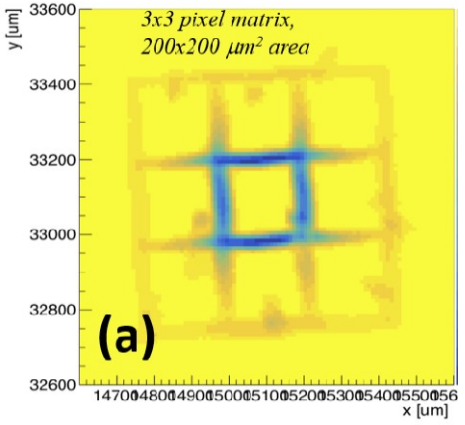
- Strip pitch = 100μm
- Wire bonded to a multichannel TA board (FNAL)



Beam Test at FNAL



TCT at BNL



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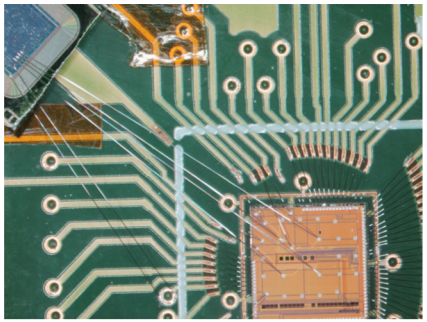
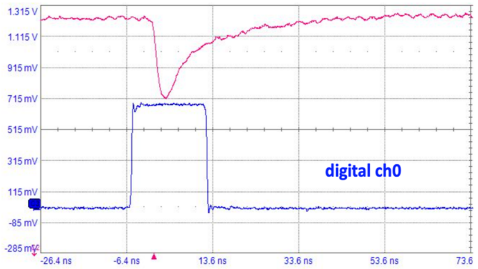
"Measurements of an AC-LGAD strip sensor with a 120 GeV proton beam," arXiv:2006.01999

AC-LGAD readout ASIC development

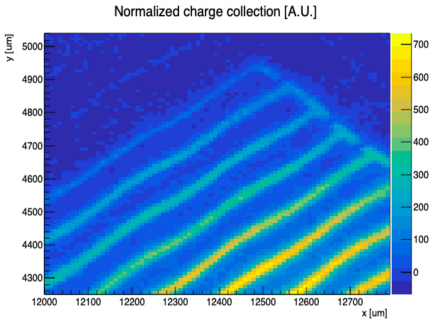
- Strategy to modify ASIC (ALTIROC, CMS TSMC 130 nm) used in ATLAS timing detector (HGTD) and make it compatible to Roman Pot specs
  - Main modifications have been identified to reduce pixel pitch from 1.3 mm to 500 μm
  - First tests of AC-LGAD compatibility with ALTIROC show that the chip can read the signals from the AC-LGAD



- Assembly: ALTIROC0 v1 prototype (4 ch) + strip AC-LGAD (100 μm-pitch)
- ALTIROC0 chip: analog readout after the preamplifier, 2 TDCs (TOA and TOT) and threshold discriminator. Time jitter smaller than 20 ps for input charge larger than 5 fC



- Signal from beta-particles from 90Sr source
- **Clear signal with negative and positive polarity**
- Fast (~5 ns) signal compatible with published results for (DC) LGAD sensors read-out via ALTIROC0 [JINST 15 P07007 (2020)]



- Laser Scan - Colors: integral charge of the signal peak from the ALTIROC analog output generated by IR laser on sensor
- Results compatible with those with beta-particles ('waves' due to board vibrations - to be fixed)

Accelerators create harsh environments

Background/radiation

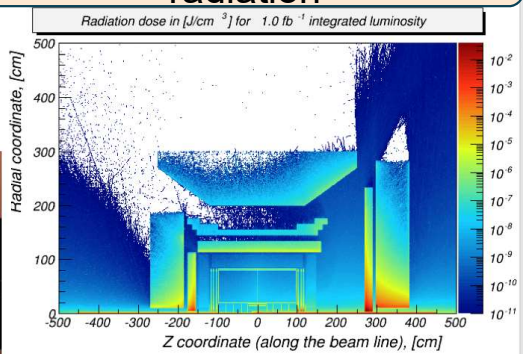
- Having backgrounds under control is crucial for the EIC detector performance (HERA and KEK experience)

- There are several background sources:

- primary collisions - beam-gas induced - synchrotron radiation

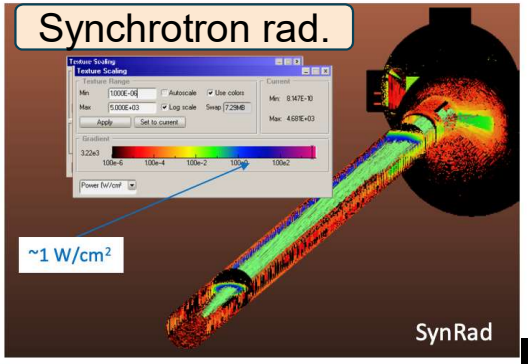
- The design of absorbers and masks must be modeled thoroughly

Primary collisions/ionizing radiation

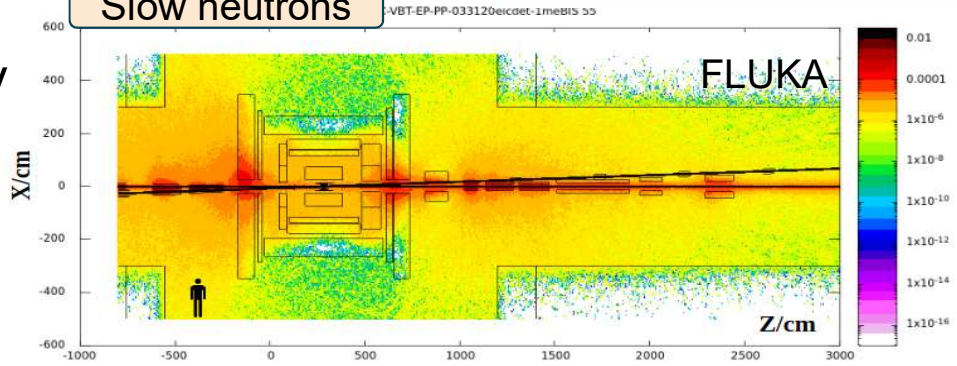


-> backward EmCal: ~250 rad/year
(at a "nominal" luminosity
~10^{33} cm^{-2} s^{-1})

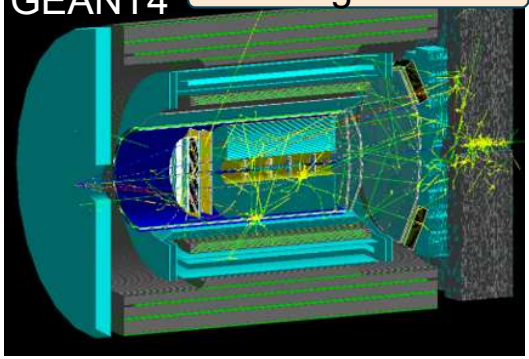
Synchrotron rad.



Slow neutrons



Beam-gas event



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Radiation effects in microelectronics

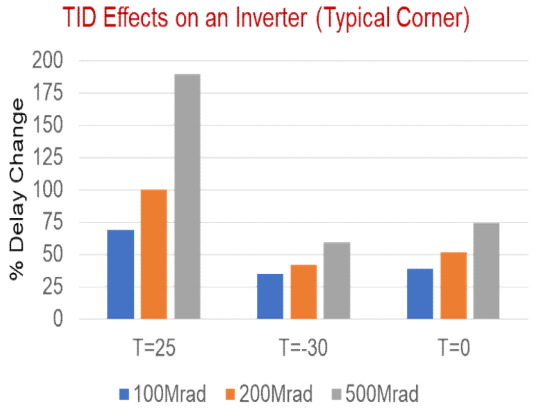
The most common radiation effects of concern are:

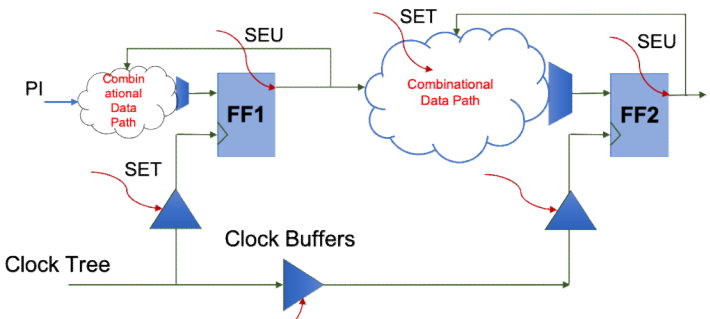
Total Ionizing Dose (TID) – charged particles and photons

- Introduces defects in the SiO2 present at the MOS gate and at the shallow trenches used for the device isolation (STI)
- Threshold voltage (for both PMOS and NMOS) and leakage current changes with the accumulation of these defects over the circuit lifetime

Displacement Damage – neutral and charged particles

- Produces physical damage and introduces defects in the lattice (bulk) and SiO2



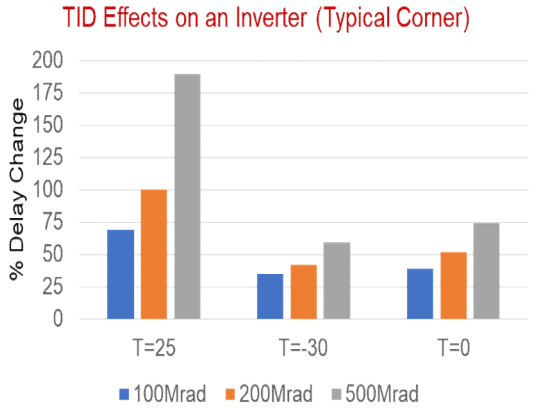


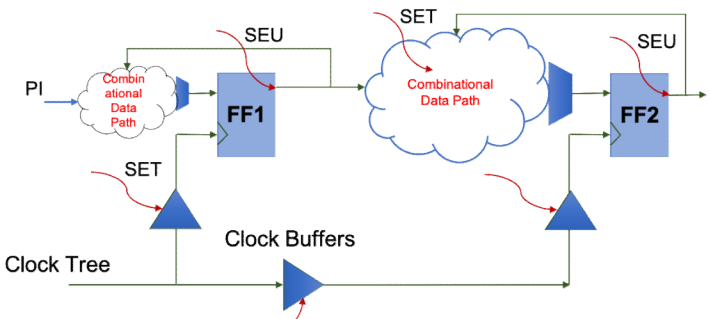
Generic digital design showing Flip-Flop (FF) memory elements and their connectivity through a combinational data path. Also shown the potential possibility of SEU and SETs

Radiation effects in microelectronics

Single Event Effects (SEEs) – deeply penetrating particles

- Produces a series of effects: latchup or device death, excess carriers in device, signal corrupted, data upset
- The most concerning ones are the Single Event Upsets (SEUs) and Single Event Transients (SETs)
  - SEUs arise in memory elements and flip the data stored in the memory elements (Flip-Flops, Latches, SRAM Memories)
  - SETs arise in combinatorial gates in data path and introduce unintentional glitches which may propagate leading to capturing of wrong data in the memory elements





Generic digital design showing Flip-Flop (FF) memory elements and their connectivity through a combinational data path. Also shown the potential possibility of SEU and SETs

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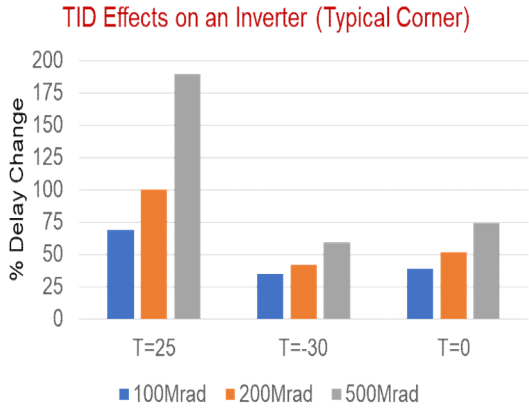
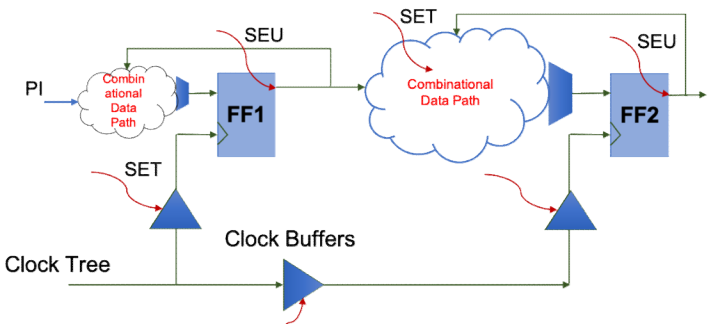
Radiation effects in microelectronics

- Analog designs have the flexibility to choose the device length and width in a way that they are less susceptible to the radiation effects
- Digital logic designs are based on custom or pre-built digital standard cell libraries
  - They use short channels and narrow width device their performance and functionality are largely degraded due to TID or SEE effects respectively
  - Techniques such as Triple Modular Redundancy (TMR) are often employed to counter SEE effects however more understanding





Generic digital design showing Flip-Flop (FF) memory elements and their connectivity through a combinational data path. Also shown the potential possibility of SEU and SETs

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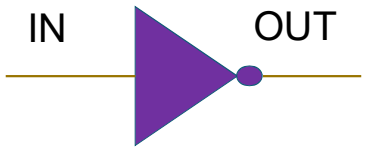
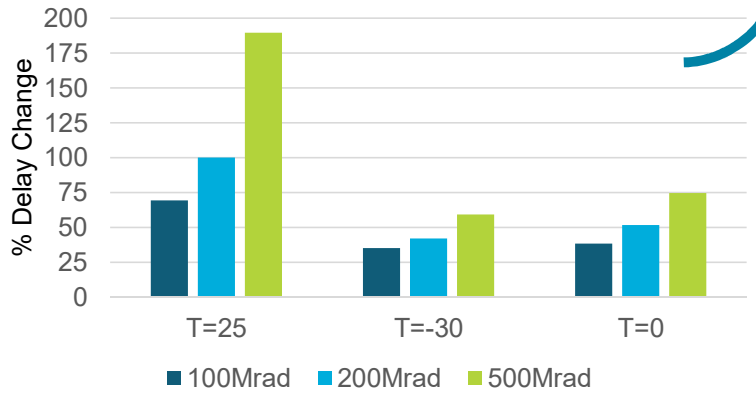
How to mitigate these effects?

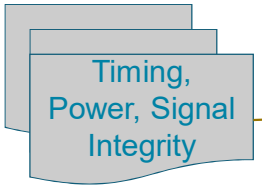
- **TID** alters the performance of CMOS device - degrades logic gate performance
- HEP detector for phase-II Upgrades - expected to tolerate 100 Mrad to 500 Mrad



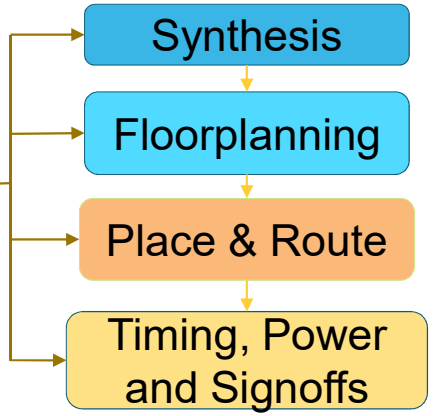
TID Effects on an Inverter (Typical Corner)



Liberty Timing Models



Radiation corner timing libraries in digital design flow



Digital libraries characterized with TID models

TSMC 65nm TID Models

acaratel Alessandro Caratelli MICSFT-Users 2 Oct '19

The timing libraries are characterized for 9-track standard cell library using radiation corner device models, released by the CERN foundry services.

This work has been carried out and made available for the community by:

Sandeep Miryala - ASIC Design Engineer - Fermilab, Batavia, USA - smiryala@fnal.gov
Grzegorz Deptuch - ASIC Group Leader - Fermilab, Batavia, USA - deptuch@fnal.gov

Please kindly consider acknowledging in your future publications for works using these blocks the names of the designers of this libraries and the CERN ASIC support service.
It helps the recognition of the work of fellow designers and motivates other designers to contribute with new material for the community.

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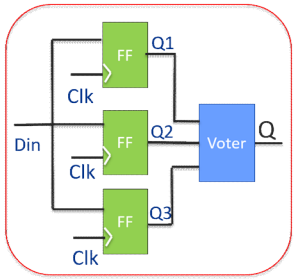
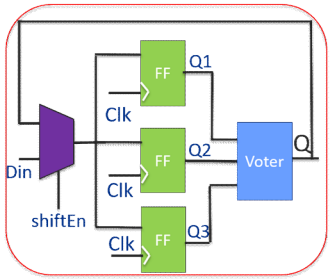
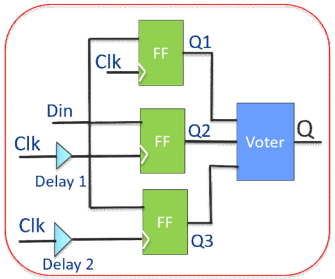
SEE tolerant ASICs

- **SEE mitigation technique in a digital logic**
  - Triple Modular Redundancy (TMR)
  - From regular synthesis flow to automated TMR insertion
- **SEU protection areas in an ASIC**
  - Global configuration and state machines
  - Pixel configuration bits
  - Data path memory elements
- **SEE tolerant digital design flow**
  - Using commercial design tools and flow
  - Spatial separation of flops in a layout







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Neutrinoless double beta ($0\nu\beta\beta$) decay experiments

0νββ is a hypothetical (and rare) decay process that would allow further (new) understanding of particle physics (and the universe)

- This process can occur only if specific circumstances are proven
- Recent studies have shown various properties of neutrinos
  - Suggest neutrinos have a nonzero mass

- Several experiments implementing different approaches and technologies
- Focus on increasing detection sensitivity – some common strategies:
  - Increase the chance of detecting rare events by increasing the exposure
  - Improve energy resolution and minimize background events
  - Shields (active and passive) & purification and radio assays

$0\nu\beta\beta$ decay: detector approaches

- Loaded liquid scintillators (LSs): KamLAND-Zen, SNO+
- High-purity Ge (HPGe) – (76Ge): GERDA and Majorana → LEGEND(-200)
- Time projection chambers (liquid): EXO-200, nEXO
- Time projection chambers (gas): NEXT, PANDA-X-III
- Low-temperature (mK) thermal calorimeters: CUORE, CUPID, AMoRE
  - e.g., NTD Ge sensors, transition edge sensors (TESs) and metallic magnetic calorimeters (MMCs)
- **(Micro)electronics challenges**
  - **operation at cryogenic temperature and radiopurity**

Cryogenic electronics

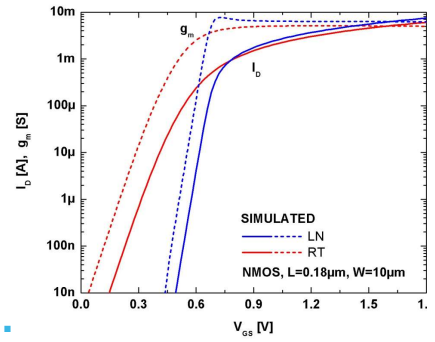
Several (many) technologies from JFET to CMOS, SiGe…

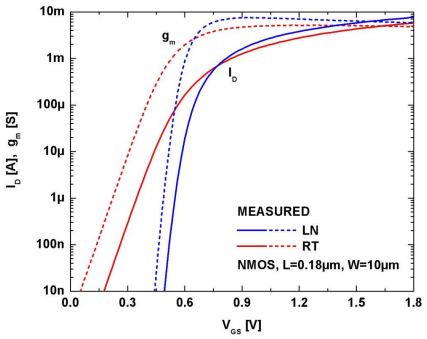
The good: low temperature provides reduced leakage, improved carrier mobility, increased conductivity

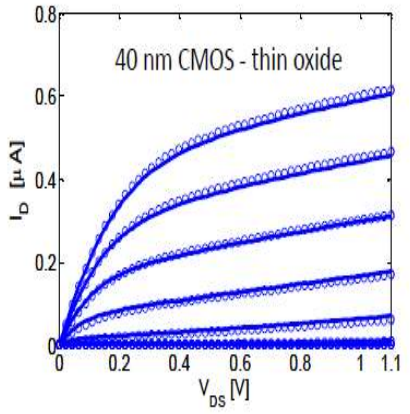
- Results in better performance: **much higher g_m/I_D … and lower noise (mostly)**

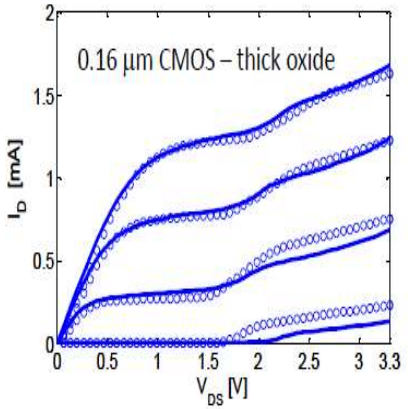
The bad: no models, test structures/specific measurements for extraction, it depends on specific technology

The ugly: it has to work at room and cryogenic temperature - big change of transistor (all devices!) parameters









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Cryogenic electronics: challenges

Models (active components), reliability and lifetime

Typically **models** of commercial foundries are valid *for temperatures **from -40°C to 125°C**, and cover frequencies **up to the lower of 30-GHz** or cut off frequency of active devices, or the resonant frequencies of the passive components*.

Must be done:

- Measuring transistor characteristics and extracting Spice-type model parameters
- Static measurements (ID(VGS), ID(VDS)) are easy but require test structures with transistor flavors (LVT, NVT, HVT, 2.5V, etc.) and representative W/Ls
- Standard cells need to be redesigned (increased L) and timing libraries rebuilt using parameters of transistor models newly extracted for CT
- Mismatch and process variations should be extracted or CT for corner, MC simulations and timing margins – e.g. Vth (threshold voltage goes up at cryo) variation's lead to mismatch

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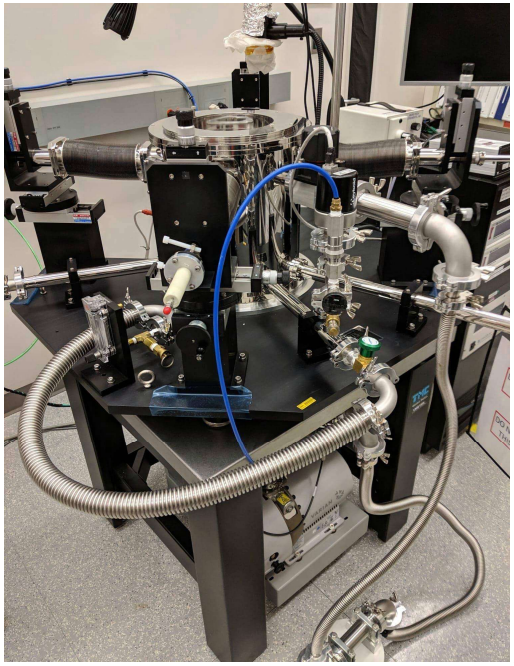
Measurements require cryo-probe-station static and RF

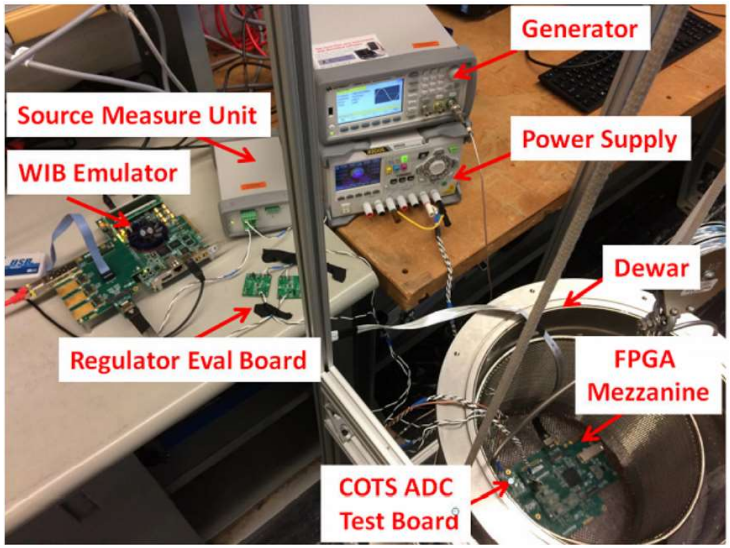


Cryo-probe station at the CFN

Cryogenic electronics: challenges

Models (active components), reliability and lifetime

- Degradation due to impact ionization causes interface state generation and oxide trapped charge → may affect the lifetime (not a sudden failure)
- Usually foundries guarantee a lifetime of about 10 years at room temperature under the worst operating conditions for aging with transconductance used to define lifetime (e.g. 10% reduction)
- At cryogenic temperature the impact ionization increases → lifetime reduces
- **Accelerated lifetime test** by placing transistor under severe electric field stress



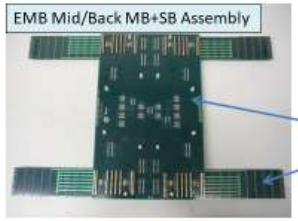
Picture of lifetime study evaluation test setup with both Commercial-Off-The-Shelf (COTS) ADC test board and FPGA mezzanine submerged in LN2 dewar

Device under test: ADI AD7274 fabricated in TSMC 350nm CMOS technology [25]

Reliability of ‘cold’ electronics – history

Electronics components operate immersed in liquid noble elements (Ar, Kr, Xe)
They have to function ‘*continuously and unattended*’ for long time (>10s years)

Reliability of Cold Electronics *wrt* *thermal contraction-expansion*
PCB and Cold Electronics in **ATLAS:**

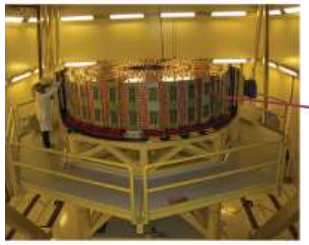


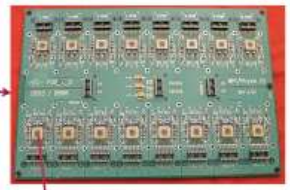
- ATLAS LAr Calorimeter
  - 182,468 readout channels
- EM Barrel Mother Board and Summing Board
  - EMB has ~110,000 detector channels read out by 896x128-ch FEBs
  - 960 Mother Boards (MB)
  - 7,168 Summing Boards (SB)
  - 20,480 resistor network chips, 0.1%
  - ~110,000 protection diodes on MBs/SBs
- EM Barrel Calorimeter has been cold since 2004
  - Operation: 7 years so far
  - MB/SB will remain in operation without upgrade for super LHC

- ‘Inoperative’ channels <0.5%, as of 05/10/2011
- Dead channels in the cryostat ~0.02% since 2008

…as of ten years ago

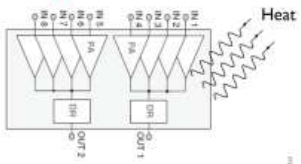
HEC Cold Electronics





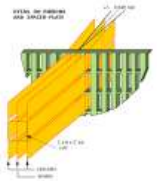
- GaAs TriQuint QED-A $1\mu m$
- Stable operation at cryogenic temperatures

35840 preamps , 8960 summing amp,
5632 read-out channels
2005 first commission in cold: 5 dead channels
(< 0.1 %). None due to preamps.
Two due to sum amp (already at warm).
In 2011 still 5 dead channels:
stable after 6 six years of operation.
High reliability of this cold electronics



Good track record!

Liquid Krypton calorimeter with JFETs in **NA48-NA62**



- JFET preamplifiers in LKr: 13,212 channels; surface mounted components
- Operated at very high voltage
  - Tested up to 7kV, operated in 3kV
- Failures
  - ~50 because of an HV accident in 1998
  - ~25 cold electronics failures after 1998,
    < 0.2% in 13 years
  - The last failure recorded was more than 10 years ago
- Always kept at LKr temperature since 1998
- Operation
  - **23 years** so far

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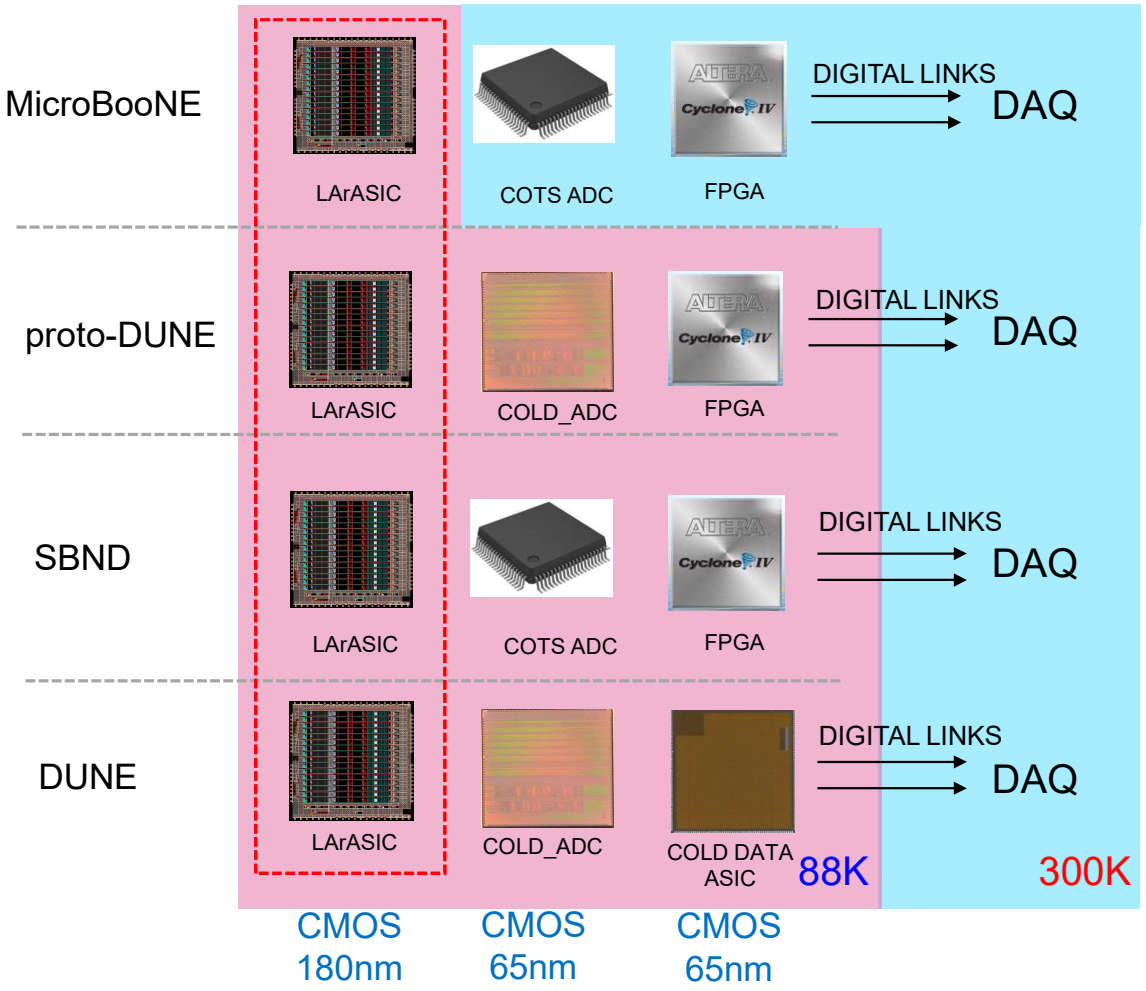
Evolution LAr (~80K) electronics chain

About a decade of development



DUNE cold electronics

Waveforms are digitized at 2MHz and read out without zero suppression

Electronics mounted near the sense wires, in the Liquid Argon

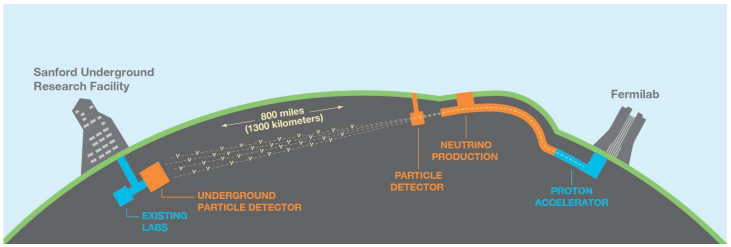
- Amplifier and Shaper, ADC, Data merger and Serializer

3-ASIC readout for DUNE far detector: LArASIC (180nm), ColdADC & ColdDATA (65nm)

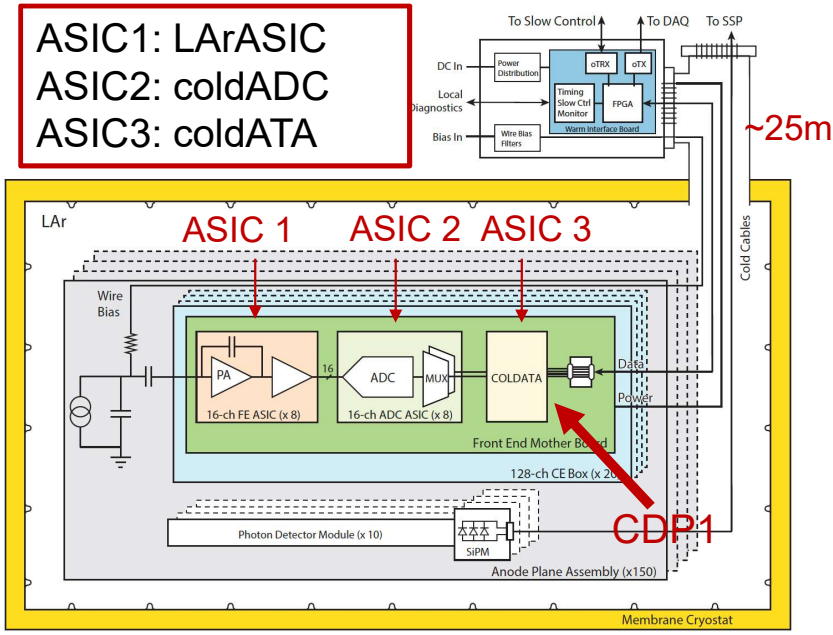
- Front-End: LArASIC (BNL)
- Time interleaved ADC: ColdADC (LBNL, FNAL, BNL)
- Data concentrator/transceiver: ColdDATA (FNAL, BNL digital implementation and P&R)

One 10 kTon detector has

- 3000 128-channel Front End
- 24000 FE ASICs, 24000 ADC ASICs,
- 6000 ColdDATA ASICs
- 12000 1.28 Gbps links (9.2 Tbps of waveform data)



ASIC1: LArASIC
ASIC2: coldADC
ASIC3: coldATA



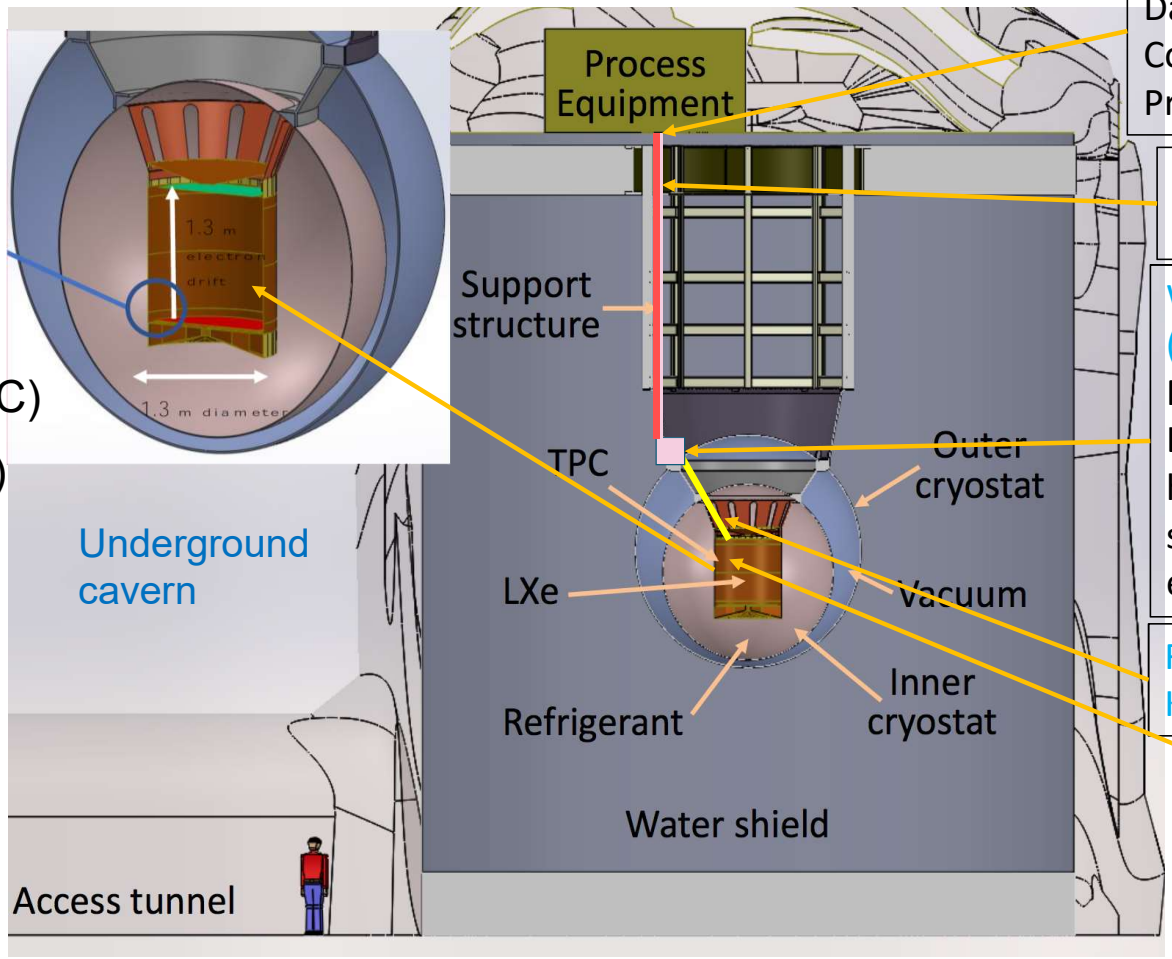
nEXO electronics

LXe TPC

Two main readout developments:

Charge readout (SLAC)

Photon readout (BNL)



Backend Readout (FELIX): Data reception, Slow Controls, Trigger Processing, Clock dist, etc

Regular Optical Fibers, Copper for Power

Warm Transition Cards (LVDS to Fiber): Multiplex LVDS to fiber, LV+Bias handling/distribution, slow controls processing, etc.

Radiopure High Speed Kapton Cables

Stave/SiPM Tiles

SiPM ASIC

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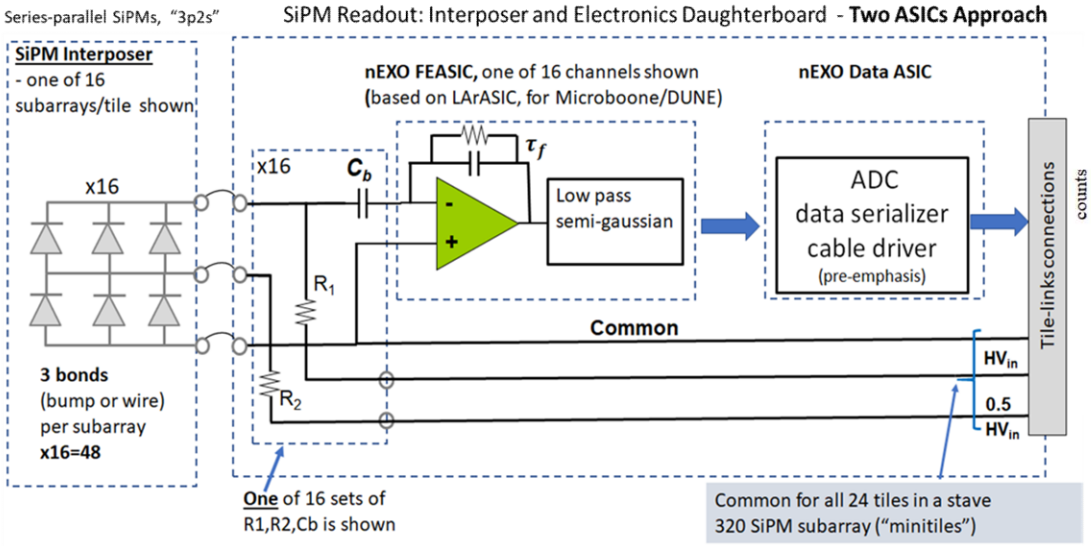
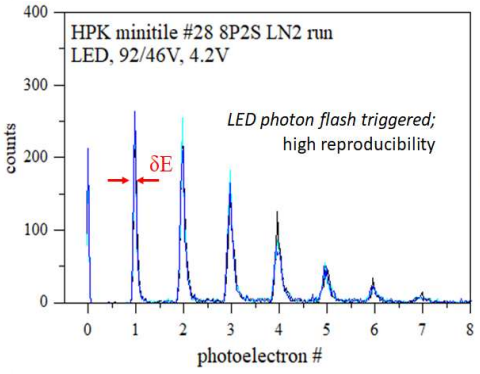
nEXO photon readout

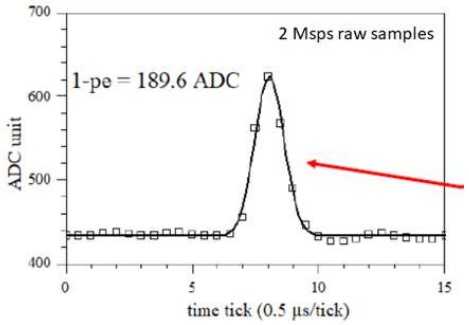


Demonstration of 6 cm^2 SiPM(HPK) subarrays with LArASIC in LN_2



Photon rate: ~80 Hz (trigger rate 100 Hz)

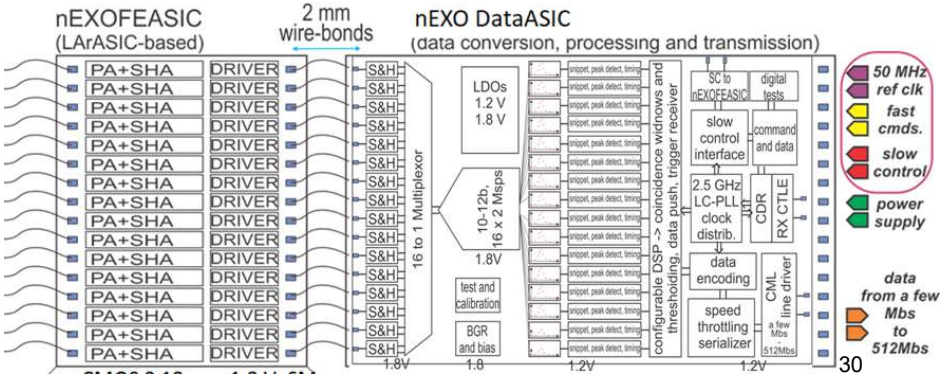
1-pe resolution (δE): 3 to 3.5% rms



Single photoelectron waveform "snippet" of samples :

***- S/N* ~60 - *coincidence resolution* between two subarrays < 19 ns**

- Optimal S/N based on AC coupled solution for large capacitance SiPM (Demonstrated)
- Two ASIC solution
  - Low noise analog front-end based on LArASIC used in many experiments (16 channels, with adj. Gain and Peaking time and low power operation)
  - Digital backend ASIC with DSP capability for Snippet waveform sampling (reduced data rates and volume)
- Concept demonstration using LArASIC and FPGA show SPE resolution and timing in line with nEXO requirements



Photon readout in nEXO - radiopurity

Specific Activity	U-238 ($mBq\,kg^{-1}$)	Th-232 ($mBq\,kg^{-1}$)
Gold Bonding Wire	1.74×10^{2}	1.91×10^{2}
Aurubis Copper	3.16×10^{-3}	5.17×10^{-4}
Alpha Vaculoy Solder	1.9×10^{-1}	-9×10^{-2}
Heraeus Spectrosil Fused Silica	6.97×10^{-3}	-6.11×10^{-4}

U-238 Hit Efficiency	Th-232 Hit Efficiency
3.8×10^{-6}	1.69×10^{-6}

Table I. Top level information about radiopurity calculations

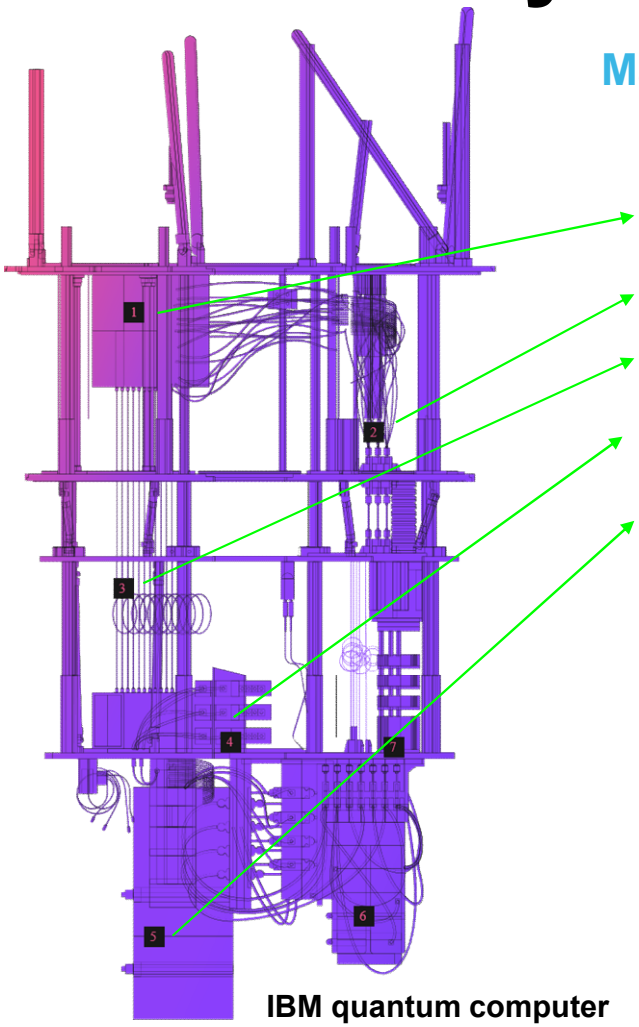
	Unit Mass (g)	Number per Module	Mass for Detector (g)	Background rate (cts /yr/inner 2 tons)	Background Fraction
45 µm diameter gold ball bump	9.23×10^{-7}	1152	0.255	1.24×10^{-2}	0.9452%
2 mm long, 45 µm diameter gold wire bond	6.1517×10^{-5}	192	2.835	1.38×10^{-1}	10.5%
300 µm diameter Alpha Solder Ball	1.04×10^{-4}	1152	28.8067	4.86×10^{-3}	0.3712%
300 µm Epoxy balls	?	1152	?	?	?

Table II. Radiopurity comparison between SiPM mounting options. SiPMs with TSVs would only require the gold bumps or solder ball. SiPMs without would require one of those plus the gold bonds

	Unit Mass (g)	Number per Module	Mass for Detector (g)	Background rate (cts /yr/inner 2 tons)	Background Fraction
45 µm diameter gold ball bump	9.23×10^{-7}	8	1.77×10^{3}	8.6×10^{-5}	0.0066%
2 mm long, 45 µm diameter gold wire bond	6.1517×10^{-5}	128	1.890	9.17×10^{-2}	7.0013%
300 µm diameter Alpha Solder Ball	1.04×10^{-4}	8	0.200	3.38×10^{-5}	0.0026%
300 µm Epoxy balls	?	8	?	?	?

Table III. Radiopurity comparison between ASIC mounting options. All options require either gold, solder balls, or epoxy to hold the ASIC down and wire bonds to connect all pins to the daughterboard.

‘Colder’ cryo-electronics

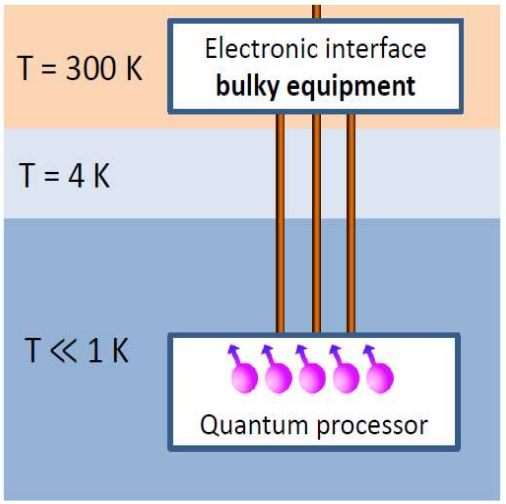


IBM quantum computer

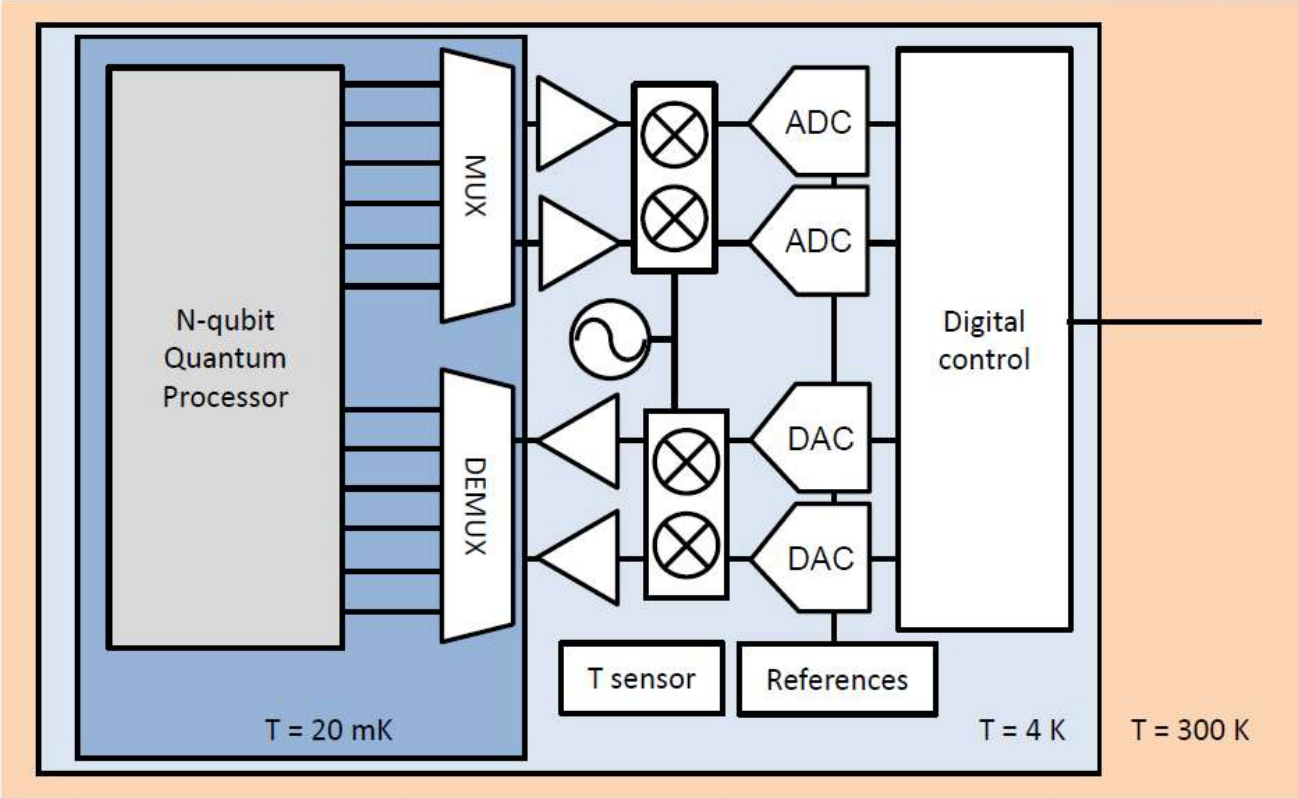
Main driver: quantum computing, opportunity for other applications

1. Qubit Signal Amplifier
2. Input microwave lines
3. Superconducting coaxial lines
4. Cryogenic Isolators
5. Quantum Amplifiers
6. Cryo-perm shield
7. Mixing chamber

How it is actually implemented in real world?



Qubits readout architecture



Basic architecture for Qubit readout

Semiconductors	Minimum temp.
Si BJT	100 K
Ge BJT	20 K
SiGe HBT	< 1 K
GaAs MESFET	< 4 K
CMOS	30 mK or below?

Technologies for Quantum circuits

- Frequency 6G-12GHz
- LNA noise: <100pV/sqrt Hz
- Resolution> 10bit
- Timing accuracy <100ps

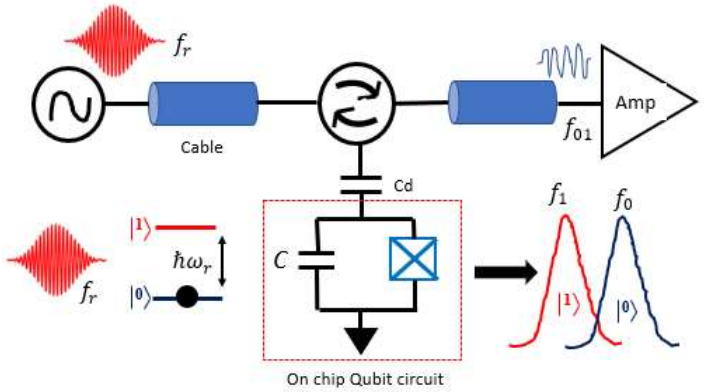
Brookhaven National Laboratory

ASIC for quantum control and readout

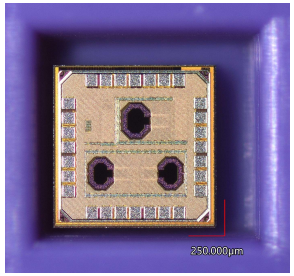
Developing an ASIC in CMOS technology operating at cryogenic temperatures for quantum control and readout

The biggest challenges are:

1. the absence of simulation device models, which reliably describe the behavior of devices in extreme cryogenic operation
2. avoiding interfering with the qubits
3. achieving the challenging low noise performance required without exceeding the tight power budget compatible with the cooling capacity of the cryogenic environment (which scales exponentially from ~1 W at 4 K to ~400 μW at 100 mK)



RF readout of qubits or quantum sensors



Quantum RF Chip Prototype 1 (QRFCP1)

V. Manthena: "A 1.2-V 6-GHz Dual-Path Charge-Pump PLL Frequency Synthesizer for Quantum Control and Readout in CMOS 65-nm Process", IEEE UEMCON - best presentation award

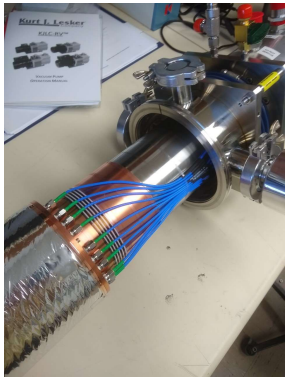
Brookhaven National Laboratory

Quantum RF chip prototype

- Started with characterization of CMOS structures at cryo-temperatures and extrapolation of models
- Developed sub-circuits of microwave signal generation (phase locked loop synthesizer, VCO's, amplifiers) in CMOS 65 nm process, which work at cryo-temperatures

Test chip performance

- Supports temperature range from 300K to 4K
  - Interesting to measure at LAr/LN/LXe temperature helping ongoing and future experiments



Cryostat for test

QRFCP1

- Designed in 65 nm process using 9 metal stack
- Chip size is 1 mm x 1 mm
- **VCO and CML divider are heart of Phased Locked Loop (PLL)**
- Chip hosts four different test structures
  - Regular Voltage Controlled Oscillator (VCO)
  - Quadrature Voltage Controlled Oscillator (QVCO)
  - I2C for configuration
  - CML divider
- Dedicated power supply for each test structure to measure the power dissipation
- The slow control configuration is carried out using I2C
- VCO's have a center frequency of 5.12 GHz
- All high-speed output signals are differential

Conclusions

- Microelectronics is at the heart of advanced instrumentation
- Constantly increased role → expect a bright future
- There is more to do → particularly access to the foundries
- Data/power problem?
- Embedded AI/neuromorphic/edge processing

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