Pacific MicroCHIP Corp.

An ASIC With a Low Power Multichannel ADC for Energy and Timing Measurements

Streaming Readout Support

Presenter: Anton Karnitski

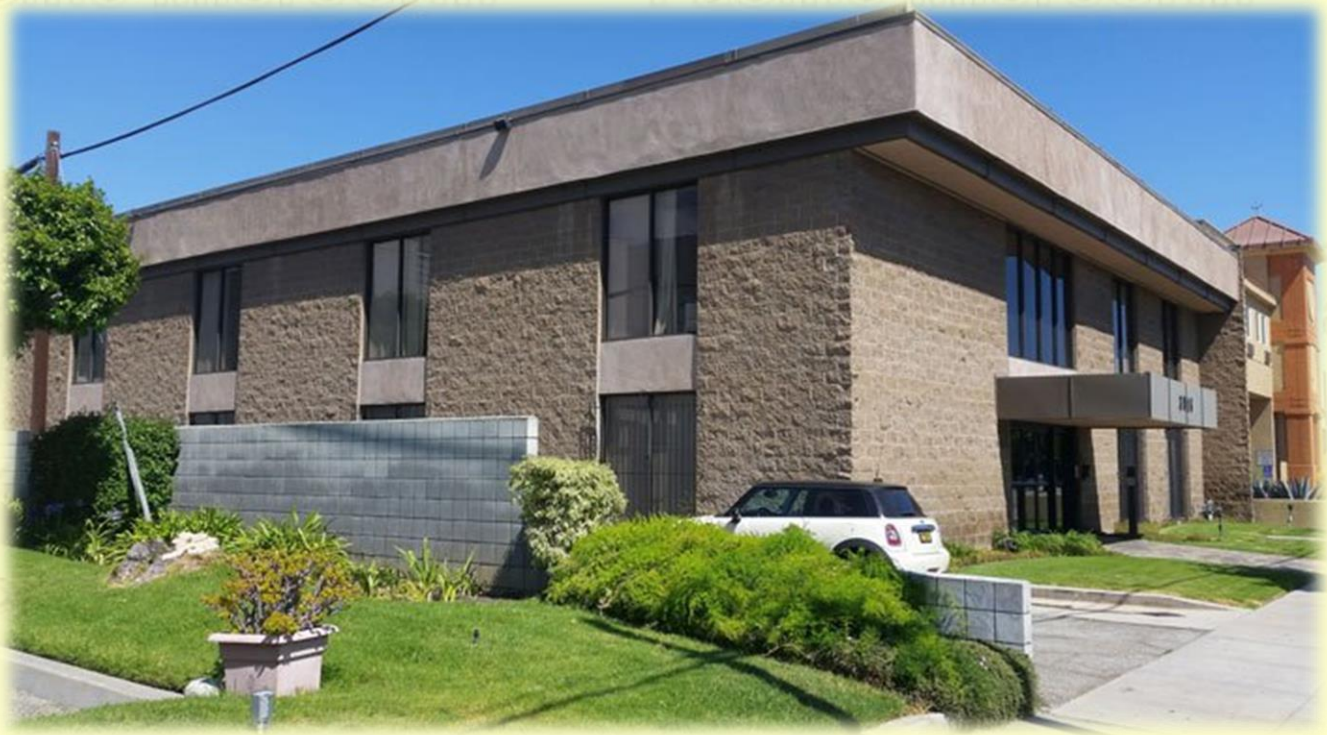
OUTLINE

Pacific MicroCHIP Corp.

- The Company, its Specialization/Expertise
- Phase II objective
- Multichannel ADC for energy and timing mesurements specifications
- ADC core architecture
- Digital architecture
- ADC data output interface
- Event-driven backend and output DATA frame structure
- ASIC layout / floorplan
- Assembled part and test board
- ADC testing results and pulse processing
- Future plans

COMPANY

- Pacific MicroCHIP Corp. is incorporated in 2006.
- It is headquartered in Culver City, California
- Main focus – providing IC/ASIC design services and turnkey solutions.



CORE EXPERTISE

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (SiGe/CMOS) down to 7nm

PHASE II OBJECTIVE

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- To design circuits and layout for the ADC ASIC.
- To fabricate the chip.
- To package the chips.
- To develop the test PCB and socket for the ASIC.
- To develop a GUI and a testbench.
- To test and characterize the ADC ASIC.
- To prepare a datasheet for marketing.
- To submit deliverables to the DoE.

ASIC SPECIFICATION

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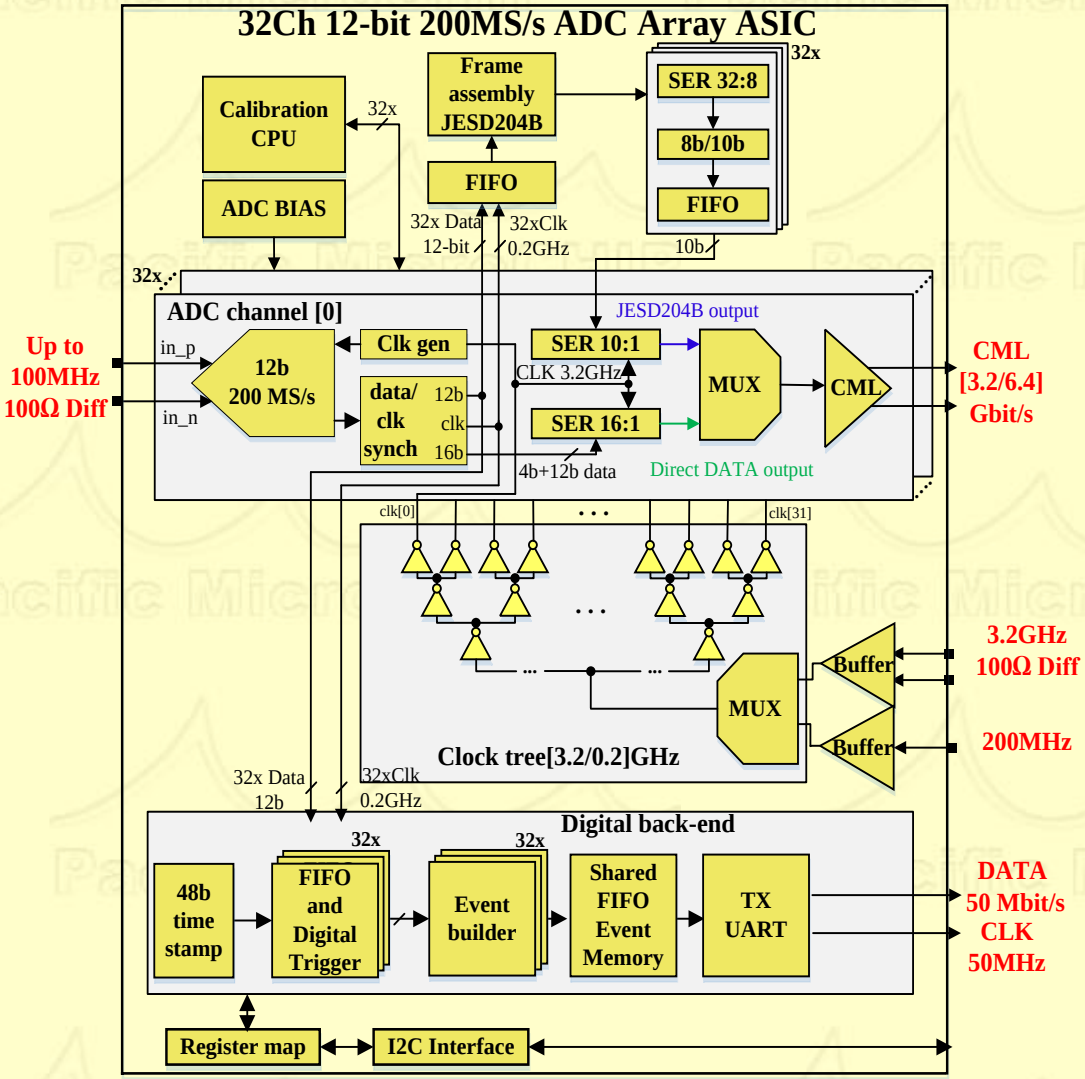
FEATURES:

- 32 independent channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input signal
- ENOB > 10-bit
- Programmable input signal bandwidth 0.1-0.3 GHz
- Integrated event-driven digital backend
- JESD204B output data interface
- Extended temperature range -40C..+125C
- Low power consumption 5 mW / channel (w/o interface)
- I2C interface for ASIC control



ADC CORE ARCHITECTURE

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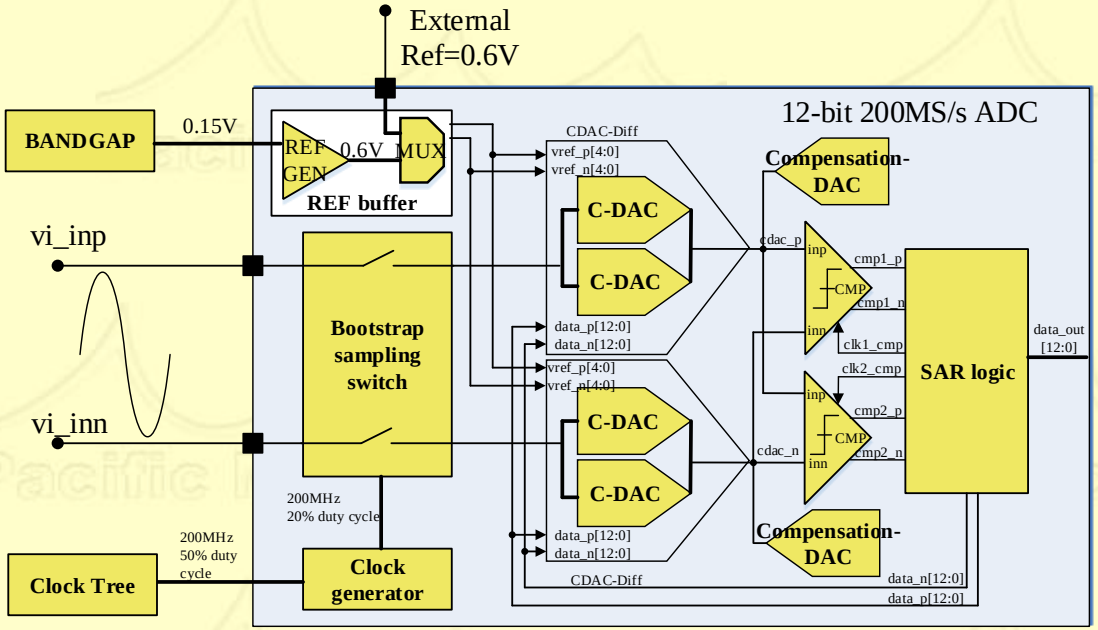
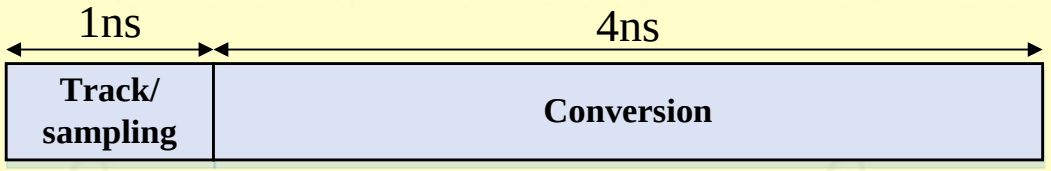
FEATURES:

- 12b SAR ADC architecture
- Segmented 3t-9b CDAC
- Optional external/internal ADC reference voltage source
- Fractional reference voltage
- Dual comparator
- Asynchronous logic
- Built-in FSM for comparator offset compensation
- Built-in FSM for CDAC non-linearity calibration

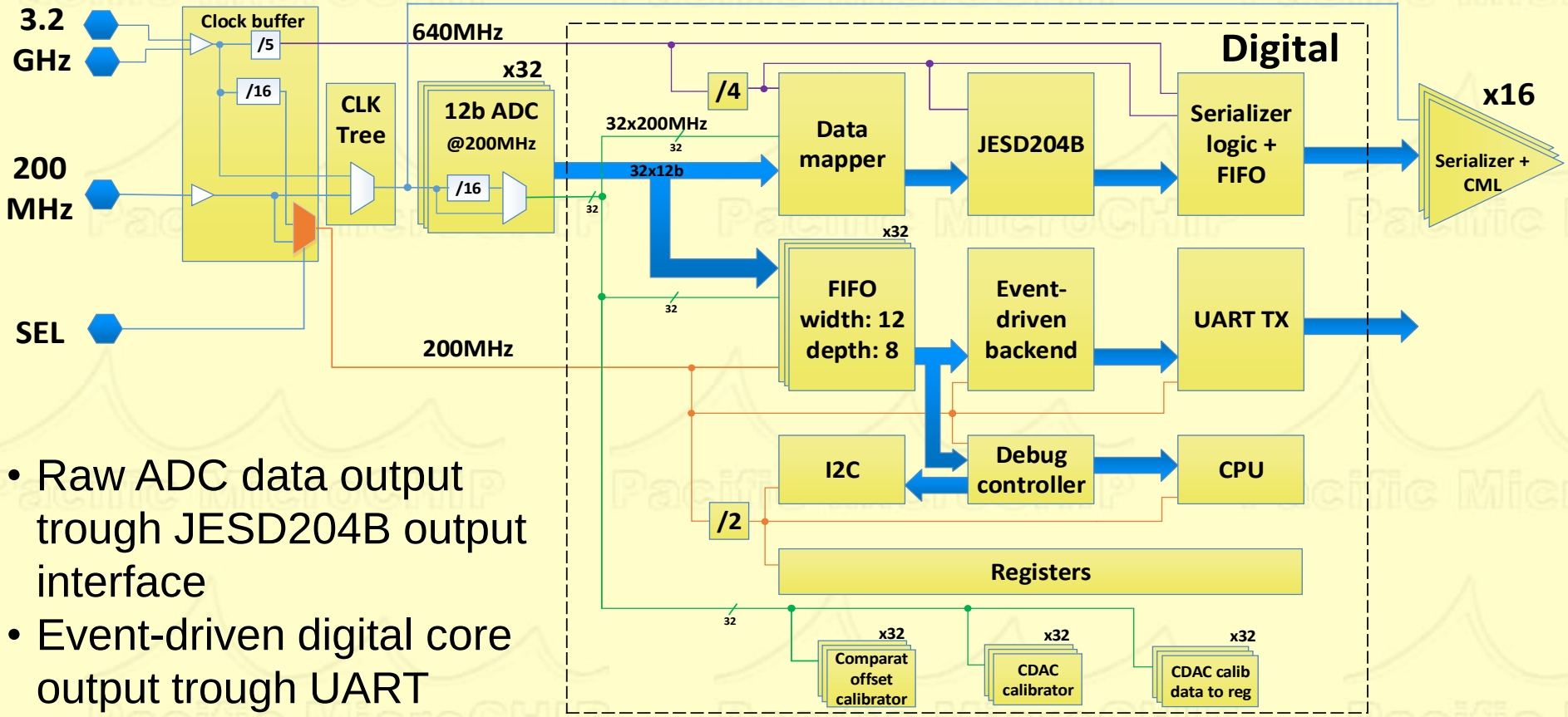
ADC CORE BLOCK DIAGRAM:



ADC TIMING DIAGRAM:



DIGITAL ARCHITECTURE



- Raw ADC data output trough JESD204B output interface
- Event-driven digital core output trough UART interface
- I2C interface for ASIC control registers programming
- Built-in calibration FSM / CPU for calibration purposes

RAW ADC DATA OUTPUT

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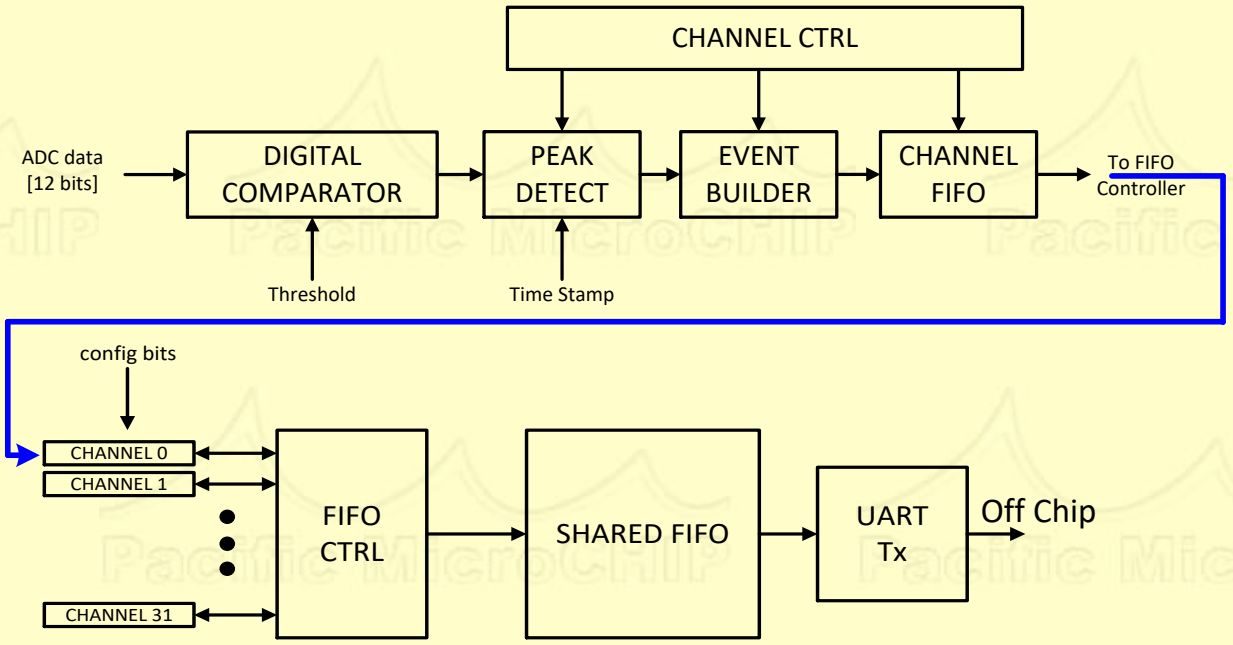
Mode	JESD 204B lanes	ADC per lane	Lane data rate	ADC data rate
Full speed	16	2	6.4Gbps	200MS/s
Half speed	8	4	6.4Gbps	100MS/s
Quarter speed	4	8	6.4Gbps	50MS/s

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate 6.4Gbit per second
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

EVENT–DRIVEN BACKEND

- This ADC output is monitored by a digital comparator with a programmable threshold

- When the ADC input exceeds threshold, a time stamp is assigned and the peak value of the incoming ADC data is recorded.

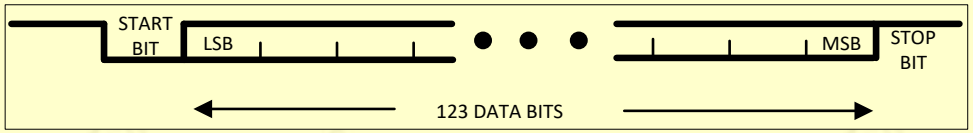


Event-driven digital backend was built in collaboration with LBNL. And we want to thank Dr. Carl Grace for his effort.

- When the event is completed, the relevant information is assembled into a packet by the Event Builder block. When the shared FIFO is ready, events stored in the channel FIFO are read out.

OUTPUT DATA FRAME

Bits	Field Name	Comment
[123]	Parity	Used to monitor integrity of data transmission.
[122]	Event Declaration	0 → test event (see text), 1 → normal
[121:119]	Fixed	Fixed bits - should always read value 3'b011
[118:107]	Window Interval	Determines the number of ADC samples to examine looking for a peak.
[106:102]	Channel ID	5-bit unique identifier.
[101:54]	TOA (Time of Arrival)	The timestamp of where the ADC value passed the threshold. Covers ~16 days at a 200 MHz clock rate.
[53:42]	TOP (Time of peak)	Supports shaper peaking times of up to 20 µs at a 200 MHz clock rate.
[41:30]	TOT (Time over Threshold)	Supports shaper pulse widths of up to 40 µs at a 200 MHz clock rate.
[29:18]	Peak Value	12-bit peak value recorded in the event.
[17:6]	Channel Threshold	12-bit threshold value used during this event.
[5:0]	Shared FIFO usage	For diagnostics and debugging.



50Mbps / 124+2bit / 32ch
≈ 12.4k events per second per channel

ADC POWER CONSUMPTION

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Block	Analog supply current, mA @ 0.9V	Digital supply current, mA @ 0.9V	I/O supply current, mA @ 1.2V	Ground, mA @ 0V
ADC CHANNEL	1.65	7.82	14.88	25.03
ADC CORE 12b@200Msps	1.46	1.62	N/A	3.73
JESD204B PHY	N/A	4.58	14.88	19.48

Typical power consumption of ADC w/o DATA interface: **5mW / ch**

Typical power consumption of ADC with DATA interface: **15.7mW / ch**

(*One JESD204B output data lane used per 2 ADCs operates at 200Msps*)

ASIC FLOORPLAN

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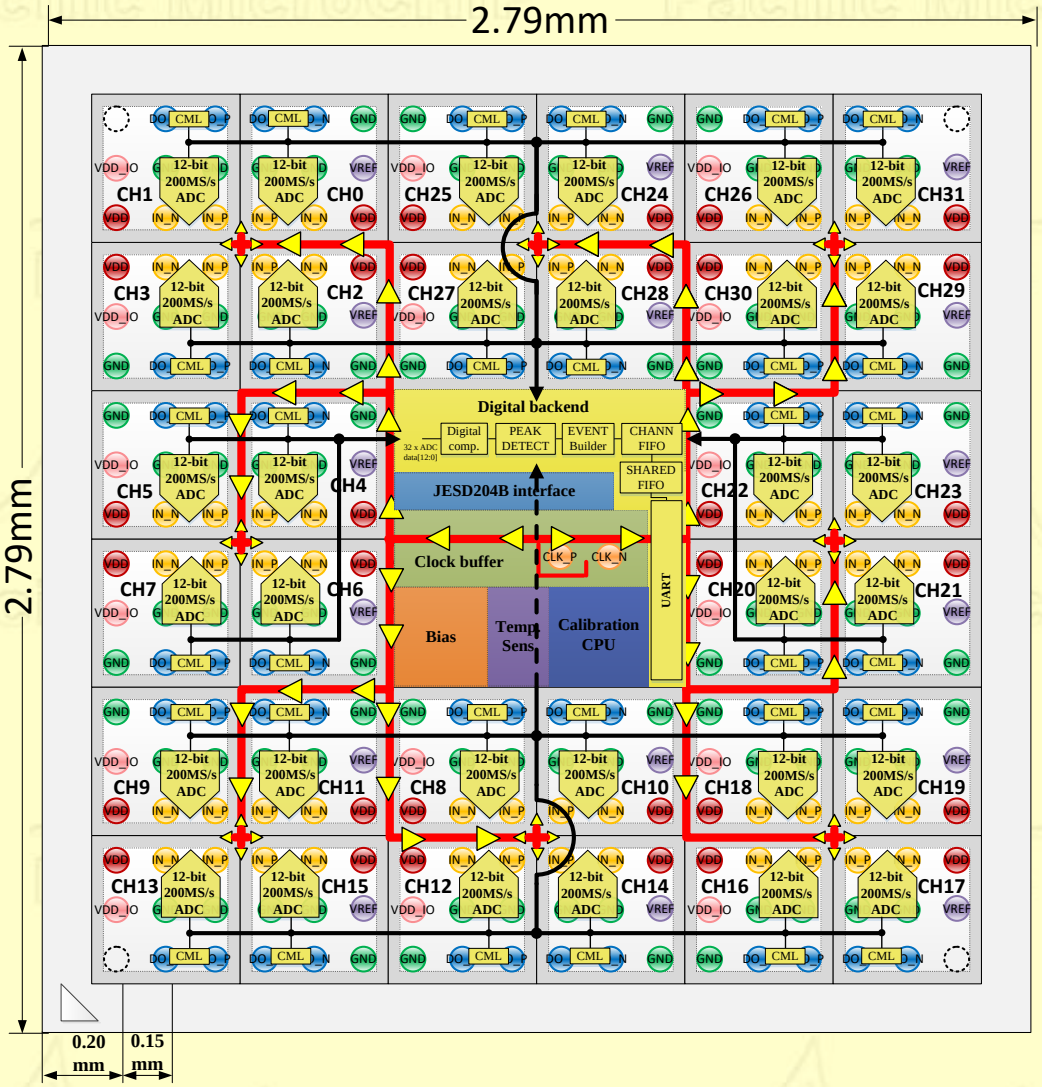
FEATURES:

- External clock input
- Can operate from 3.2GHz or 0.2GHz reference clock
- Integrated ADC sampling clock duty cycle correction
- Synchronous clock/reset for 32 ADC channels
- Integrated CPU
- Integrated temperature sensor



MULTICHANNEL ADC ASIC LAYOUT

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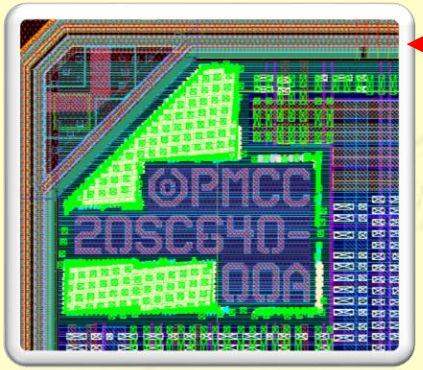
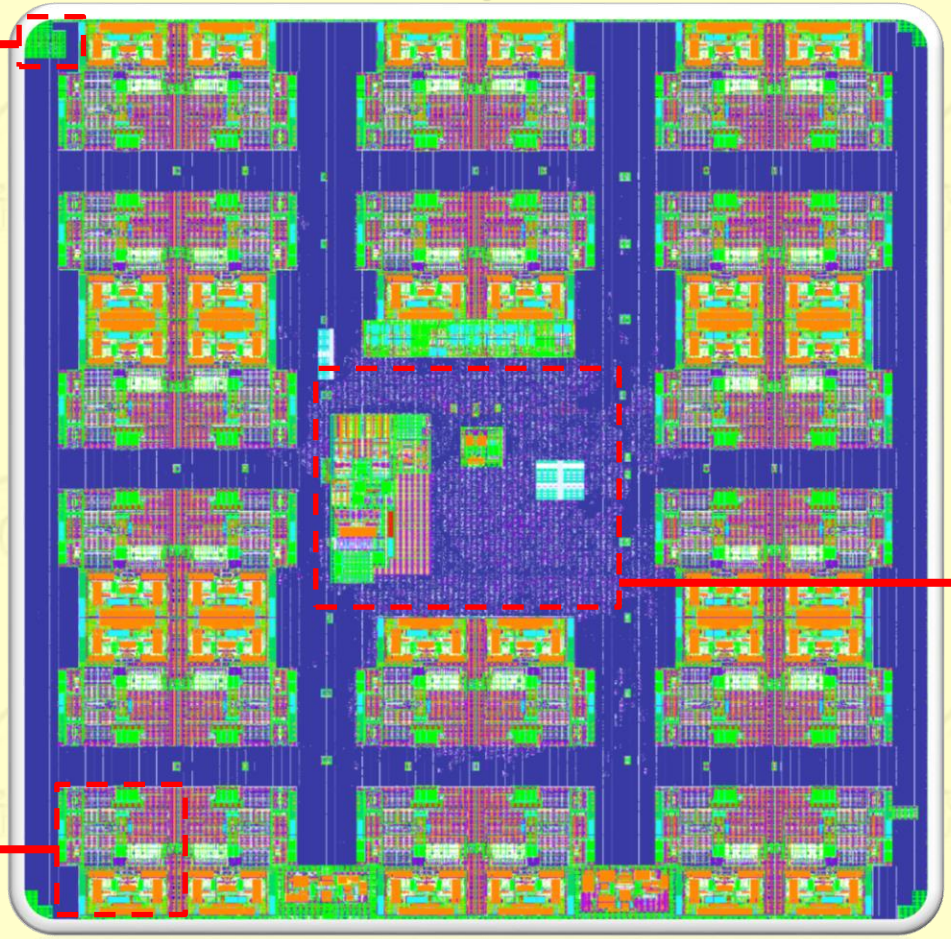
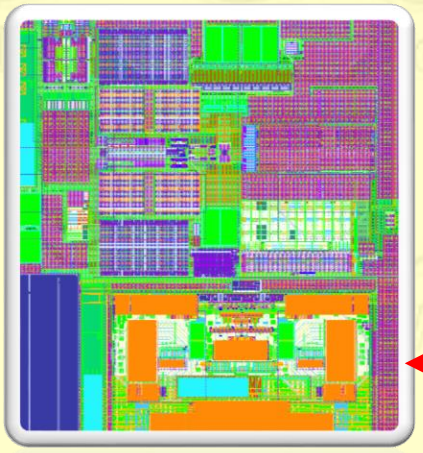
Logo



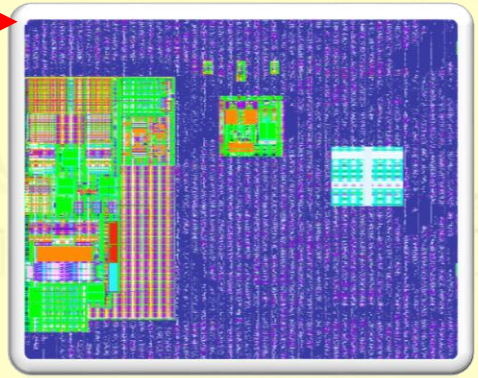
ASIC top level



ADC channel



Bias & digital core



CHIP, ASSEMBLED PART AND TEST BOARD

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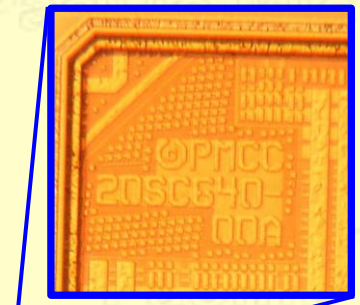
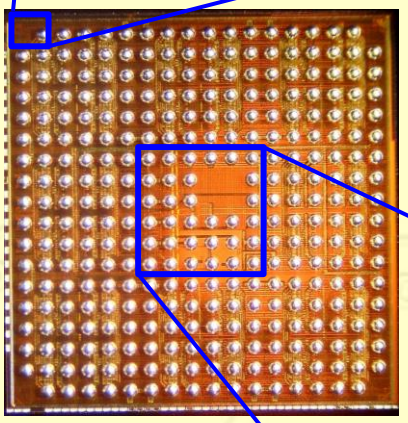
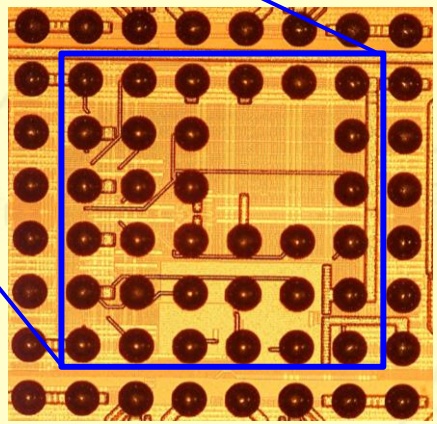


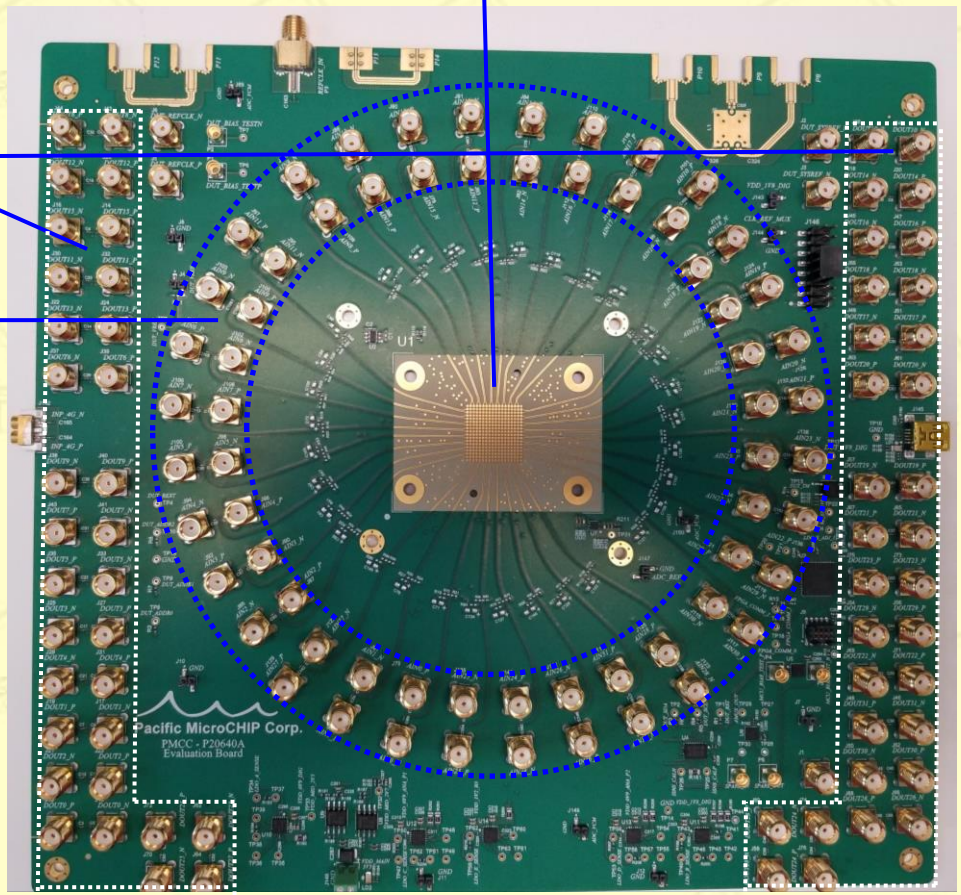




Area for DUT socket

ADC direct output

Analog inputs



TESTING RESULTS : PERFORMANCE

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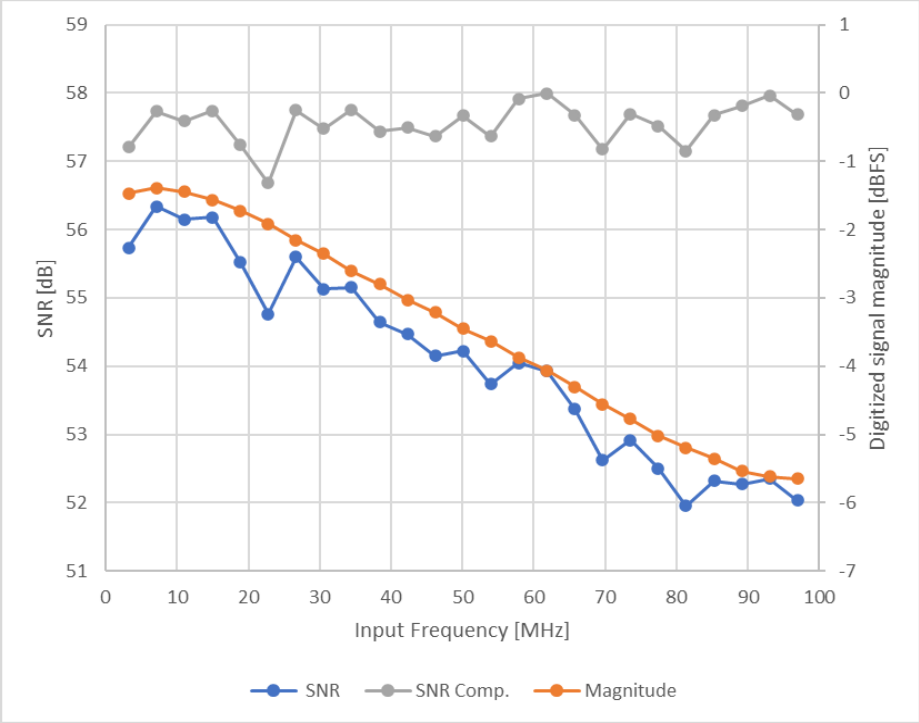
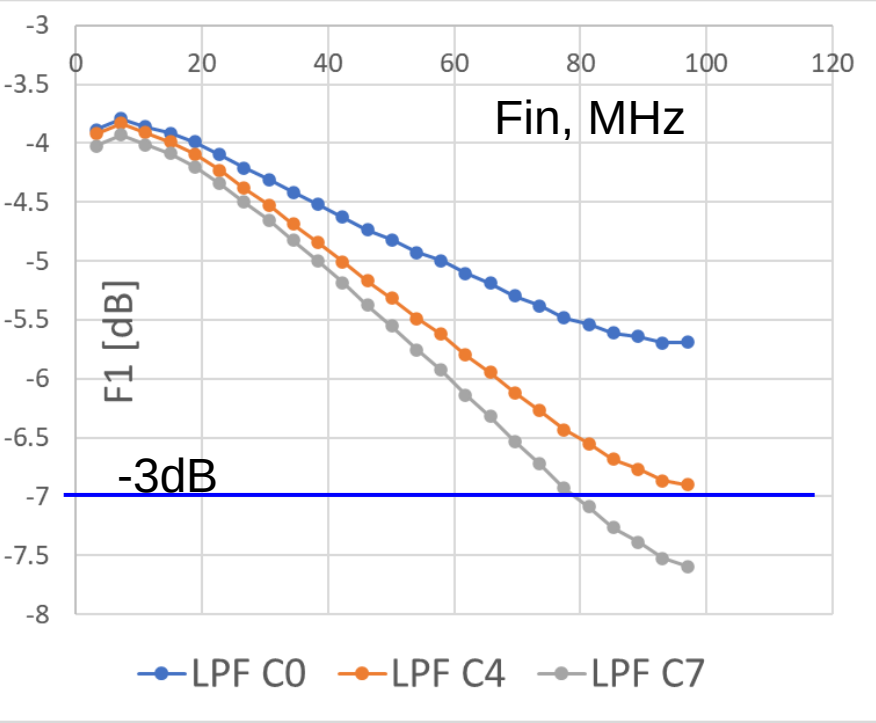
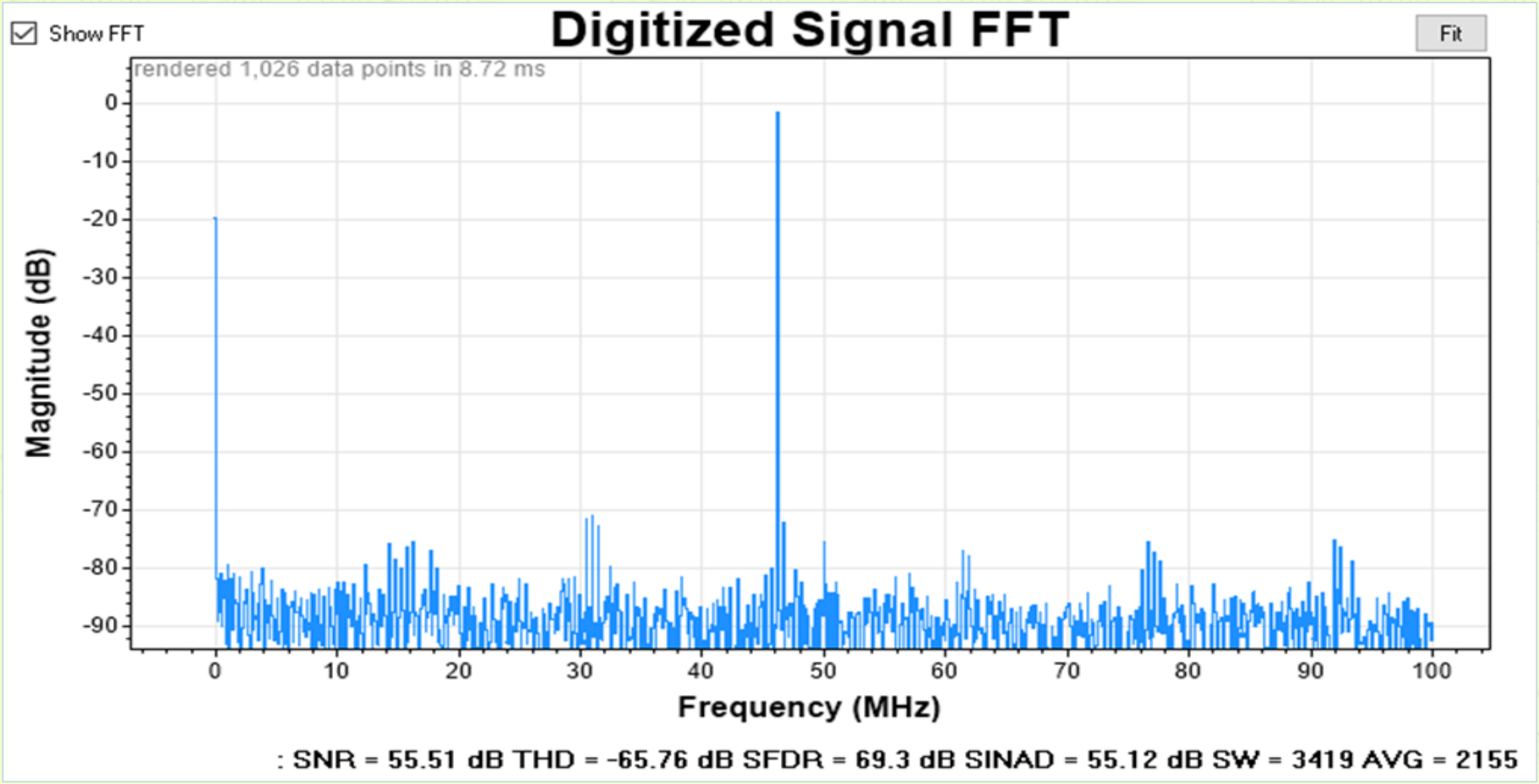
SNR within 56dB to 57dB => ~9-bit
ENOB Target is >10-bit ENOB

BW depending on LPF coefficients:
40MHz to 60MHz @ -1dB
80MHz to >100MHz @ -3dB





TESTING RESULTS : SPECTRUM



Simulated: **SFDR > 74dB**, **ENOB > 10.4-bit** for Fin<100MHz

Tested: **SFDR > 69dB**, **ENOB > 8.9-bit** for Fin=47MHz

PULSE PROCESSING

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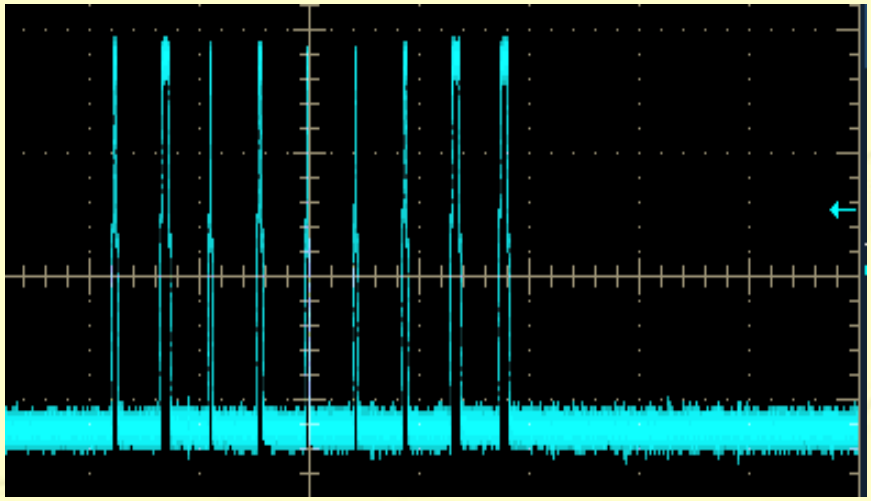
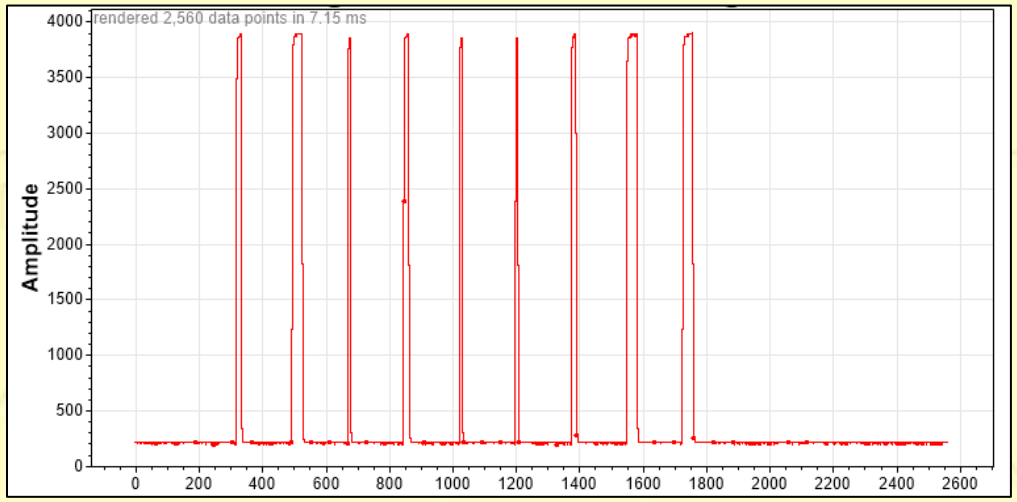
Incoming Pulses



Digitized Pulses



Event Builder Output Data

Par	Event	Fixed	Wind	CH	TOA	TOP	TOT	PEAK	THRESHOLD	SHARED
1	1	3	64	4	578680317105	13	17	3893	1024	0
1	1	3	64	4	578680317281	11	33	3893	1024	0
1	1	3	64	4	578680317457	6	9	3861	1024	1
0	1	3	64	4	578680317633	13	17	3893	1024	1
0	1	3	64	4	578680317809	6	9	3861	1024	2
1	1	3	64	4	578680317985	6	9	3861	1024	3
1	1	3	64	4	578680318161	14	17	3893	1024	3
1	1	3	64	4	578680318337	14	33	3893	1024	4
0	1	3	64	4	578680318513	31	33	3904	1024	5

FUTURE PLANS

Pacific MicroCHIP Corp.

- Transition to SBIR Phase IIA or IIB – to redesign the chip, increase its performance, fix issues identified during testing.
- To fabricate the final chip.
- To test/evaluate it.
- To provide the chip to the NP community and commercial customers.

THANK YOU

Application Ideas for the ADC ASIC are appreciated!