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Design and Measurement of the High Density Digitizer System on Chip (HDSoC): A 64 Channel 1-2 GSa/s Waveform Digitizer for High Density Detectors

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Tuesday, August 23, 2022
Virtual 2022 DoE Exchange Meeting

Tuesday, August 23 2022 11:05 am EDT

Work partially funded by US DOE DE- SC0020457 grant

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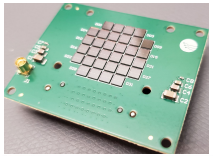
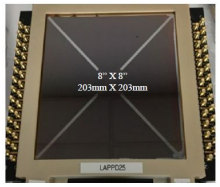
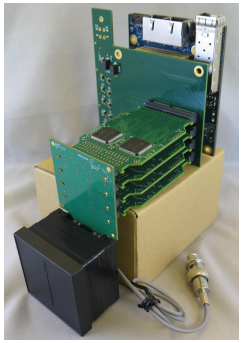
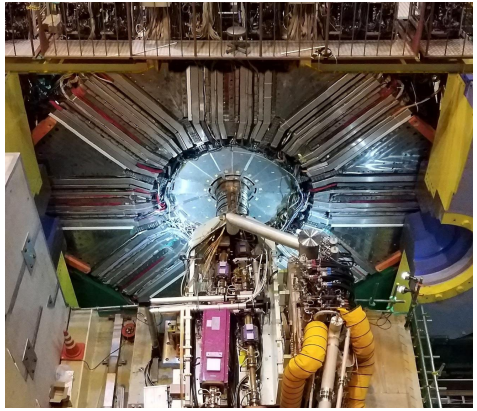
WAVEFORM DIGITIZER SoCs
FOR PRECISE TIME OF FLIGHT ESTIMATION









1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

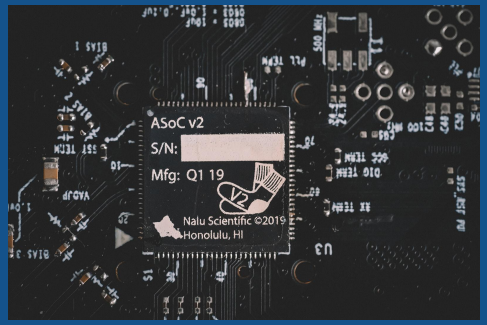
- SiPM
- PMT
- LAPPD
- Detector arrays

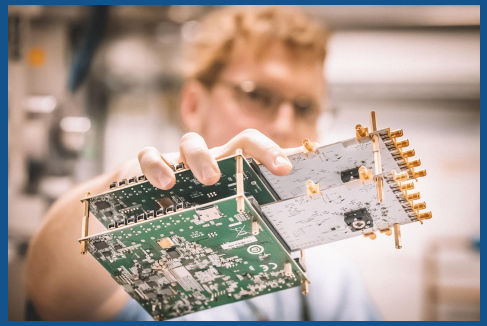
3a. Main application:

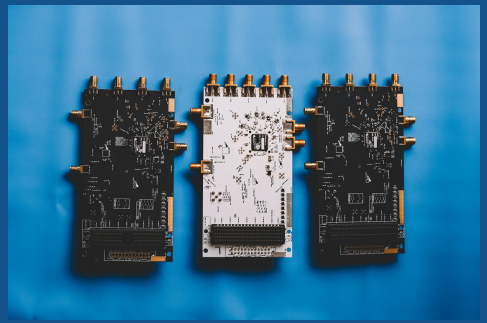
- NP/HEP experiments
- Astro particle physics

3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging







ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members-diverse background
- Access to advanced design tools
- Rapid prototyping and testing lab

Technical Expertise

IC design:	Analog + digital System-on-Chip (SoC)
Hardware design:	Complex multi-layer PCBs
Firmware design:	FPGAs, CPUs
Software design:	GUI, analysis, documentation

Scientific Expertise - NP/HEP subject matter experts

- Physicists (3x)
- Electronics for large scientific instruments

Exclusive Distributor Agreement for North America

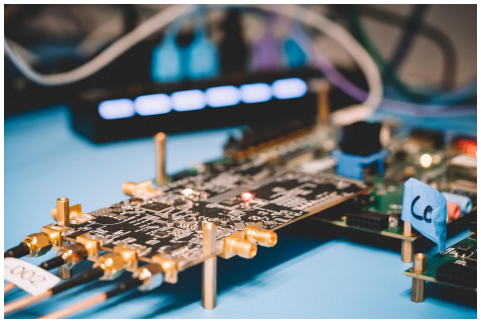
- Sales of ASICs, eval boards
- Enhanced OEM opportunities

CAEN Technologies Inc.

Nalu = 'wave' in native Hawaiian language

Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	Rev 1 avail
AARDVARC	8-14	2.5	32k	4	10	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5-2	4k	16/32	10	Rev 1 avail



- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
  - Baseline readout for EIC hpDIRC
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option

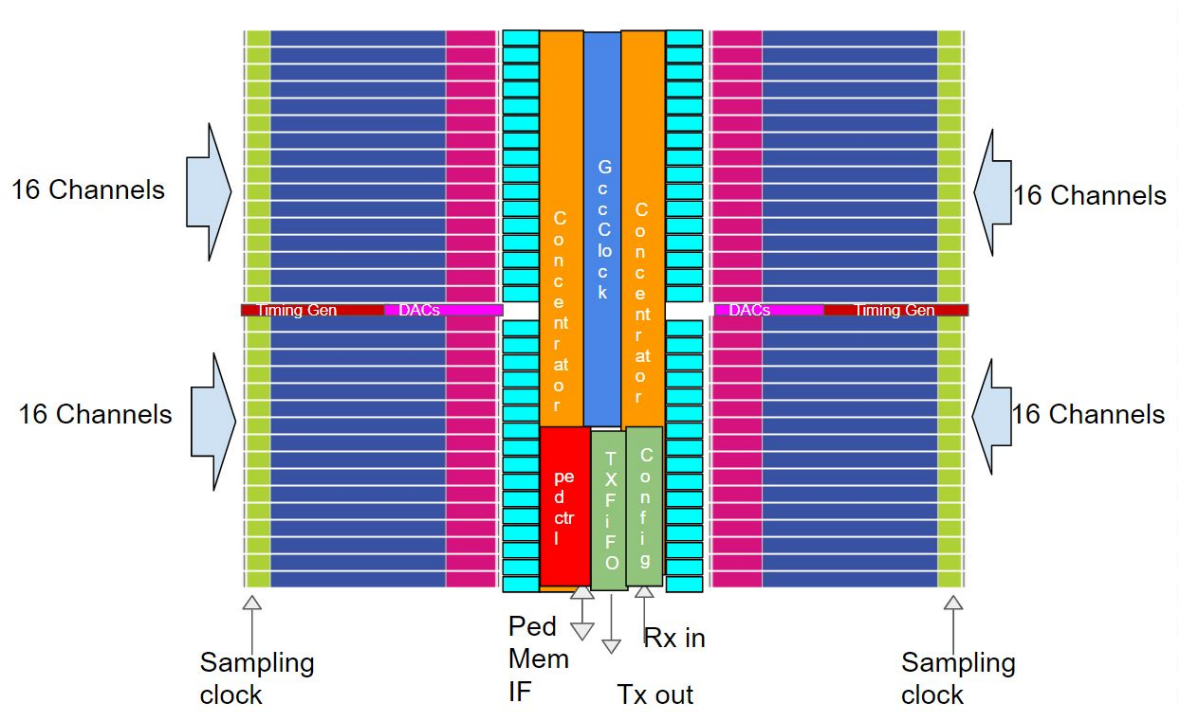
Work funded by DOE SBIRs. University of Hawaii as subcontractor.

High Density Digitizer SoC - concept

Readout Integrated circuit with the following features:

- Very High density (64 channels) to support high channel count sensors:
  - SiPM arrays, MA-PMTs, LAPPDs
- Full Waveform sampler and digitizer
- High sampling rate 1-2 GSPS
- Input stage with current amplification
- Long internal buffer (2048 samples) and virtualization
- On chip data reduction/feature extraction for high rates (>100kHits/second)
- On chip discriminator for self-triggering, window marking - exported in serial stream
- Serial interface (>=500 Mb/s)

64-Channel HDSoC Floorplan



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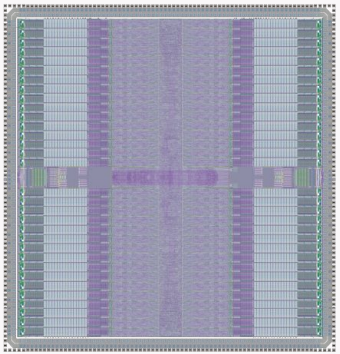
64-Channel HDSoC concept



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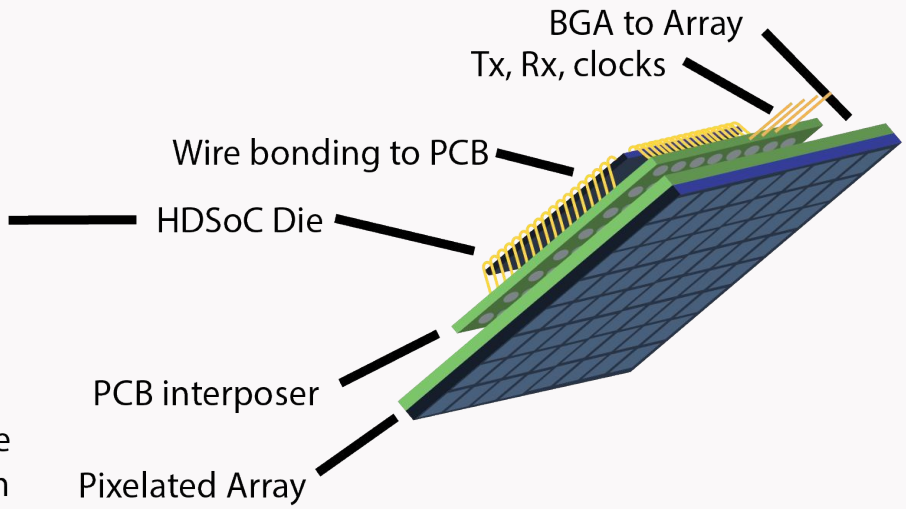
HDSoC V1 64 channel estimate
64 channel = 7.2 mm x 7.4 mm



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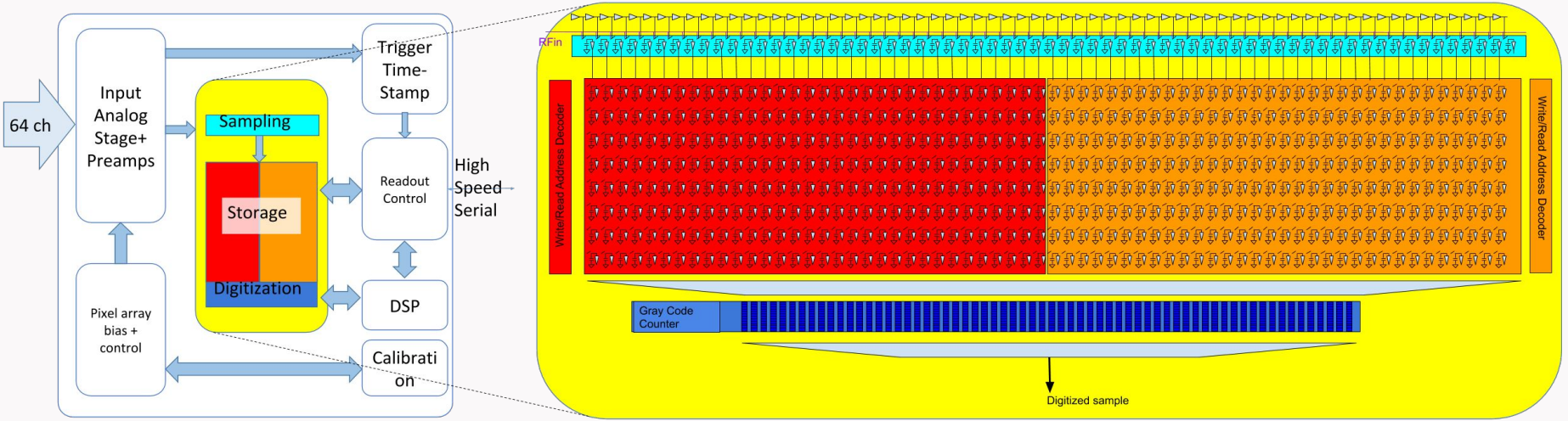
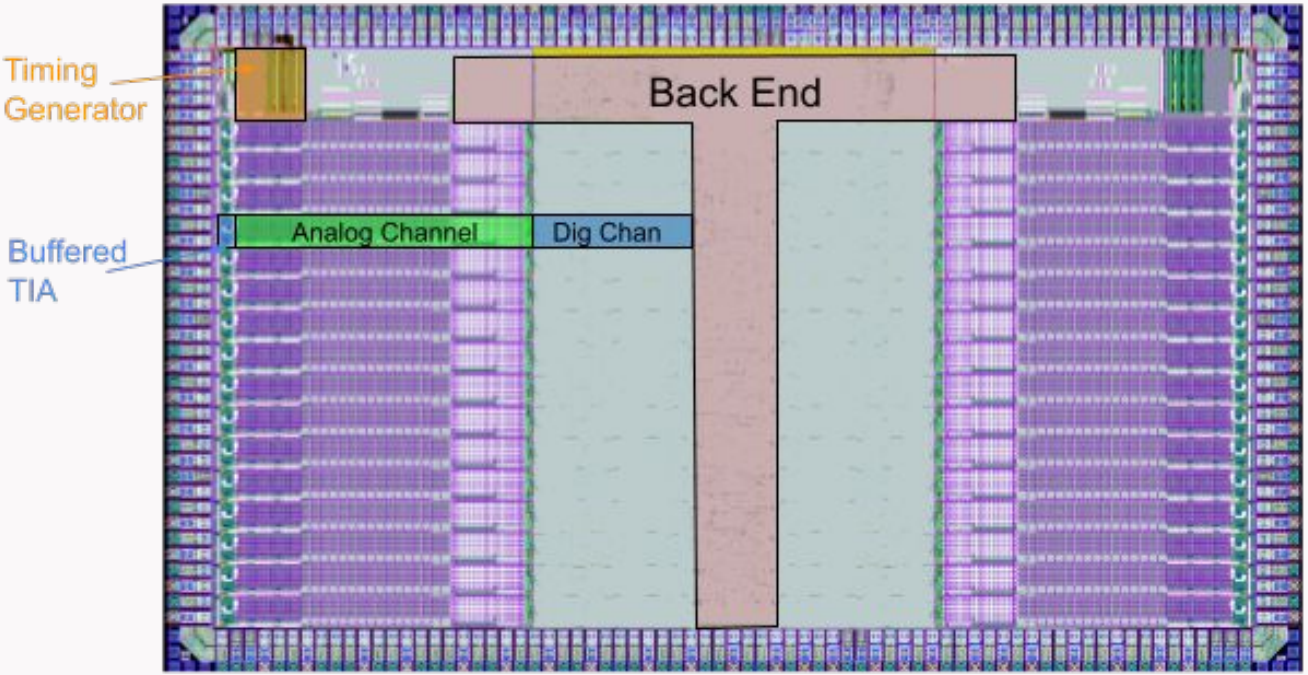
Channel Architecture



HDSoC Rev. 1 Layout - 32 ch proto



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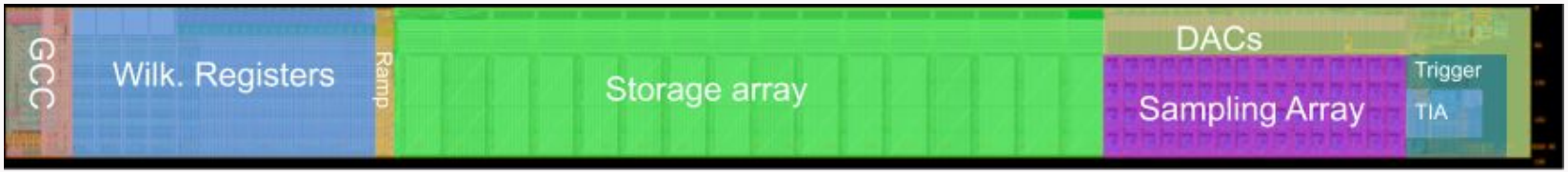
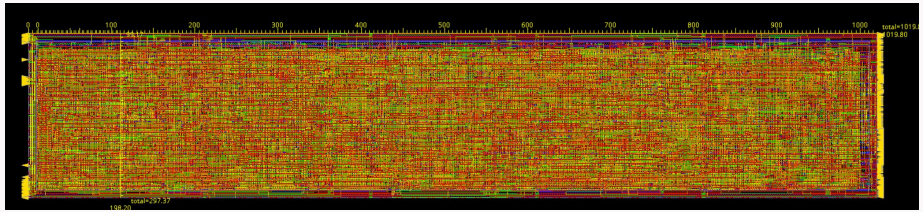
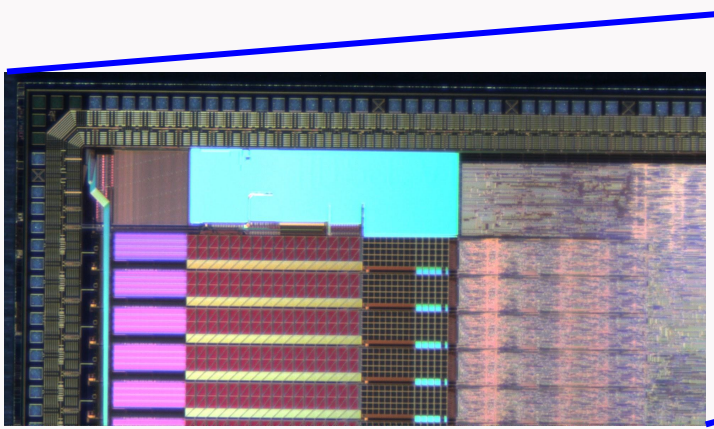
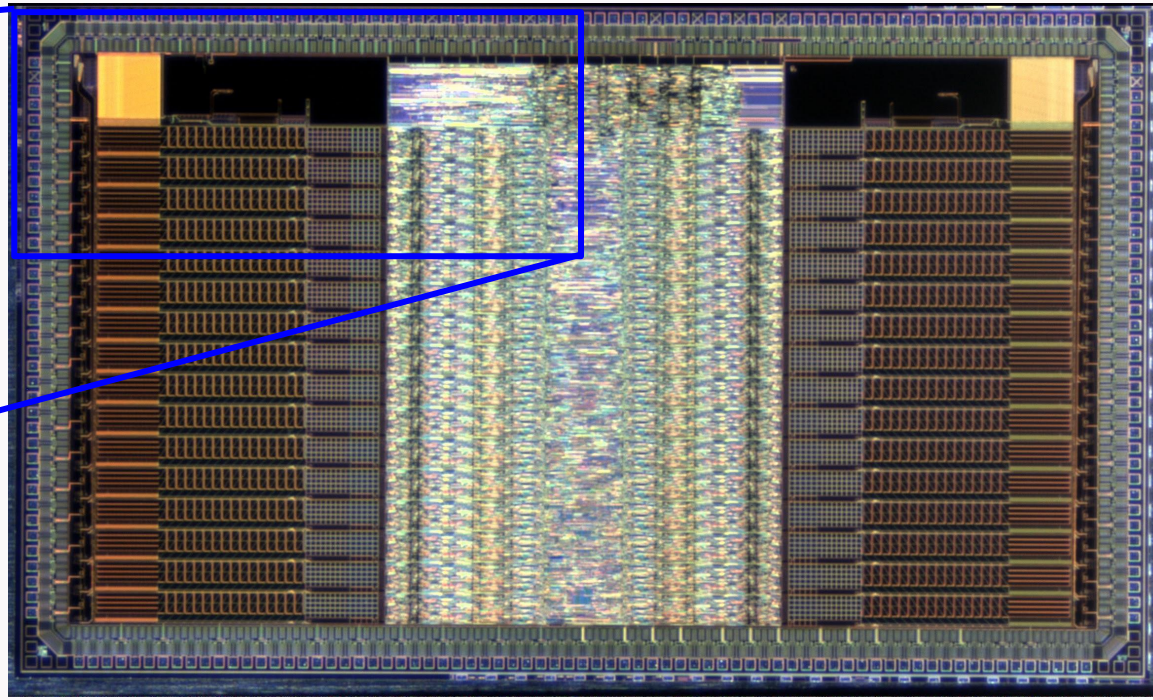
HDSoC Rev. 1 Channel Layout (Mixed signal and digital control)





HDSoC Rev. 1 Die



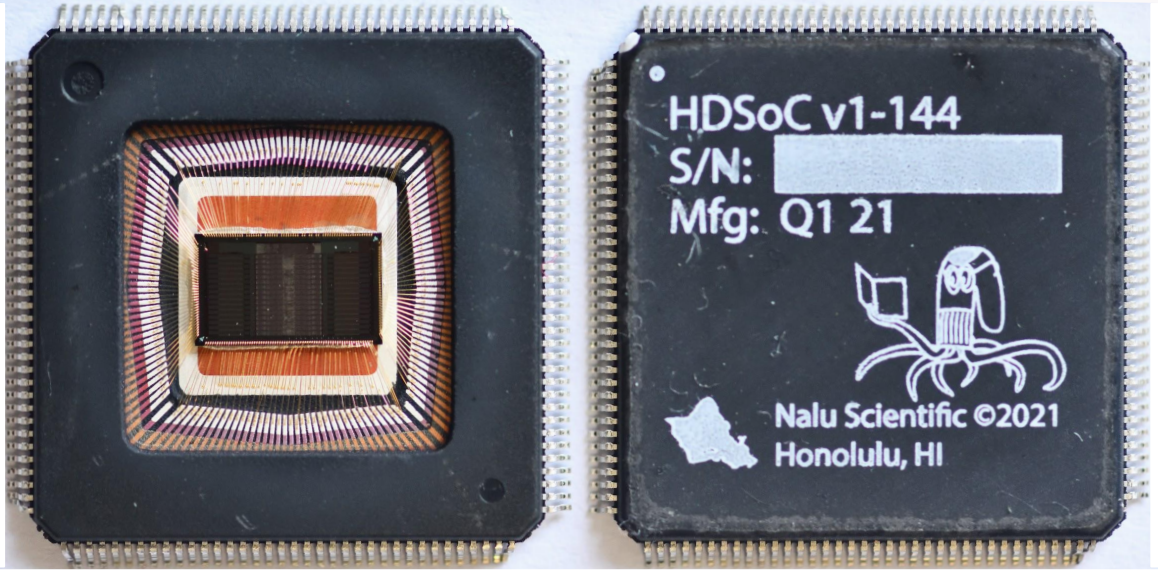


HDSoC Rev. 1 Package

Packaged in QFP144 (22 mm side)
All I/Os connected:

- Serial IF
- Parallel IF

After validation, a smaller package (LQFP128 - 16mm side) with only serial interface will be used.
Ultimately - a custom package will be used to reduce the footprint.



HDSoC v1 design specs

Specifications	
Sampling Rate	1-2 GSPS
ABW	0.8-1GHz
Depth/channel	2048 Samples
Trigger Buffer	~2 us
Max rate w/out deadtime	23kHz/channel (full readout) 200kHz hits/array
Channels	32
Supply/Range	2.5V/0.5-2.2V
ADC bits (stated res.)	12
Timing accuracy	Better than 100ps
Technology	250 nm CMOS
Power	20-40mW/ch

Tested at 1 GSPS - currently being tested up to 2 GSPS

Based on 1GSPS

Maximal <u>including header and 8b10b encoding overheads</u> - assumes full readout of 1 window (32 samples) and operation at maximum speed for serial interface (500 Mb/s) and system clock (125 MHz) - feature extraction will be implemented in v2 - current tested limit 13.2kHz @312.5MHz serial interface and 31.25MHz system clock.

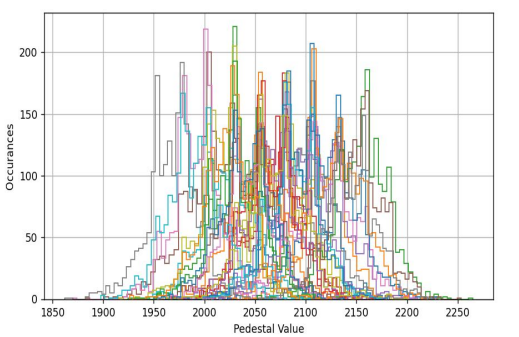
Currently measured higher ~47mW - Some sources of extra power identified - to be fixed in V2
Includes: sensor bias, amplifier, trigger, data transfer.

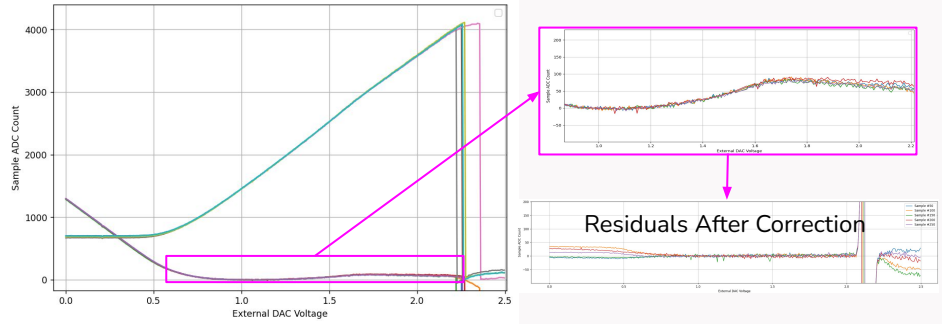
HDSoCv1 tests and measurements

- Digital interface and configuration:
  - Configuration of mixed-signal partition
    - Timing generator - control of speed and DLL registers
    - Transfer buffer biases
    - Ramp generation biases
    - Discriminator thresholds, offset adjustment and bias
  - Configuration of digital backend
    - Streaming pattern (for trigger outputs)
  - Configuration of individual channel (individual or broadcast)
    - Write modes
    - Acquisition modes
- Timing configuration:
  - Two timing generators (East and West):
    - Use an external reference clock @1/64th of sampling rate
    - Main (rising) edge for all timing critical signals by a voltage that can be generated in closed loop via DLL
  - Functionality verified @ 1 GSPS (currently being checked up to 2GSPS) (DLL locking and other timing strobes)
- Waveform collection and power measurements - see next slides

HDSoCv1 Static accuracy

- "Pedestal" evaluation:
  - Due to internal offsets the individual sample values need to be calibrated
  - Statistics on the individual readout for the calibration can be used to estimate the "static error" at bias level -> ~2 ADC count standard deviation
- Varying the input bias to the chip allows studying the overall non-linearity of the conversion - pattern can be calibrated in a large range (1.2V) with residual of ~5 ADC counts (3 ADC counts for a central range of ~200mV)





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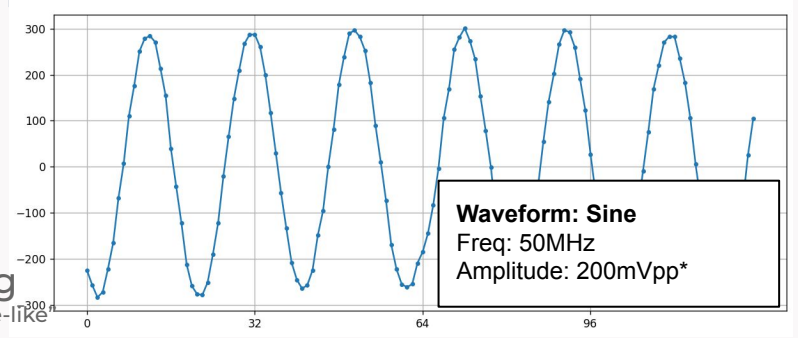
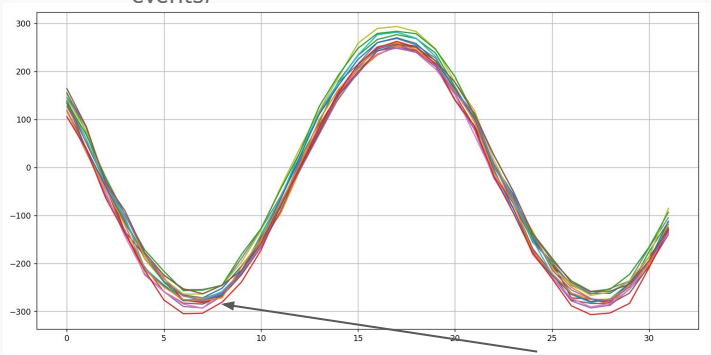
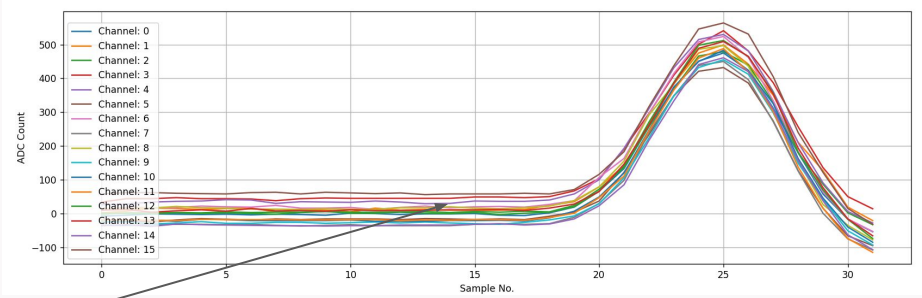
Waveform collection

- Waveform collection, initial calibration
  - Single channel acquisition
  - Sine wave input case
  - Proper timing (“stitching”) across windows
  - First order amplitude calibration
  -
- Multi-channel: synchronized data taking
  - Same signal split into multiple channels (sine and “pulse-like” events)



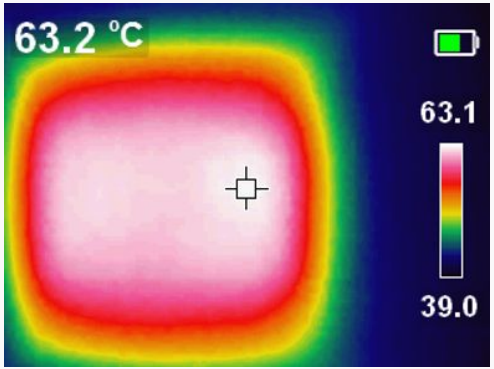




Signal drift resolved - issue with board biasing network

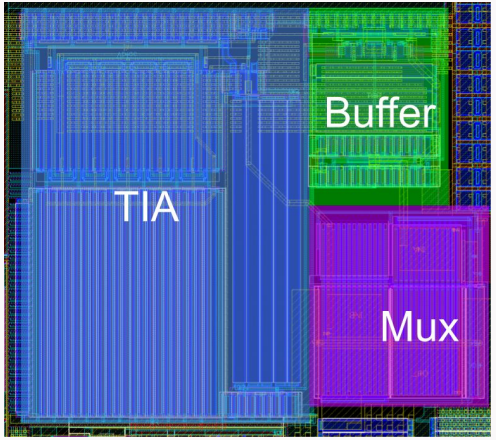
Power and package temperature

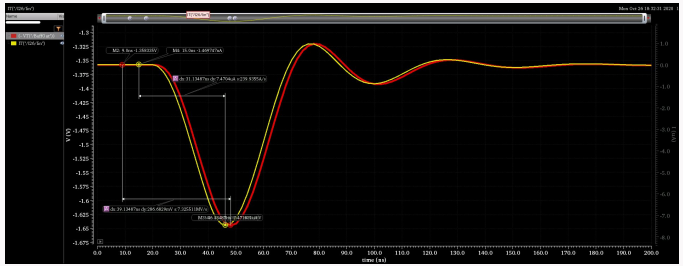
- Full chip configured and acquiring data
- Overall power draw: 1.5W
  - 47 mW/channel
  - ~12.5 mW for transfer buffers
  - 3.7 mW for buffered TIA
  - Overhead: - digital+biases/large number of DAC buffers -> will minimize in rev. 2
  - Fast clock power can be substantially reduced with appropriate gating



HDSoC Rev. 1 buffered TIA

- Common gate input with feedback on tail transistor to permit some bias control
- Followed by a buffer to drive the sampling array (standard 2 stage OTA)
- Simulated with a SiPM model:
  - Transimpedance of ~39 kohm
  - Noise - 5.7mV - SNR ~50V/V
- TIA can be excluded from the signal path, allowing use of external TIAs
  - Current version has BW limitations - new version being designed and will be incorporated in the next revision



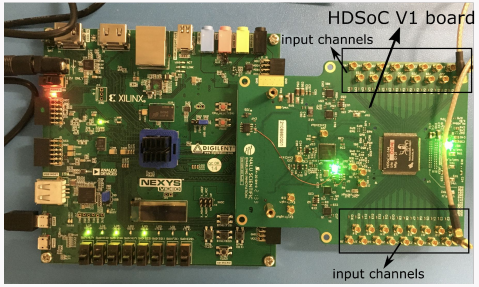


SiPM readout experiments

1. HDSoC V1 connected to a Digilent Nexys FPGA board with a serial communication interface, and connected to a SiPM array.
2. SiPM pulses acquired via HDSoC self-triggering capability
3. SiPM pulse template (via averaging) calculated.

   A spline fit was used to smooth the averaged pulse.
4. Template fit to estimate the amplitude of the pulse peak.
5. Pulse peak histogram shows maxima for 2 PE, 3 PE depending on the trigger threshold

1



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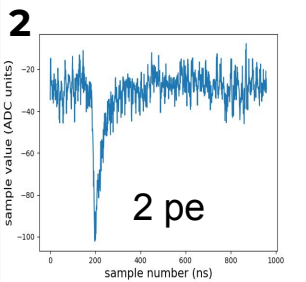

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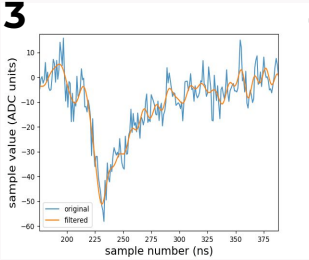

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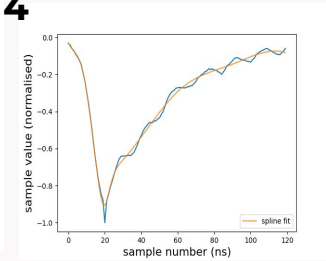

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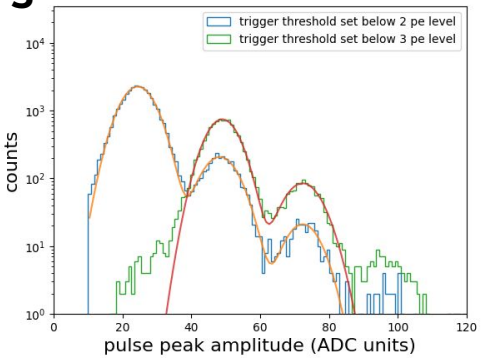

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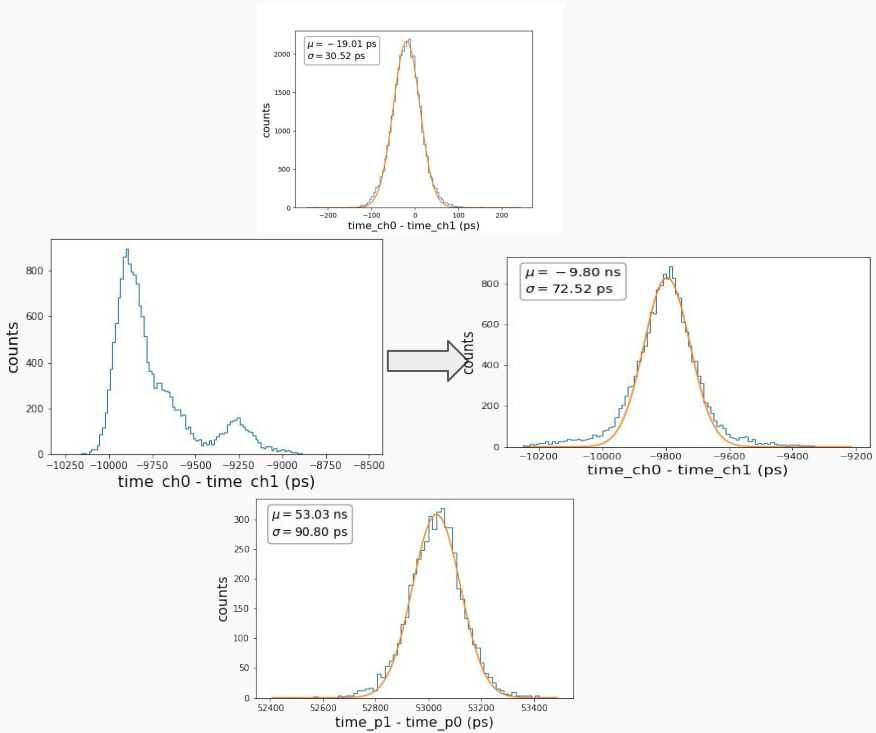
Timing Measurements and calibration

Estimating timing accuracy:

1. Identical Split pulse to two channels: ~30ps

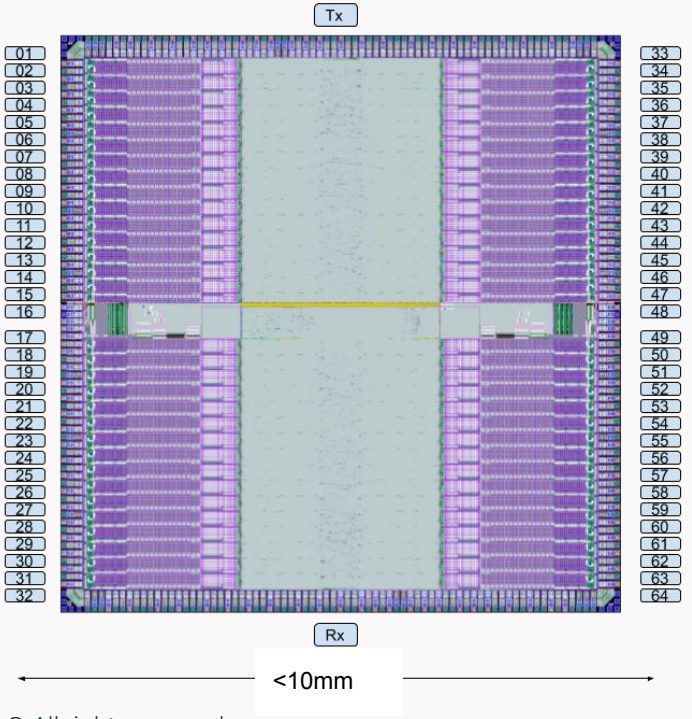
2. Intra-channel accuracy: signal delayed ~10ns: with timing calibration ~ 72ps

3. Inter-channel accuracy with “far” signals and timing calibration ~90ps



HDSoCv2 design

- **HDSoC v2**
  - Design in advanced stages
    - Expected tapeout - early October
  - Main improvements:
    - 64 channel device
    - Proper timing up to 2 GSPS
    - Reduced power consumption/chan
      - DAC reduction
      - Clock gating
    - Improved TIA
    - Improved signal quality:
      - Analog/digital isolation
      - Biasing control (possibly current- based)
    - On chip DSP/FE:
      - Calibrations
      - Feature extraction (calibrated timing/charge)
    - Improved Serial interface



Conclusions and future work

- **HDSoC v1**
  - All channels functional
  - Proper multi-window, multi-channel acquisition, self triggering, output streaming
  - Some issues with noise and power/ TIA BW
  - Boards available for testing for interested parties
- **HDSoC v2**
  - Available for testing by beginning 2023
  - HDSoC v1/2 may be used in beam tests for various EIC sub detectors
- **HDSoC is a novel, low cost, high channel count, high density, streaming readout capable, waveform-sampling ASIC** that can, in the words of our Letter of Support writers, significantly reduce cost, power, mass and volume in the design of readout systems optimized for use in large future detectors such as GEMs for TPCs, and for tracking and particle identification detector systems such as those being developed for EIC and other smaller detectors. The HDSoC is additionally well-suited for incorporation in portable radiation imaging systems such as for e.g. radiological source localization and identification, as well as portable detectors such as compact, high-efficiency neutron scatter cameras for non-proliferation and other national security missions.

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Any Questions?

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Tues., August 23 2022 11:05 am EDT