SC0020461

CMOS Integrated With Float Zone Pixel Sensor

Topic No: 32.c – Next Generation Pixel Sensors

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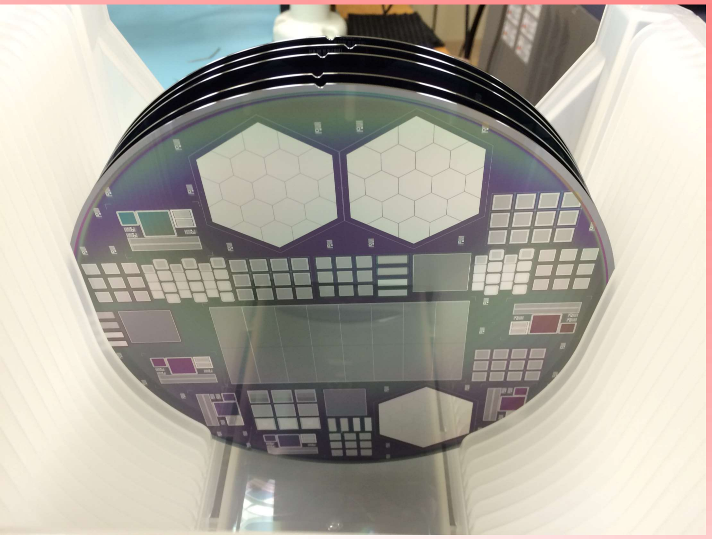
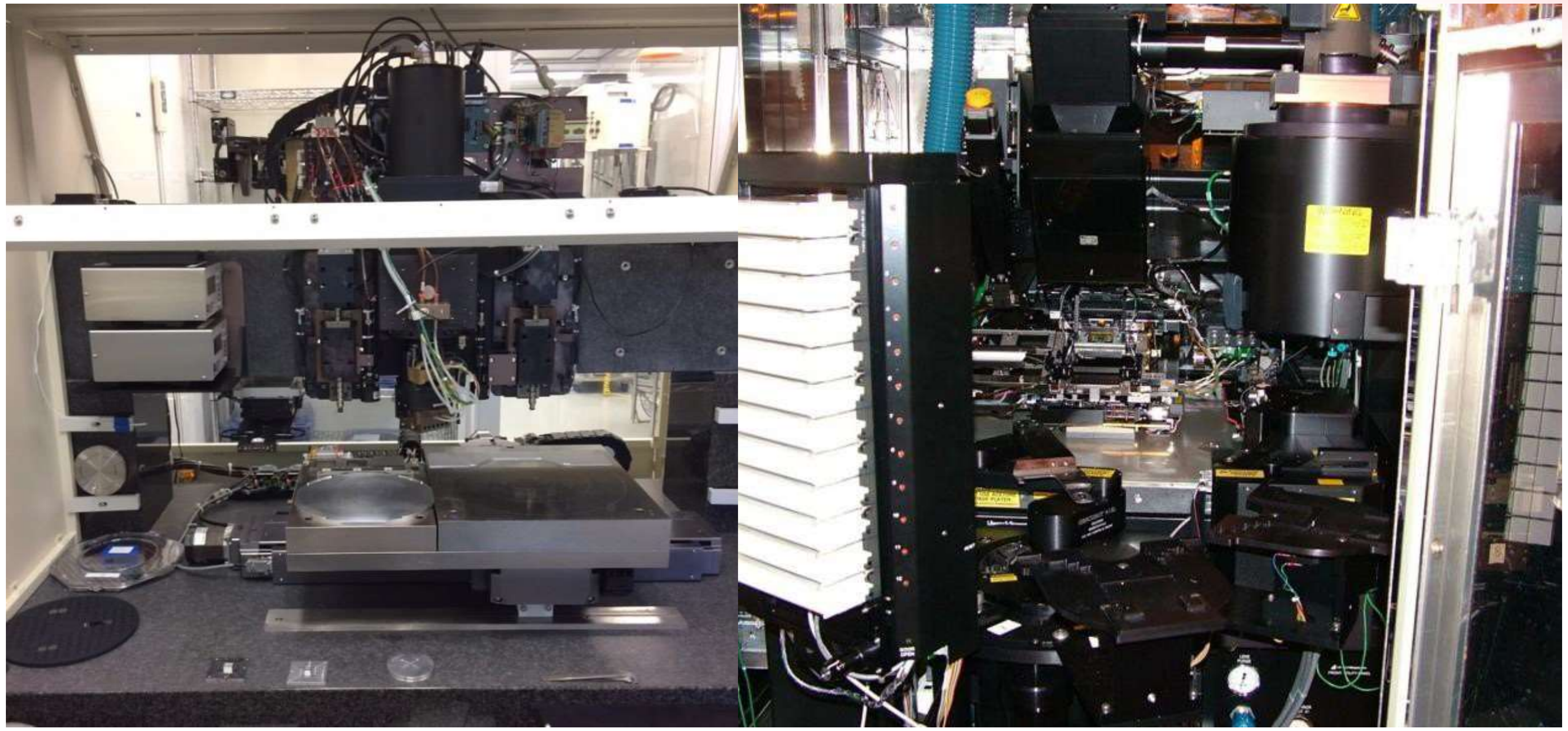
NHanced Semiconductors



- Batavia, IL: Design and Test
  - – Complete front end and backend design down to 12nm
  - – Supports AI and HPC systems development
- Morrisville, NC: Foundry
  - – 3”-200mm
  - – Copper, Al, Ni BEoL
  - – Interposers
  - – 2.5/3D Integration



Background: Next Generation Pixel Sensor

NP has a growing need to develop particle tracking devices with:

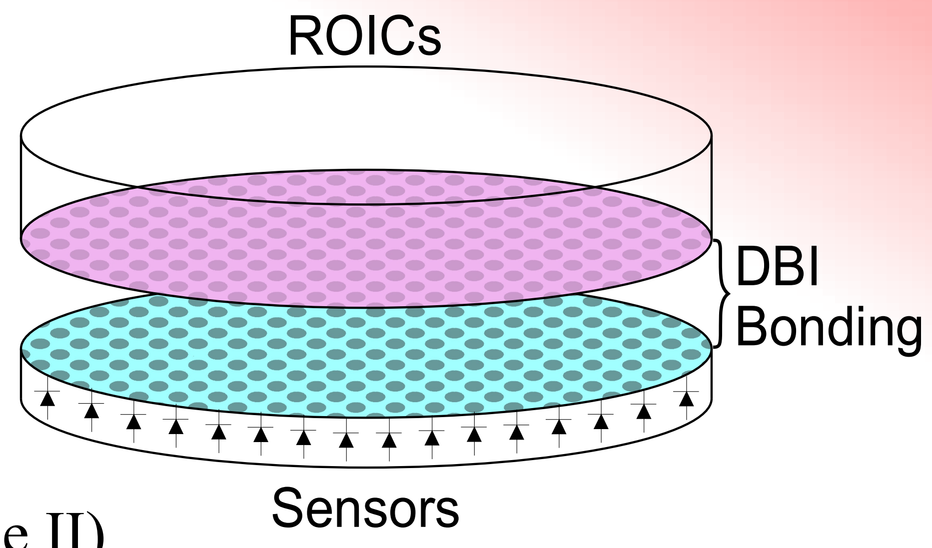
1. Improved position and timing resolution for more accurate tracking
2. Faster speed to limit event pileup
3. Lower mass sensor to minimize electron scattering, leakage (increased shot noise) and trapping distance (decreased signal)
4. High radiation tolerance to survive the conditions of high luminosity colliders
5. Lower power and lower fabrication cost

Background: Technology Overview

Technologies	Pros	Cons
Monolithic Active Pixel Sensors (MAPS)	Simple and cheap	• The sensor device can't be fully depleted • Can't use high resistivity material • Lower granularity
SOI-MAPS	• ROIC and sensor separation • High granularity • Fast	• Expensive process • Back diode effect • Sensitive to TID
LGAD	• Complete separation of ROIC and sensor • picosecond timing resolution (only limited to Laudau noise) • Lower power	• Low fill factor • Low granularity • Gain sensitive to radiation
3D Advanced Hybrid Detector (3D-AHD)	• Complete separation of ROIC and sensor • High granularity • High fill factor • Could achieve picosecond timing resolution	• Higher power than LGAD • Need to be demonstrated

NHANCED SEMICONDUCTORS

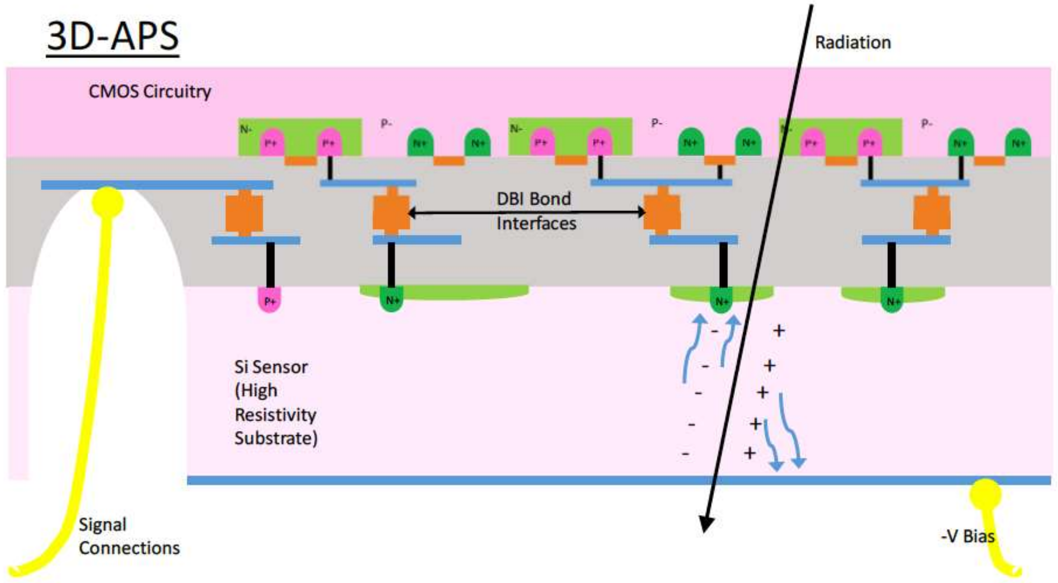
Background: Plan for 3D-AHD development



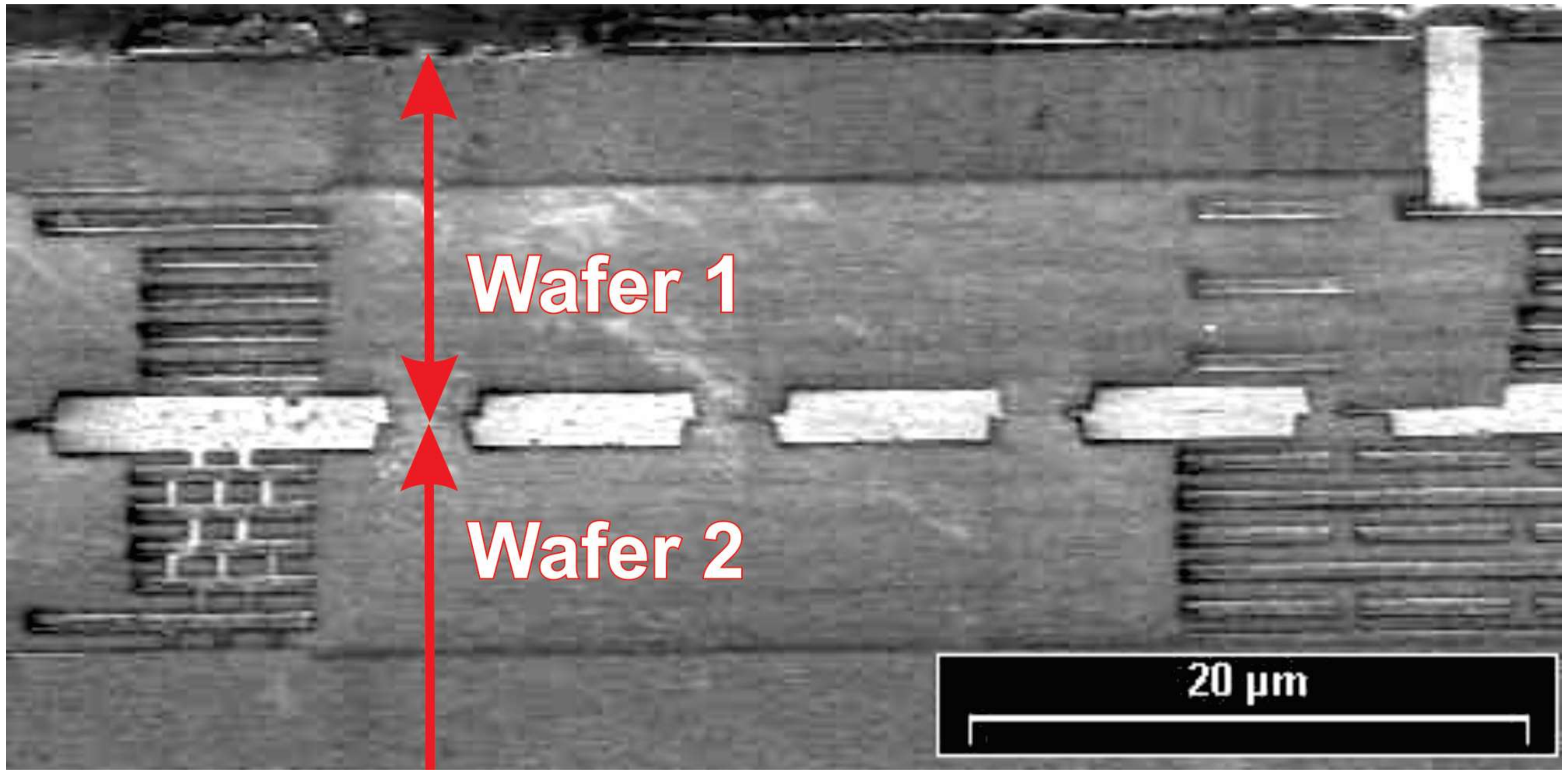
Sensor tier:
Physical implementation (Phase I)
Fabricated at NHanced on high resistivity silicon wafer (Phase II).
Thinned down to 100um to 20um at NHanced (Phase II).

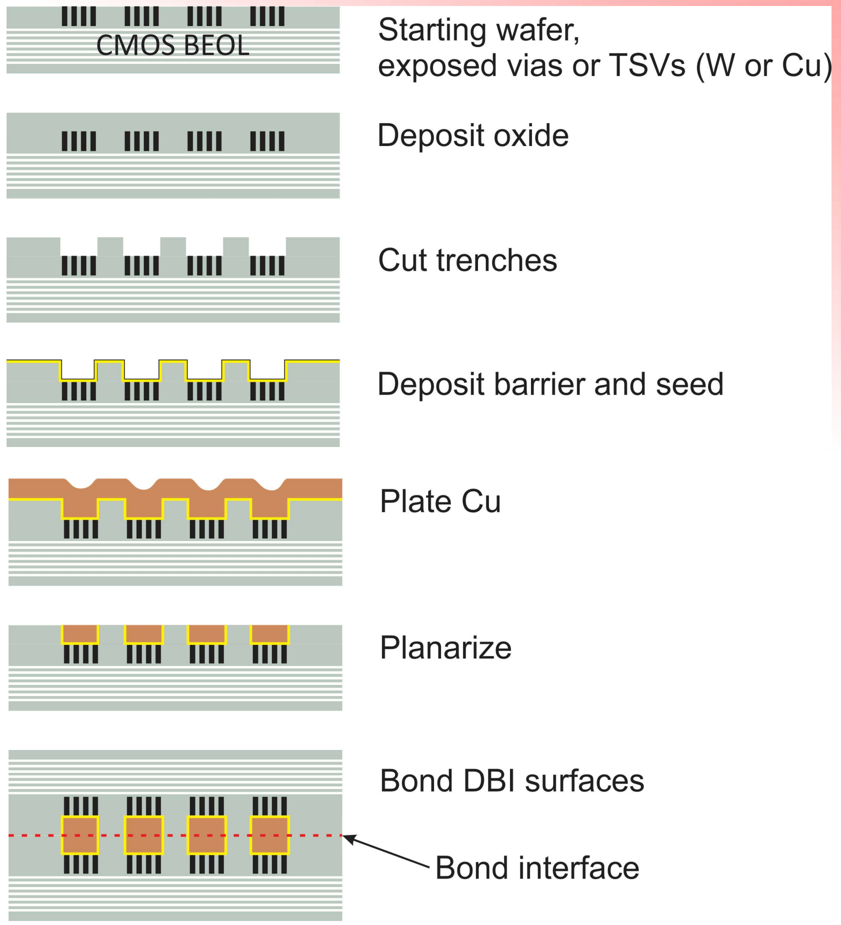
ROIC tier:
Proof of concept and designed by NHanced and Fermilab (Phase I and Phase II)
Physical implementation (Phase II)
Fabricated with RHBD (Phase II)

3D-AHD detector:
Final integration at NHanced fab (Phase II)



Bonding Technology





Starting wafer,
exposed vias or TSVs (W or Cu)

Deposit oxide

Cut trenches

Deposit barrier and seed

Plate Cu

Planarize

Bond DBI surfaces

Bond interface

Some Basics – Time Resolution

3D allows for small pixels with small associated load capacitance. Small pixels with ~25x smaller capacitance should have similar timing performance to LGADs.

Jitter

$$\sigma_t \sim \sigma_{noise}\left(\frac{\partial V}{\partial t}\right) \sim t_r\left(\frac{Noise}{Signal}\right)$$

Front end noise

$$\sigma_n^2 = \frac{C_L^2(4ktA)}{g_m t_a}$$

Time resolution

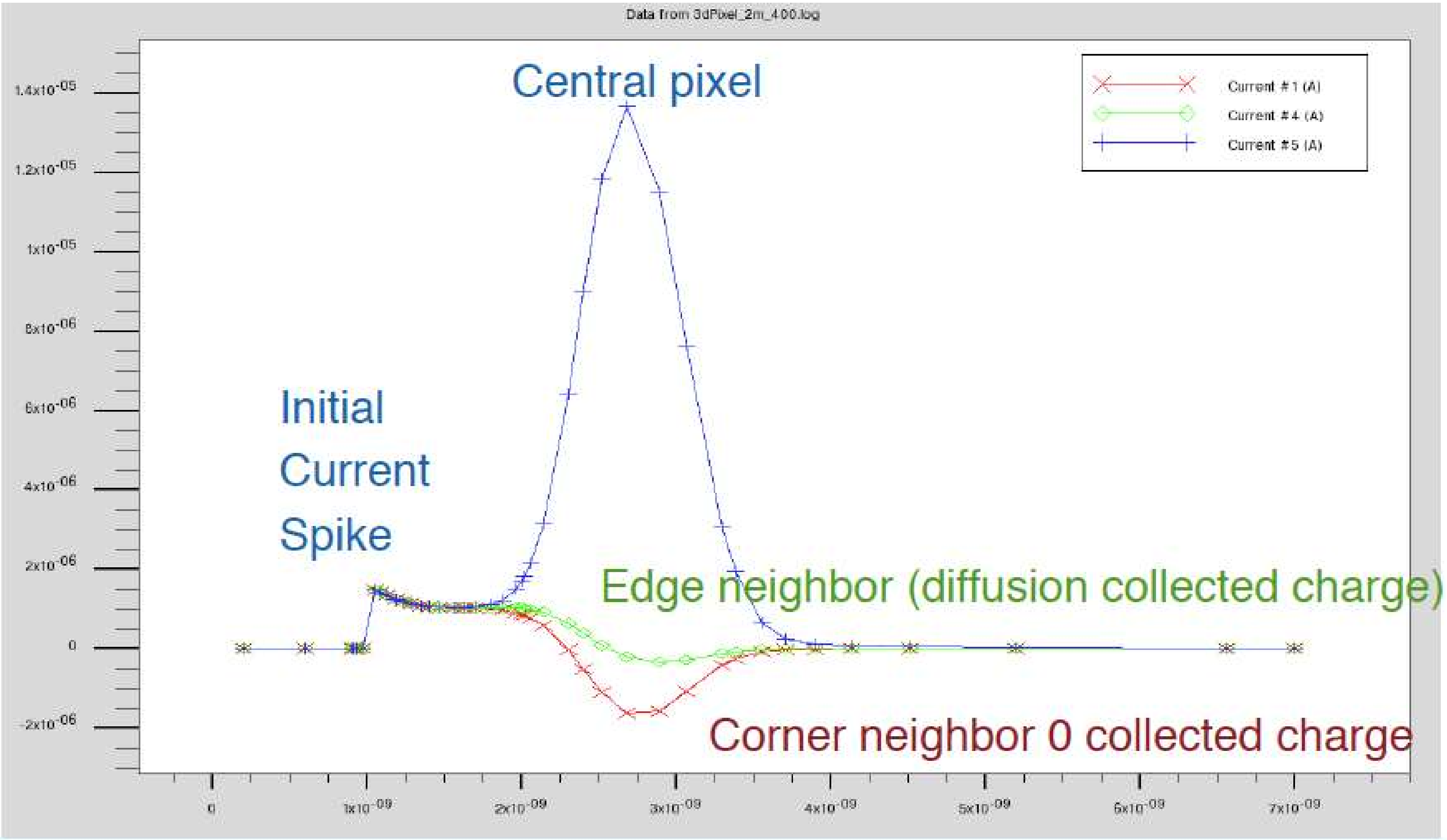
$$\sigma_t \sim \frac{C_L}{\sqrt{g_m t_a}}\frac{\sqrt{t_a^2 + t_d^2}}{Signal}$$

Fast timing -> large S/N, fast amplifier and small load capacitance

Pixel size: 25x25um
Towersemi 130nm process was selected

Induced current – Simple example – X-rays

The current pulse reflects charge motion deep in the detector



Central pixel

Initial Current Spike

Edge neighbor (diffusion collected charge)

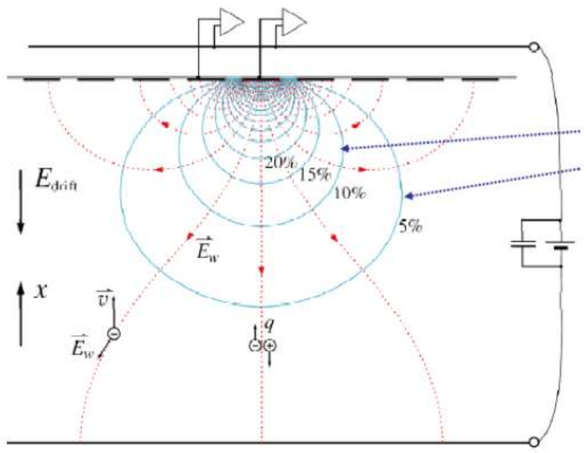
Corner neighbor 0 collected charge

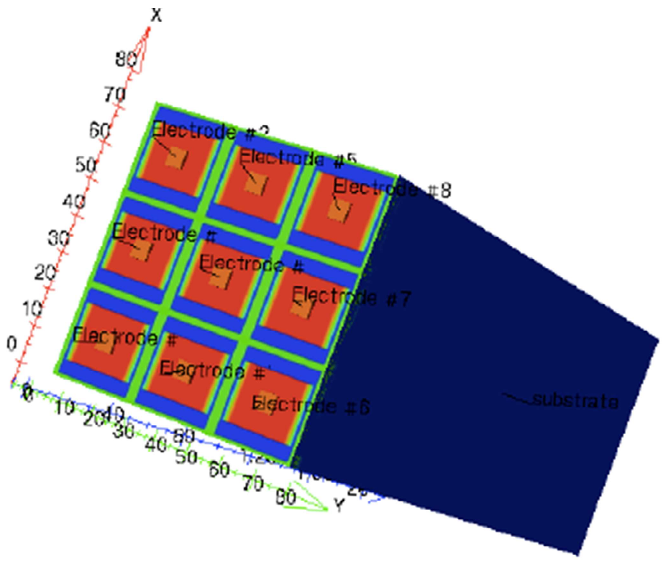
Ramo's theorem

$$i = -q\vec{E}_w \times \vec{v}$$

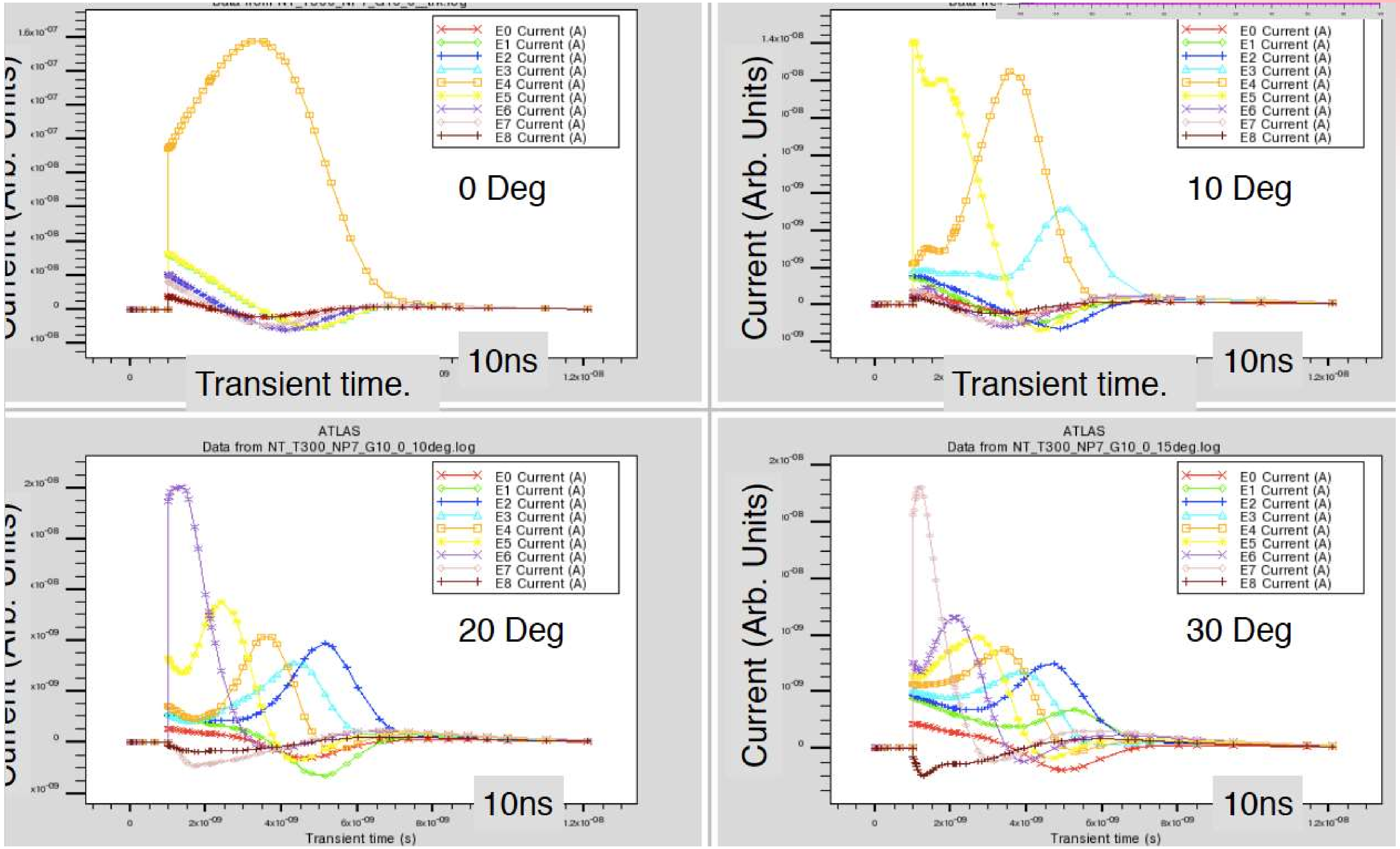
$$Q_s = \int i\,dt = q\int \vec{E}_w d\vec{x}$$

$$Q_{1\to 2} = q(V_{w2} - V_{w1})$$





Induced current - MIPs at various angles:

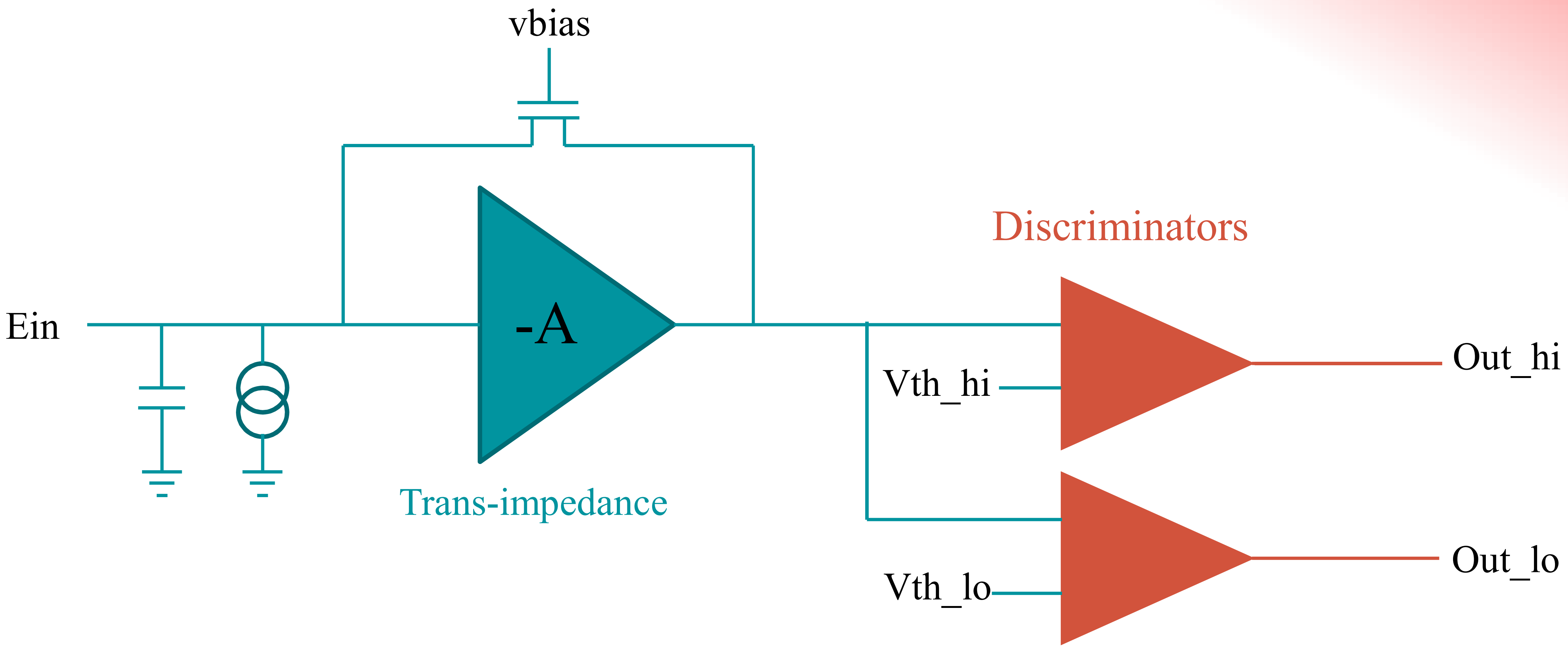


Ron Lipton
FermiLab

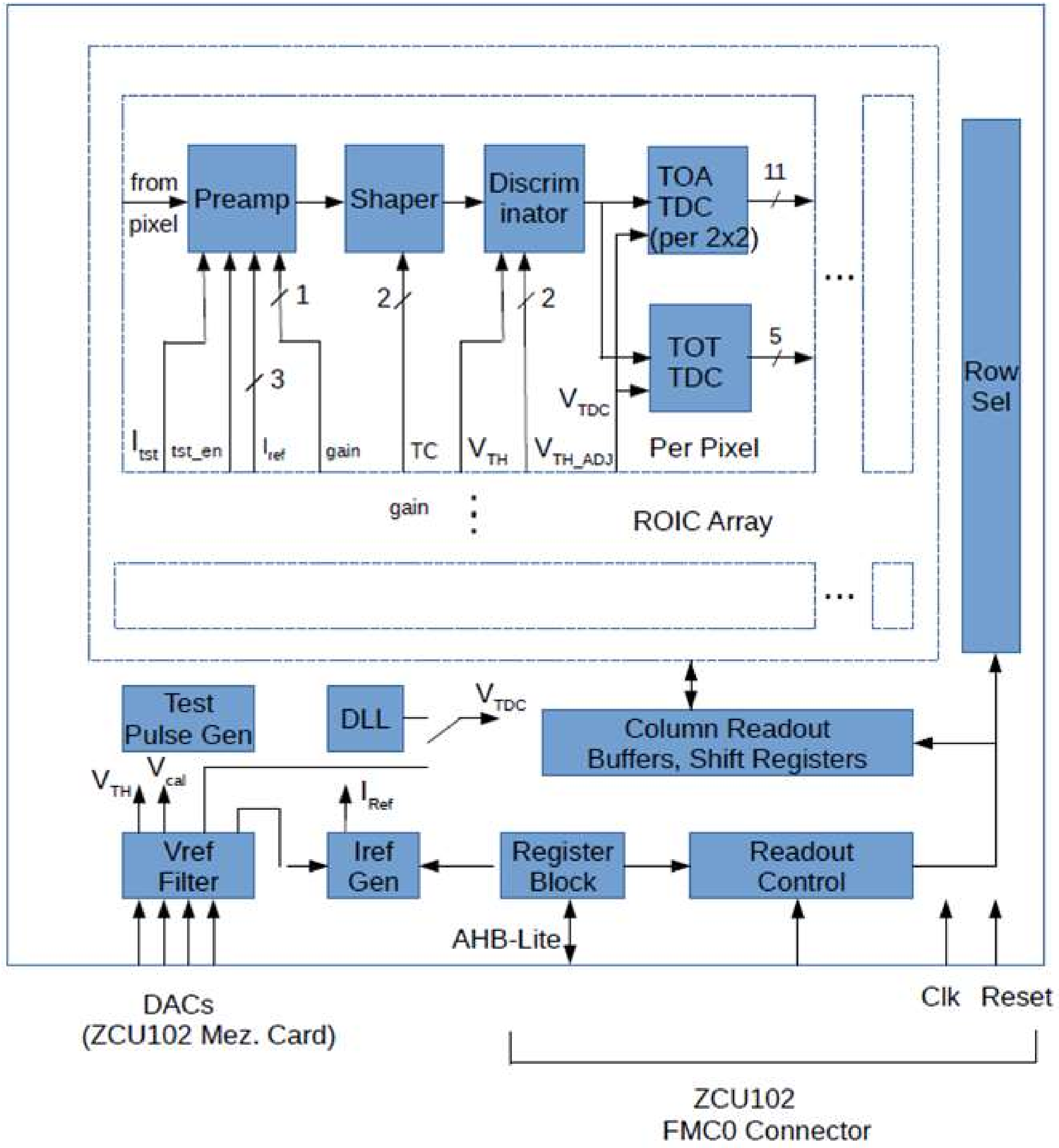
Proof of concept of Angular Resolution possibility

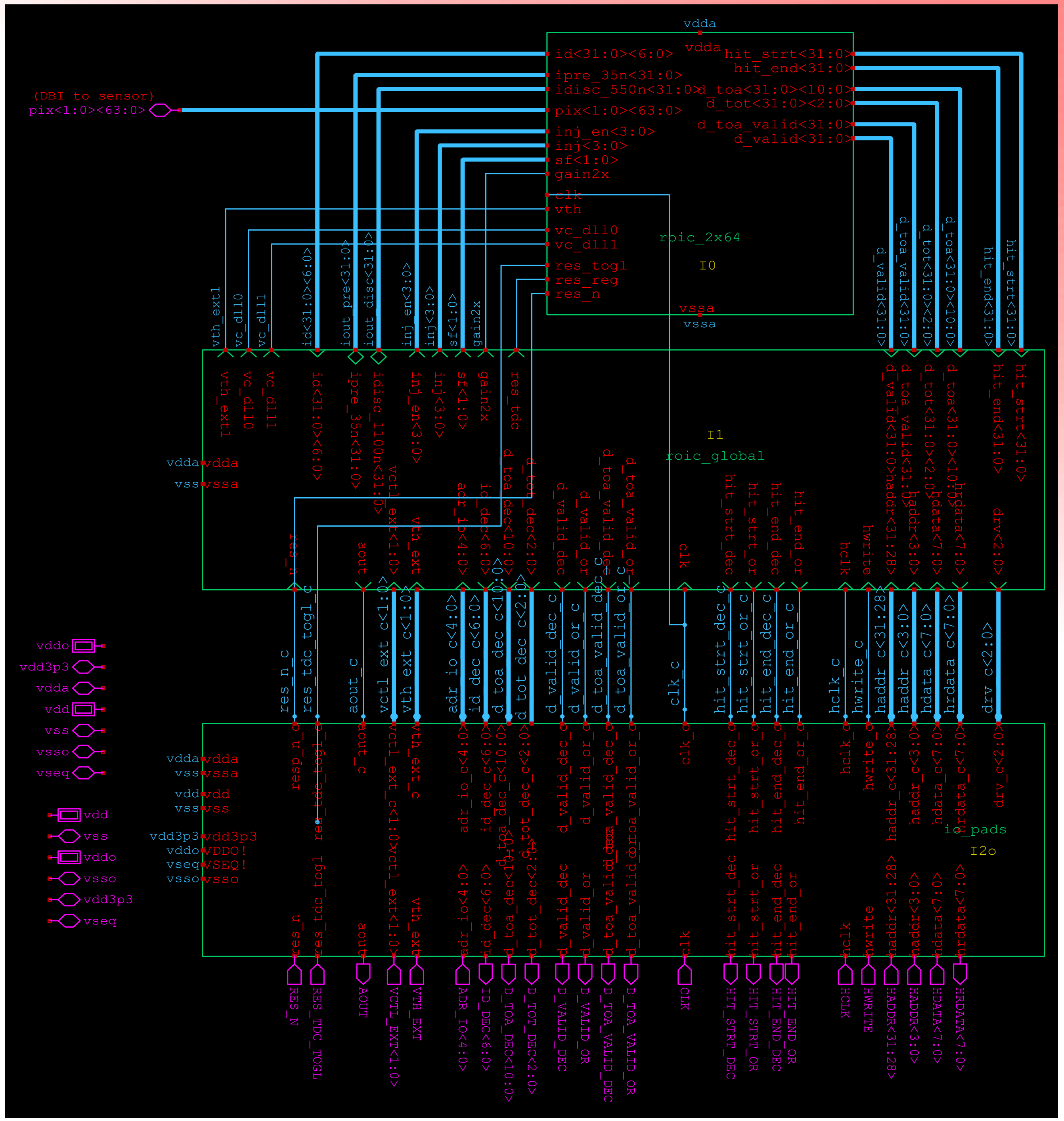
- We found angular resolution is possible for high enough pixel area/thickness ratio
  - -> Increasing the pixel size specification to 25um x 200um (smaller size along the axis perpendicular to the field).
  - -> Increasing the thickness of our simulated substrate to 200um to maintain good S/N ratio for every electrodes and angles.
- Angular resolution is only possible if we maintain the integrity of the shape of the current pulse. This concept is fundamentally enabled by the new trans-impedance amplifier as opposed to the more typical Charge Sensitive Amplifier (CSA) scheme.
  - -> Requires a more complicated front end design (stability, speed, noise)
  - -> Allows to process two consecutive pulses in a row
- Angular resolution will require a more sophisticated data processing scheme and perhaps an AI approach might work well

Front-End Analog Simplified Scheme

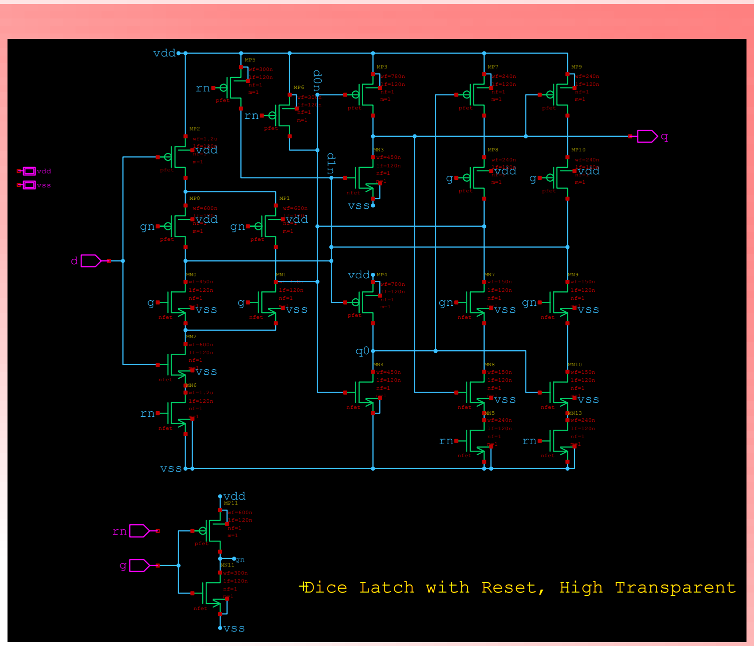


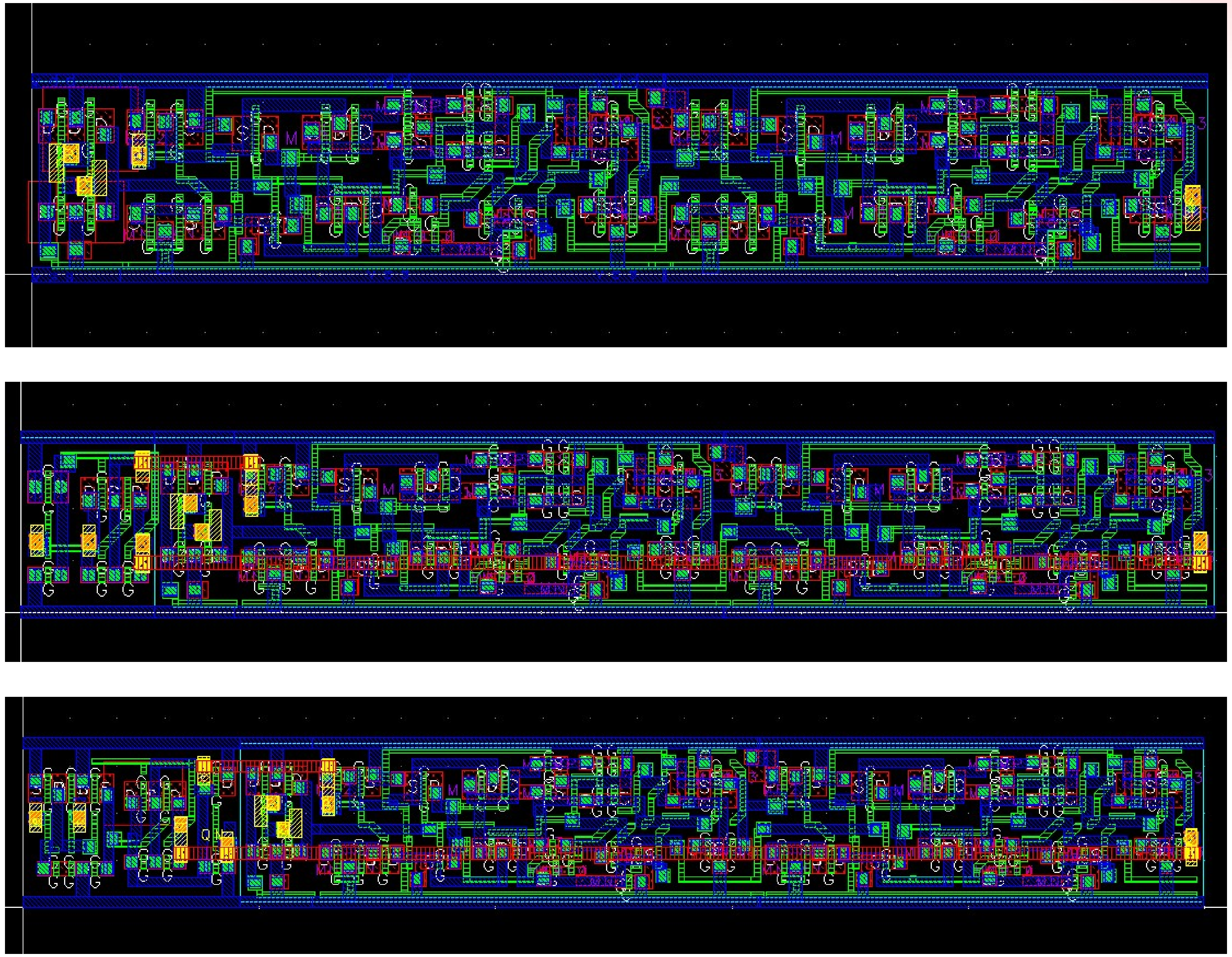
Top Level Design



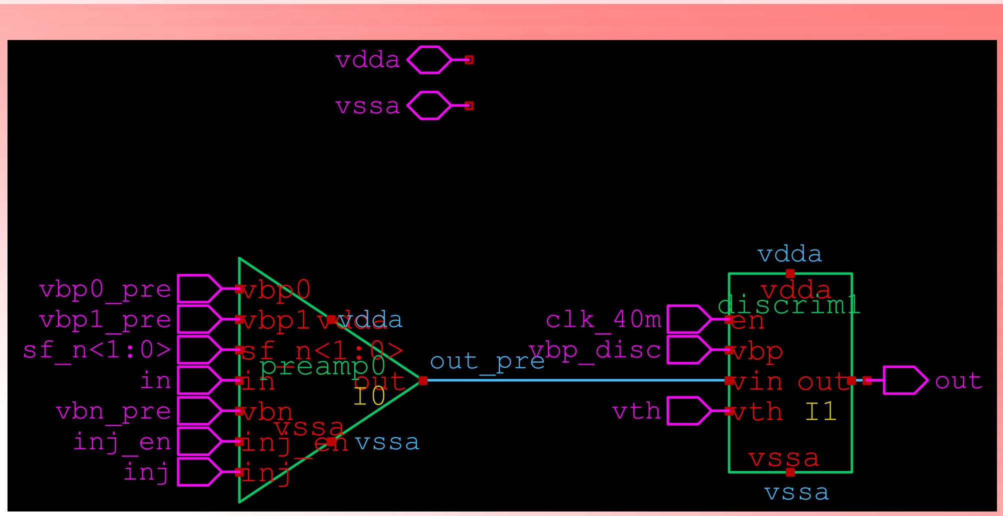


RHBD Dice Registers

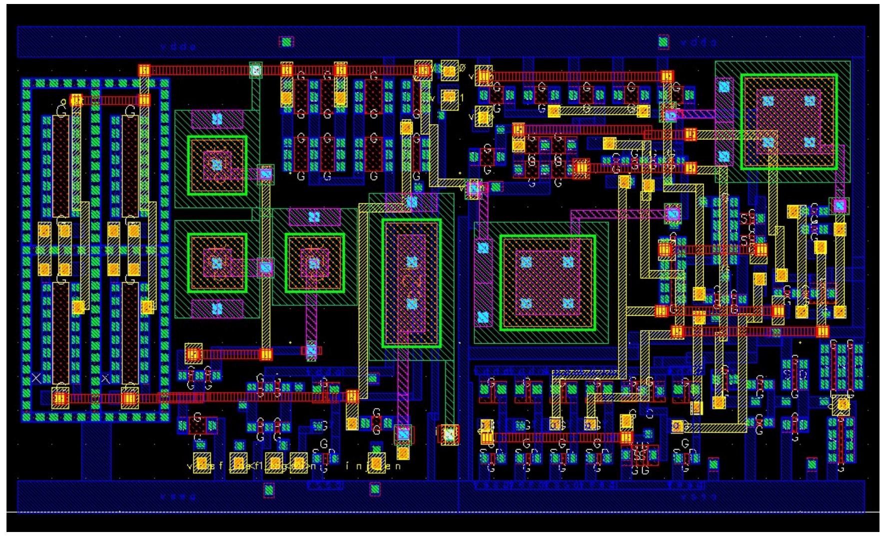




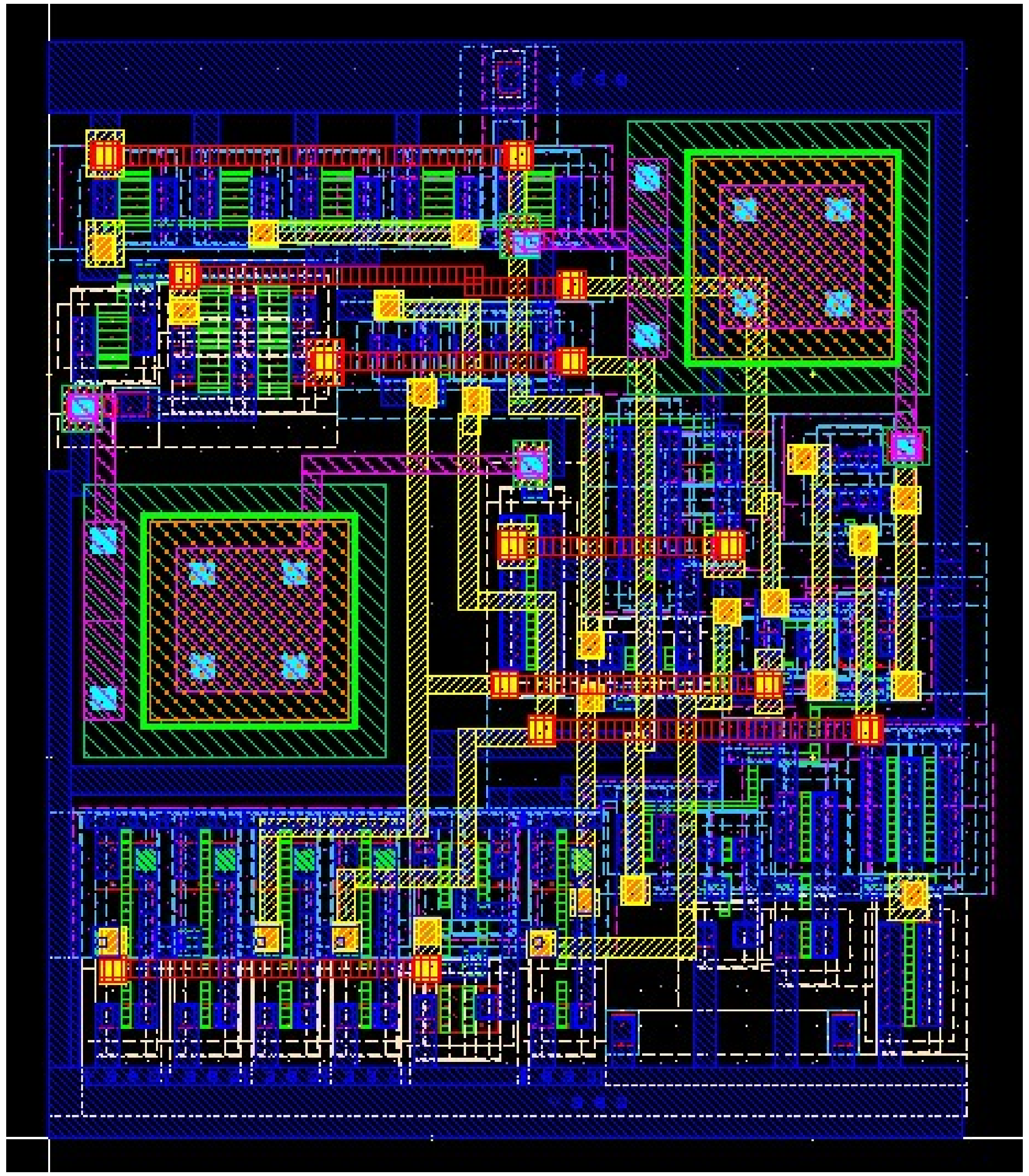
New HP Analog Designs



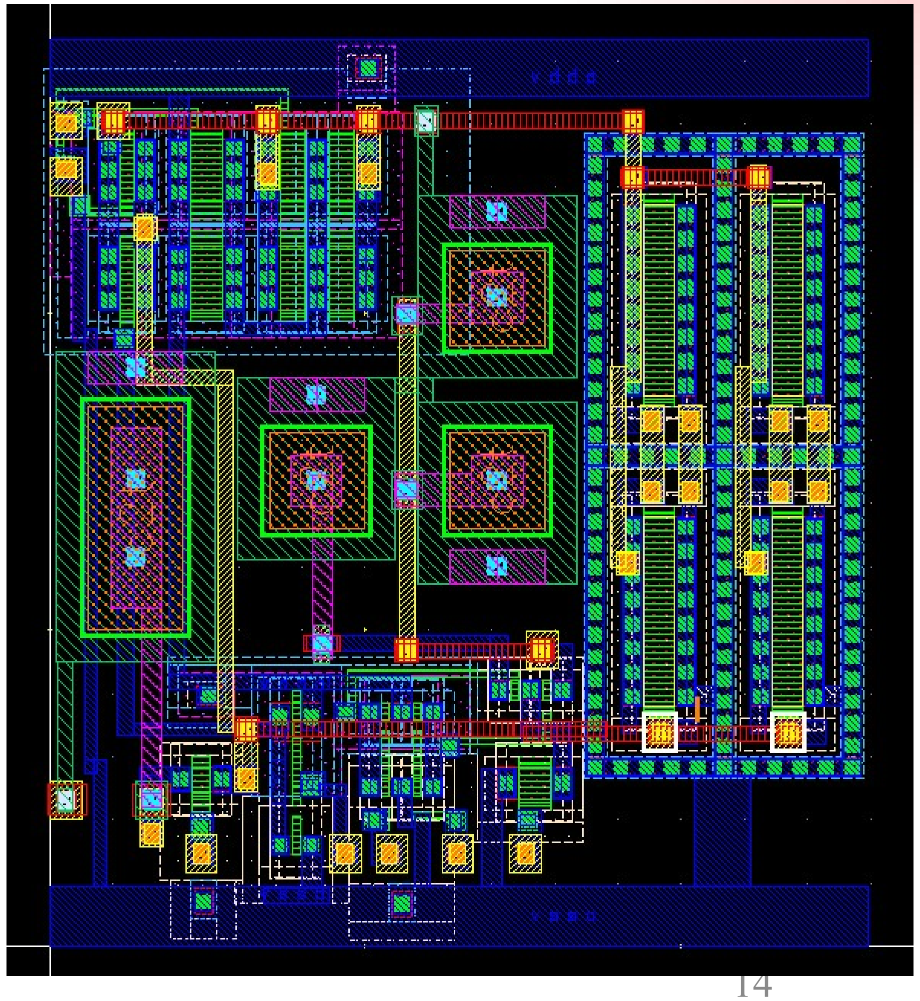
Front-End



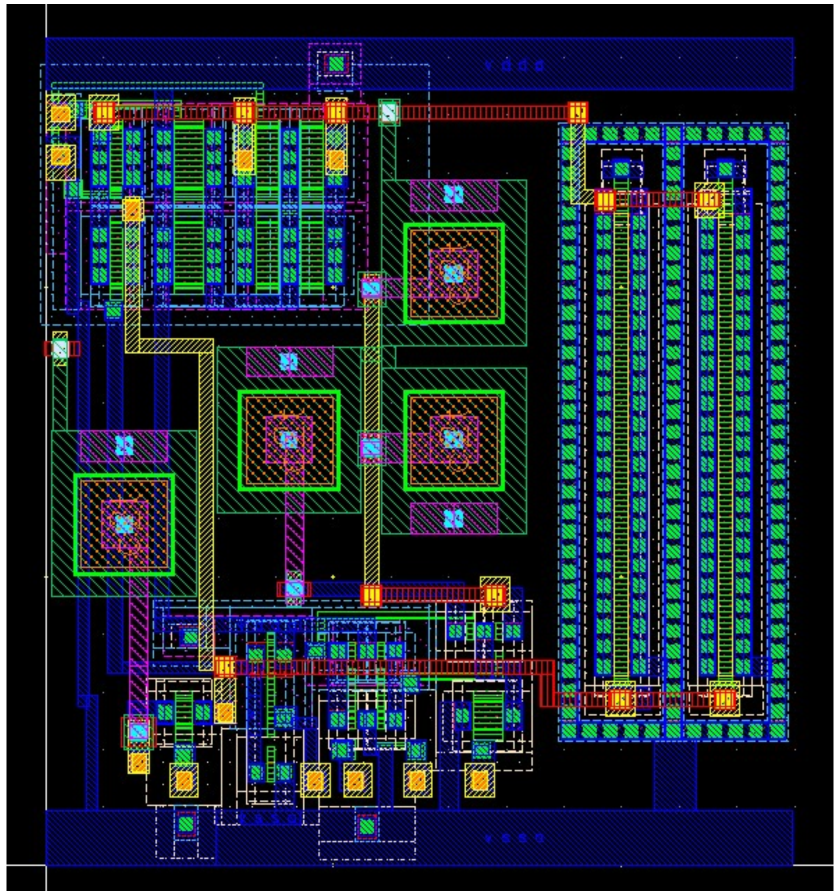
Discriminator



Preamp1

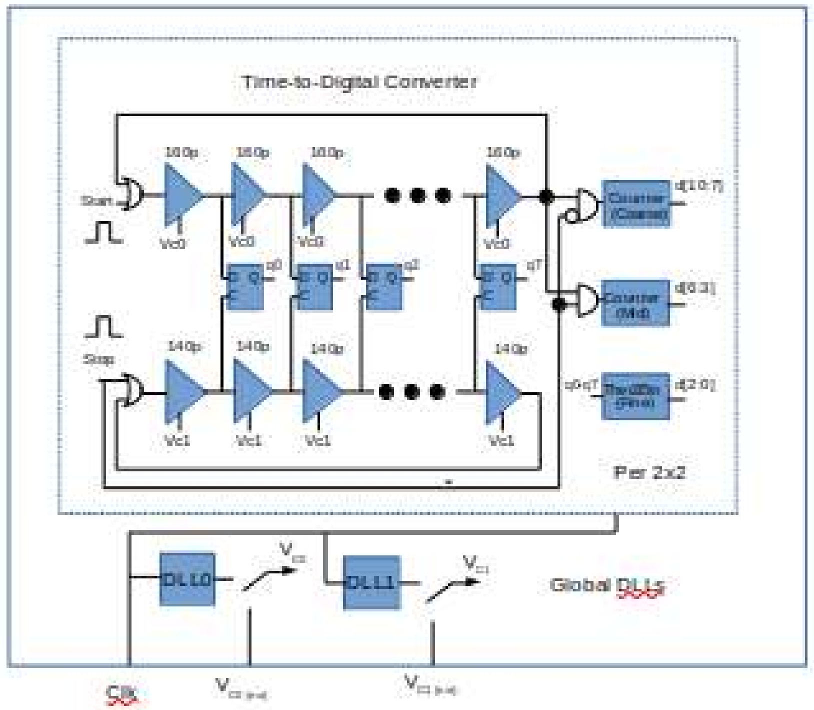


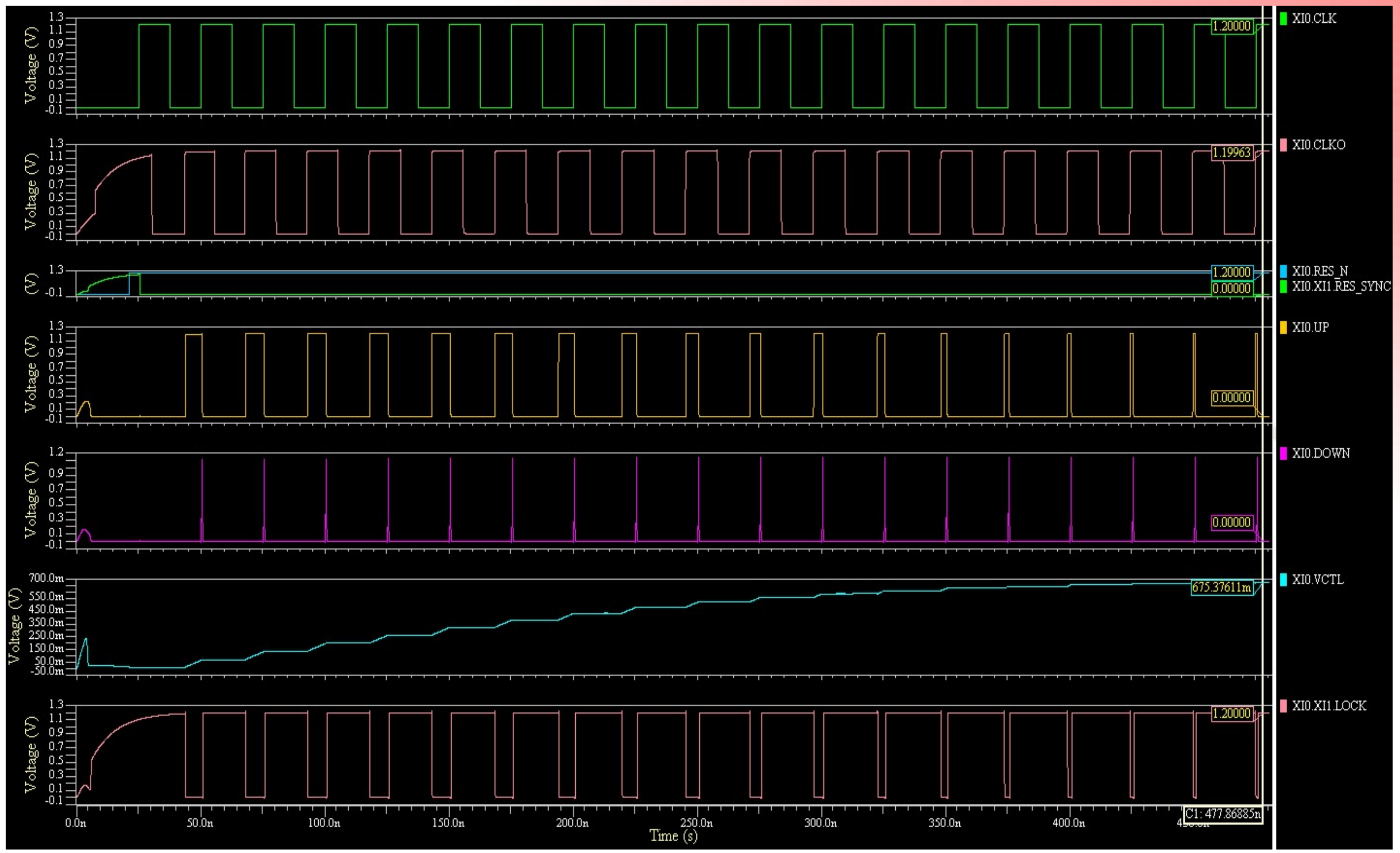
Preamp0



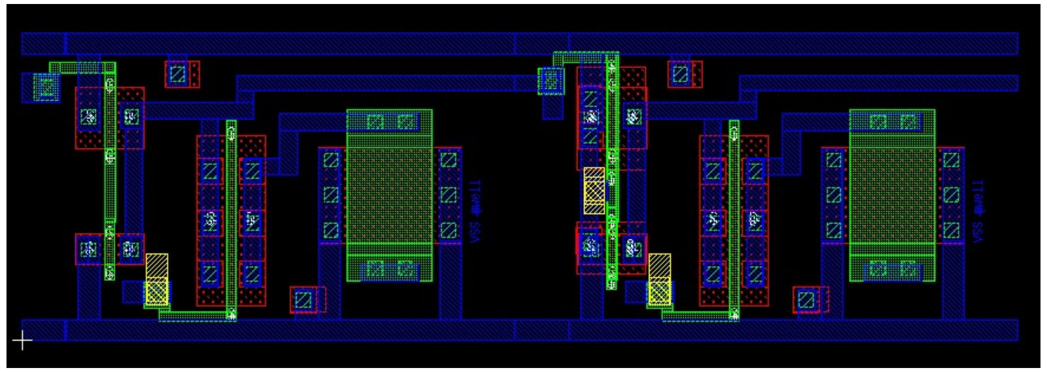
NHANCED SEMICONDUCTORS

DLL Chains: Core of LP Picosecond Resolution

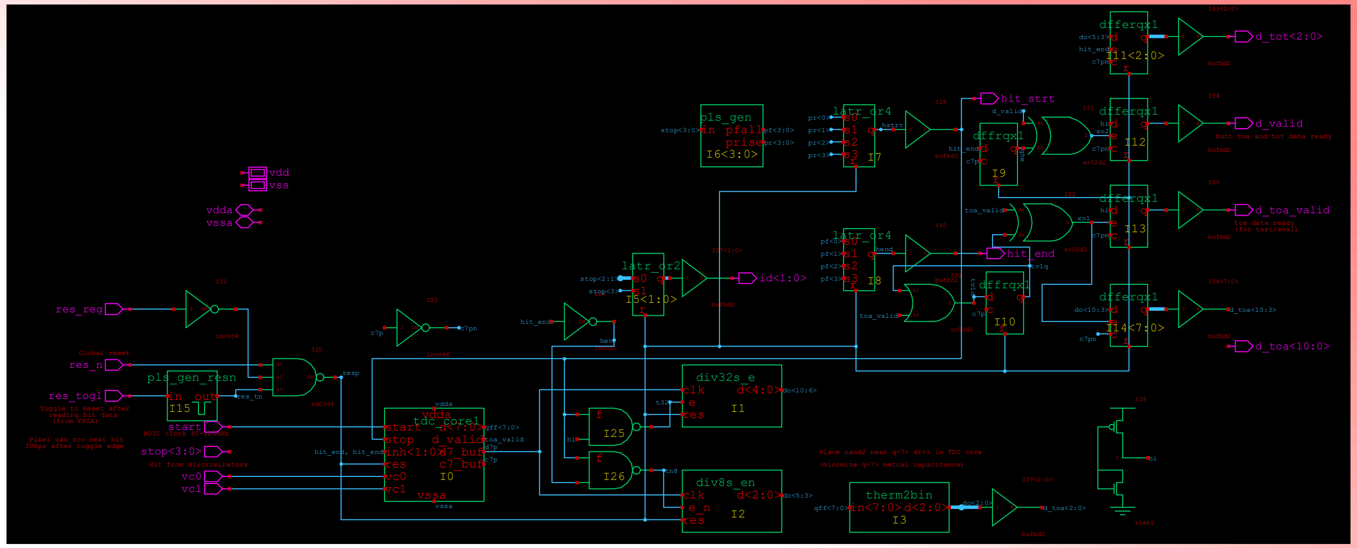




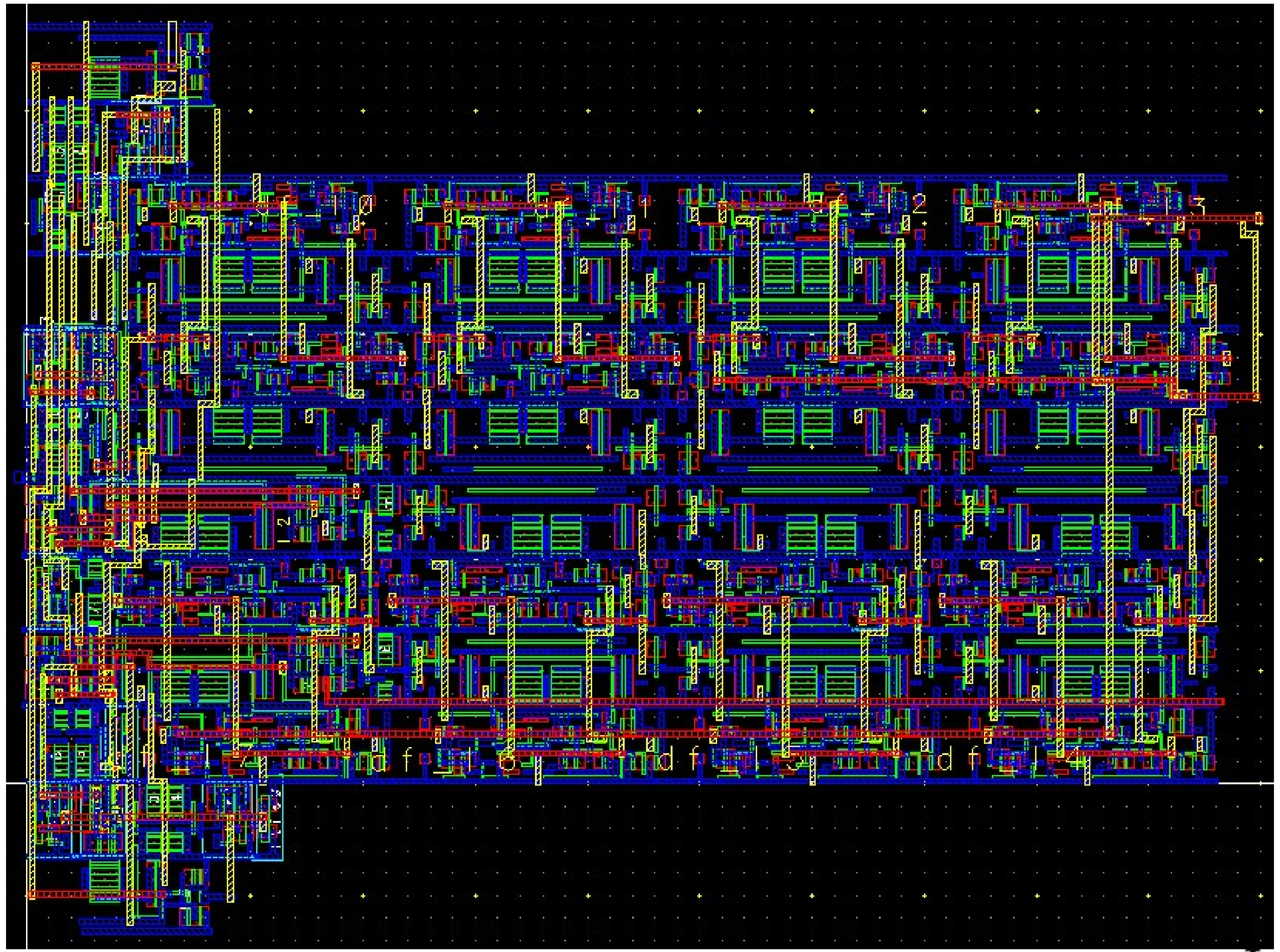
Time to Digital Converter (TDC)



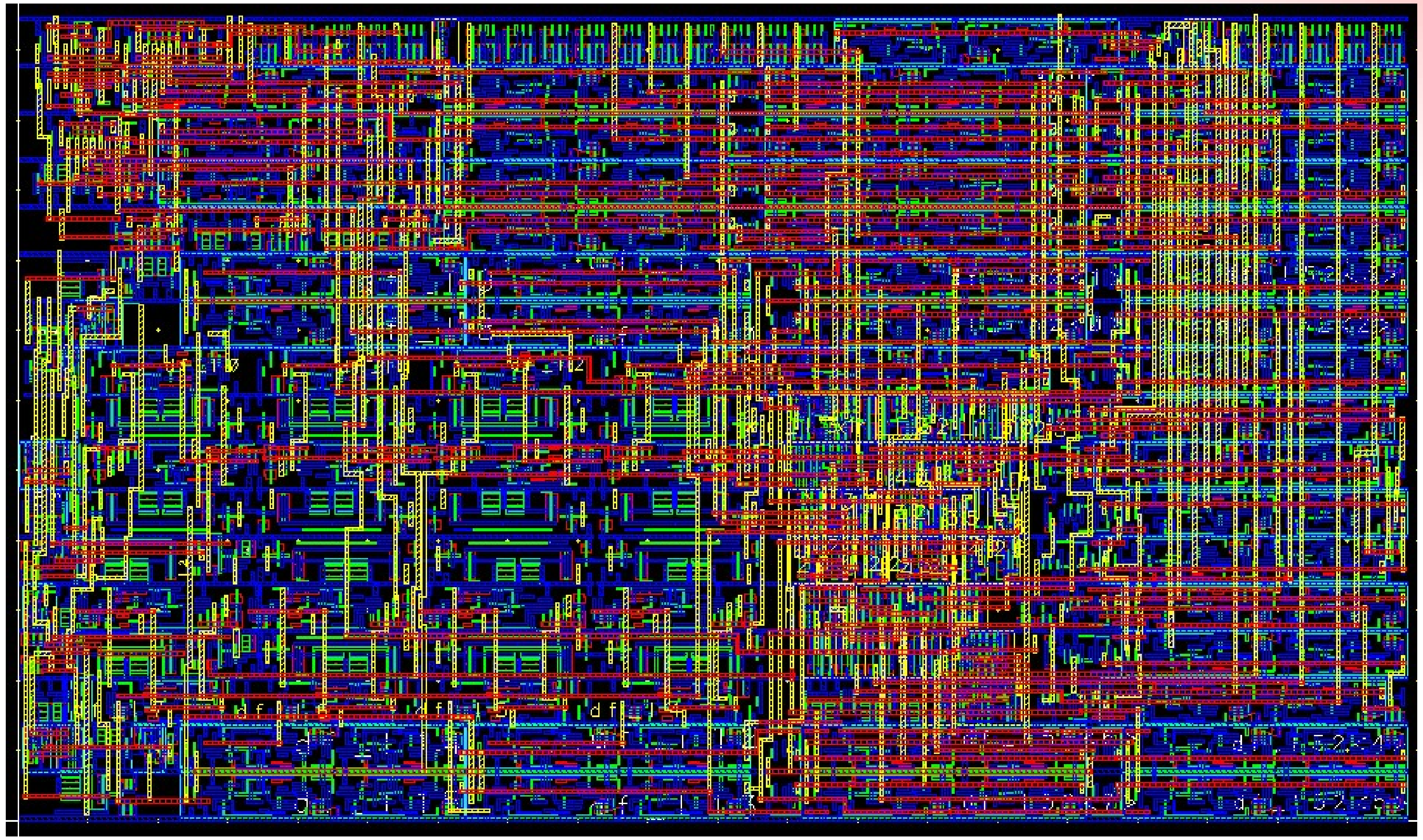
Delay Element



TDC Inner Core

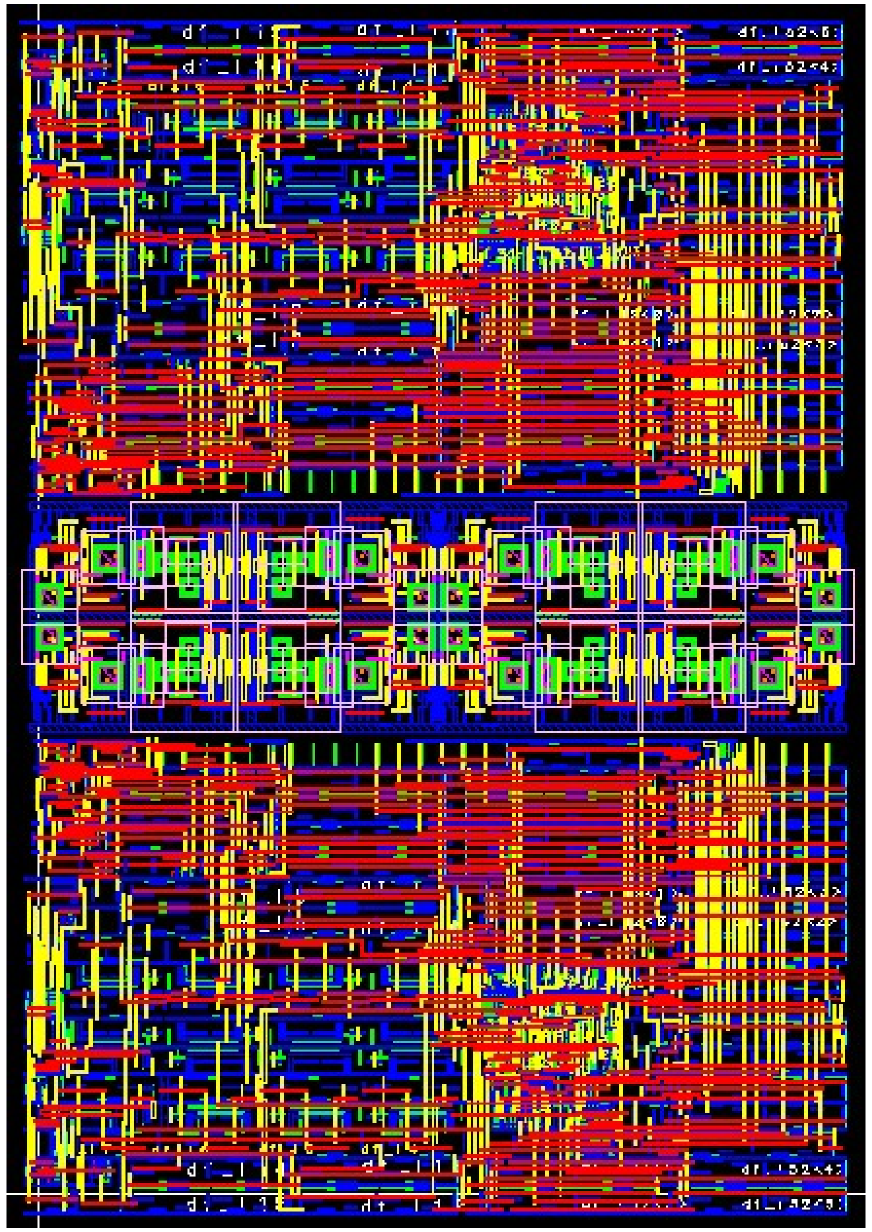


TDC Top Level

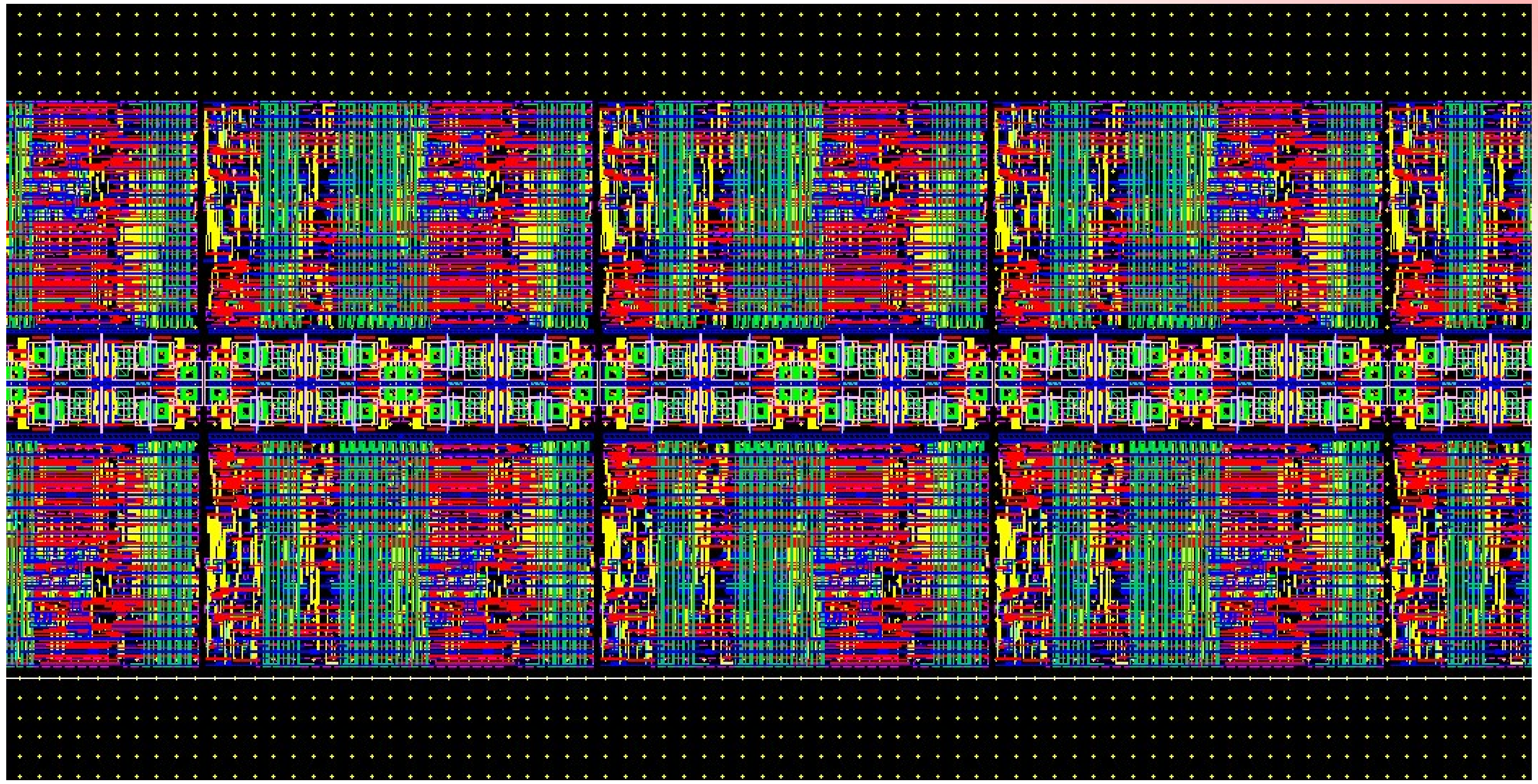


Top Level ROIC Design

2x4 ROIC Pixel Group



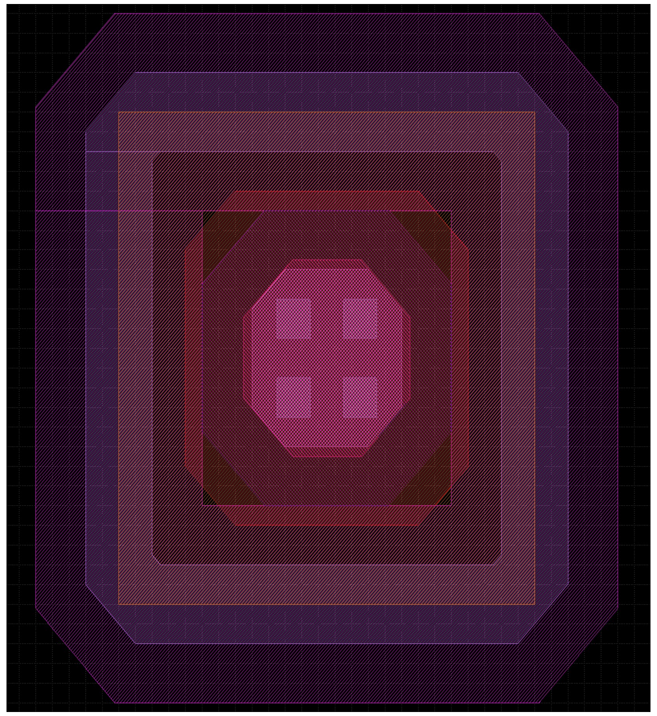
2x64 ROIC Pixel Group



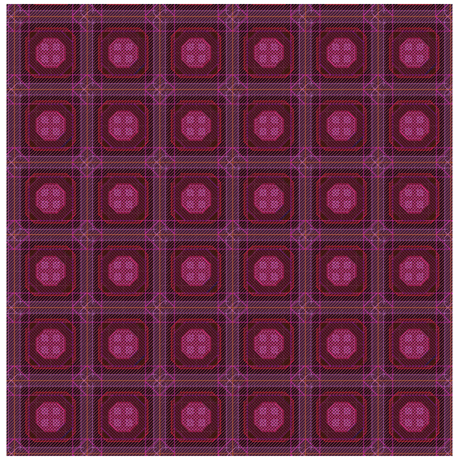
NHANCED SEMICONDUCTORS

The Detector

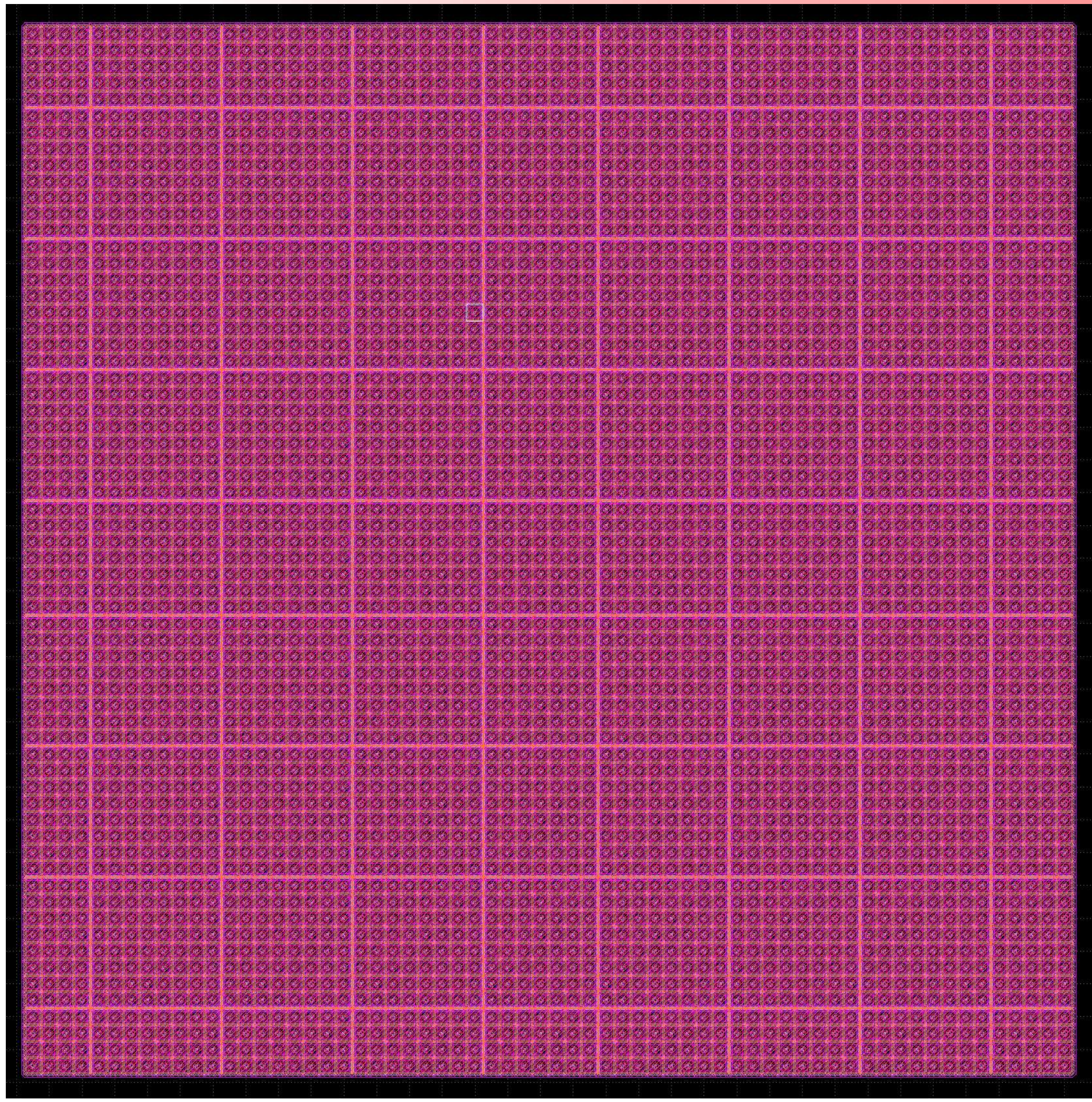
Detector Pixel (25x25um)



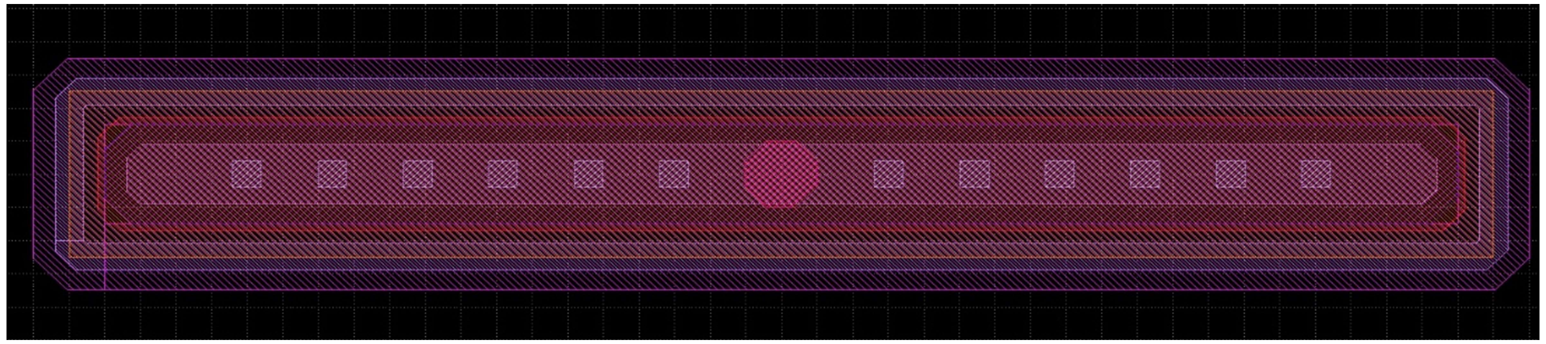
Detector Pixel Group



Detector Pixel Array



Detector Strip (25x200um)



Challenges

- PI Change
- COVID delays
  - Internal
  - Supply chain
- Tool and PDK deficiencies
- Significant cost increases
  - Tool set change over

Recent Direct and Indirect Breakthroughs

- Single Layer Directionality
- New ultra-thin temporary bonding
  - Good to >400C processing
  - Extremely planar
- Microwave annealing
- RHBD Tower 130nm Library Development

Conclusion/Status

- Design/Layout implementation of detector completed
- Design/Layout of the ROIC is >85% completed
  - Schematic designs and simulations completed
  - Fab start in 4Q22
- Detector fab started
- Concerns:
  - Costs
  - Schedule

New Manufacturing Capabilities