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DE-SC0020500
Digital Data Acquisition with High Resolution and Linearity

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Outline

- The company and its capabilities.
  - Customers.
- The ADC Nonlinearity problem.
- Nonlinearity example from Majorana Demonstrator.
- Demonstration of the Differential Nonlinearity (DNL) with our own DDC-10.
- Dedicated boards for measuring the ADC nonlinearity *in situ*.
- The nonlinearity measured with the dedicated board.
- The nonlinearity correction.
- Summary and conclusion.
- Future plans.
- Acknowledgements.

The company and its capabilities

- The team: three physicists / engineers, a senior software engineer, and a manager. We regularly work with a local Electrical Engineering consultant.
- We worked with several interns listed on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, astrophysics, etc.

Our capabilities: Development of cutting edge instruments.

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, especially Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in FPGAs (VHDL, Verilog) and in embedded processors (Pascal, Python, C).
- Processing data from nuclear detectors of any kind.
- Development of simple detector assemblies using scintillators, PMTs, or SiPMs.

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Our customers

University of Rochester

Houghton College

The University of Tennessee Knoxville

SFU Simon Fraser University Engaging the World

Université Laval

Augustana University

上海交通大學 Shanghai Jiao Tong University

Los Alamos National Laboratory

Fermilab

Brookhaven National Laboratory

NSCL **National Superconducting Cyclotron Laboratory**

Albert Einstein Center for Fundamental Physics

Universität Bern

Brown **Brown University**

Wiener Plein & Baus, Corp. Worldwide Industrial-electronic Nuclear-electronic Ressources

Nonlinear Response of the Pipelined ADC

The Problem:

- Pipelined ADC architecture causes semi-periodic nonlinearities due to imperfect matching of the ADC stages.
- Nonlinearity is impacting resolution in high precision measurements
- Example was described in the Majorana Demonstrator paper.

N. Abgrall, et al, *ADC Nonlinearity Correction for the MAJORANA DEMONSTRATOR*

https://arxiv.org/pdf/2003.04128.pdf

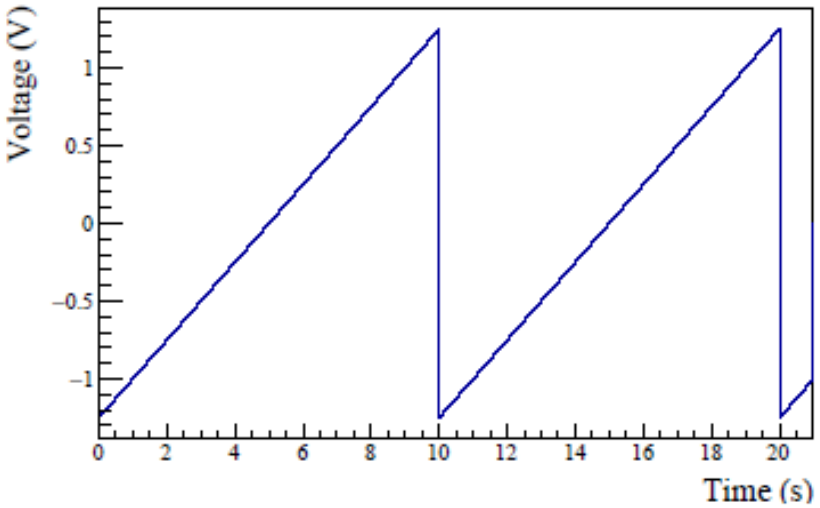
Majorana Demonstrator DNL / INL Measurement

It was quite demanding…

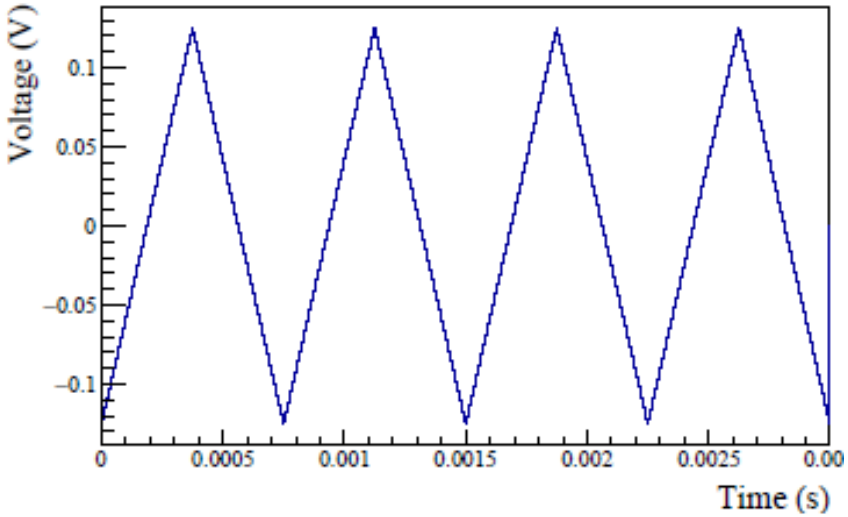
- The authors disconnected detector signals and connected two ramp generators to complementary inputs of the ADC. The nonlinearity was measured by swiping the voltages over the ADC range.

1. The method required disconnecting the signal cables and connecting the test cables.
2. It cannot be done with detectors connected to the digitizer inputs *in situ*.
3. The procedure required a lot of manual work and effort.
4. The method requires a differential input. GRETINA digitizers provide such inputs, but this is not common.

Slow analog ramp applied to one ADC input.



Fast analog ramp applied to the other ADC input.



Nonlinearities in Majorana Demonstrator Analysis

Nonlinearities of the GRETINA digitizer (AD6645) reported by Majorana Demonstrator.

N. Abgrall, et al, ADC Nonlinearity Correction for the MAJORANA DEMONSTRATOR

https://arxiv.org/pdf/2003.04128.pdf

Figure 3
DNL measured with slow analog ramp.

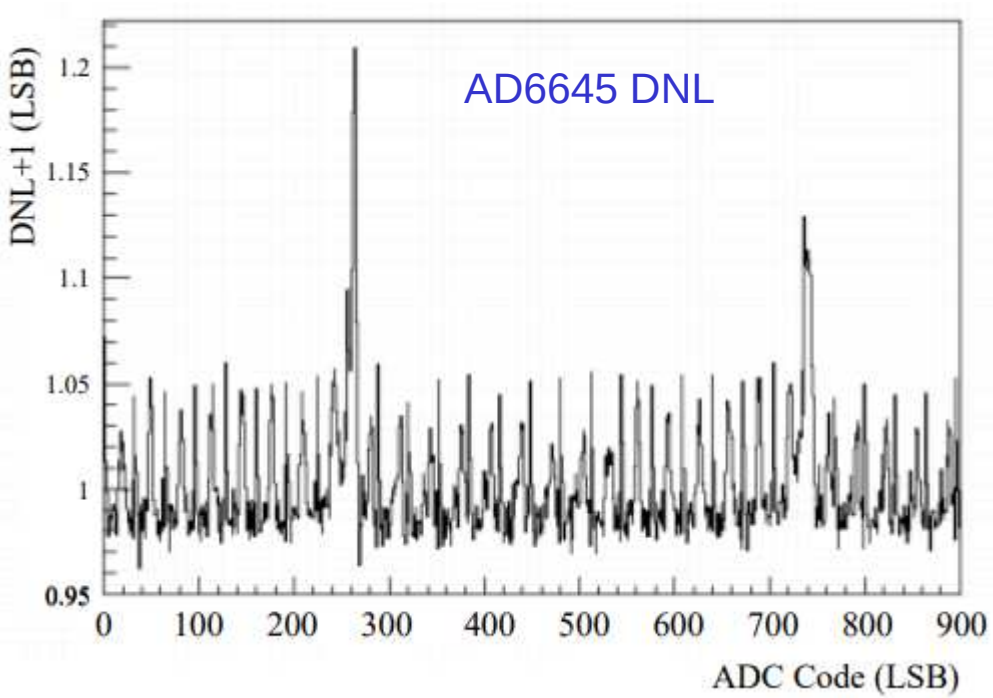
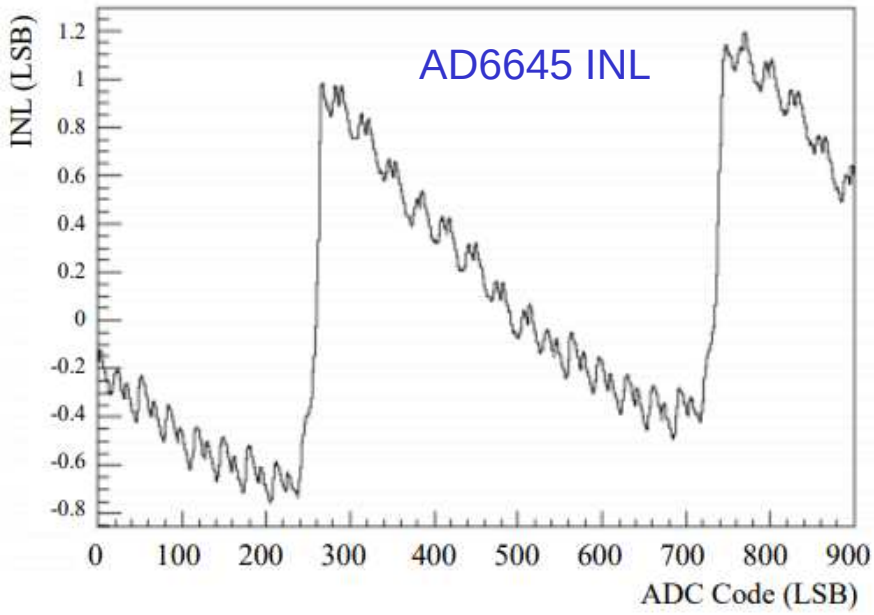


Figure 4
INL: integrate the measured DNL, subtract away overall slope.



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Majorana Nonlinearity Correction Algorithm

From Majorana Demonstrator paper

- Use the measured ADC value to index the correction table.
- The table provides deviations of the measured values from the perfect ADC response.
- Fig. 4: Corrected INL (red line) is almost perfect, except for small residual INL spikes near major ADC bit transitions.
- Fig. 8: Improvement of the 1592.5 keV and 1620.7 keV γ-lines by about 11%.
- Reference: N. Abgrall, et al, https://arxiv.org/pdf/2003.04128.pdf

Figure 4

Blue: raw data. Red: corrected

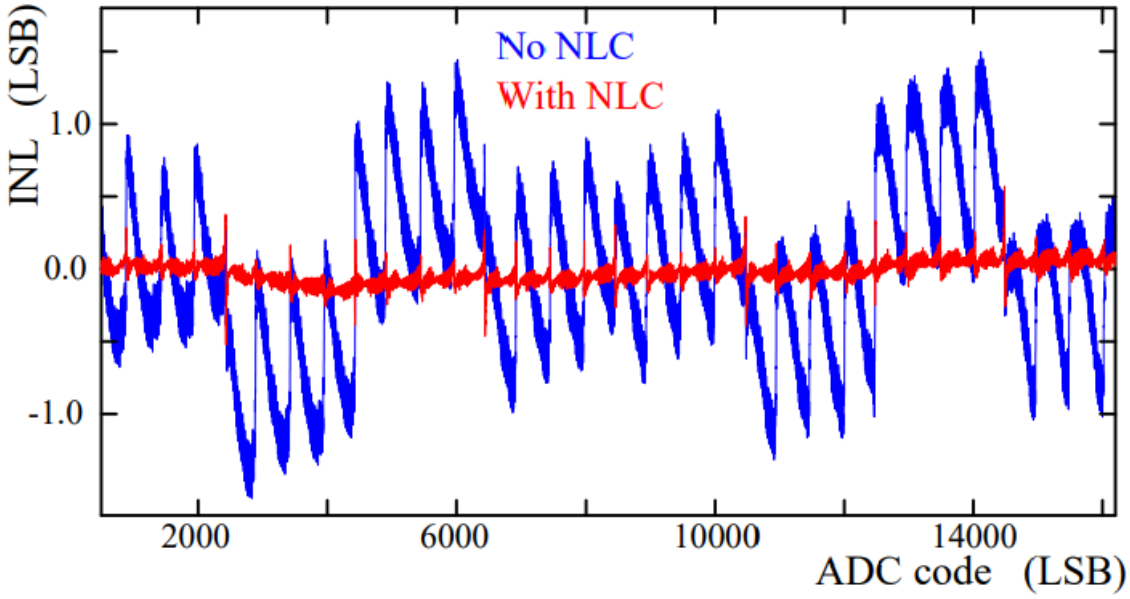
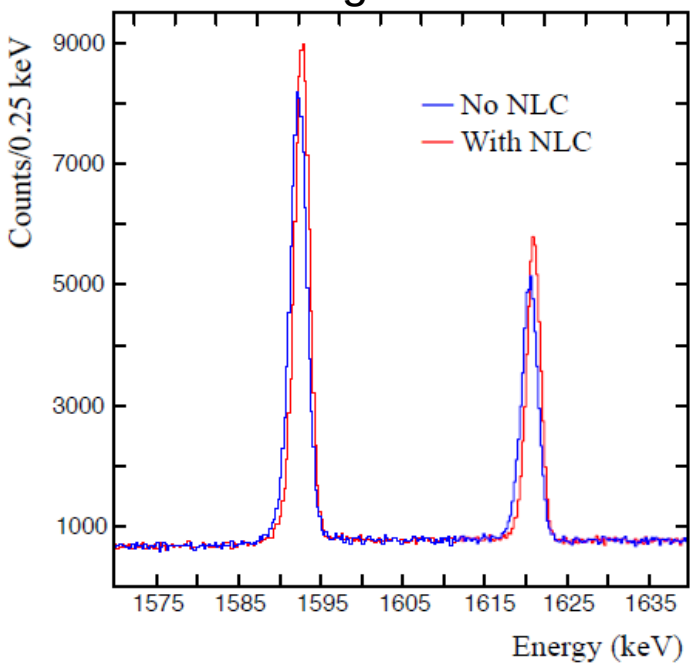


Figure 8



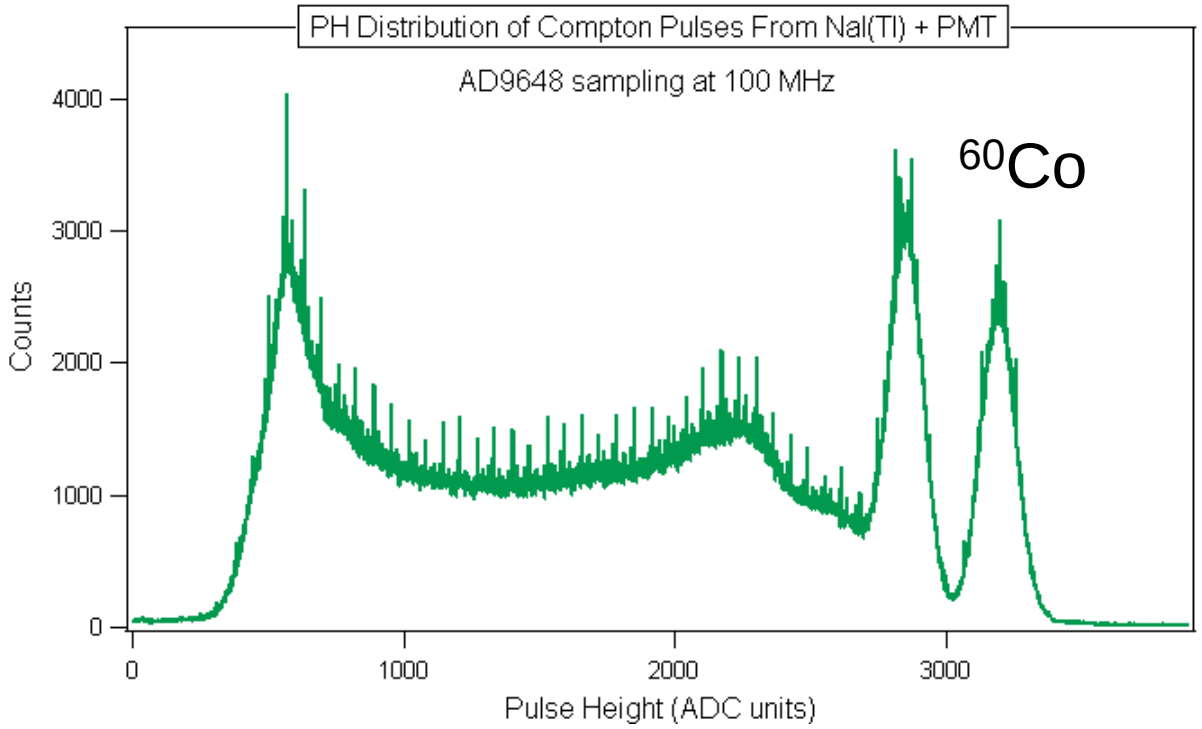
Let’s now turn attention to our project

Nonlinear Response of the Pipelined ADC

Demonstrated with our standard DDC-10 built with AD9648

- DNL is qualitatively demonstrated with the NaI(Tl) detector and ^{60}Co source.
- The spikes originate at the ADC stages which are not perfectly matched.
- The observed ADC bin width variation is in agreement with the AD9648 Data Sheet.
  - AD9648 is the name of the ADC chip which we used in DDC-10.

Spikes are caused by Differential Nonlinearity



Spikes indicate the ADC bin width variation from 1.0 LSB @ the baseline, to 1.6 LSB @ the spikes.

Consistent with the AD9648 Data Sheet, Table 1, page 4: DNL = +/- 0.5 LSB.

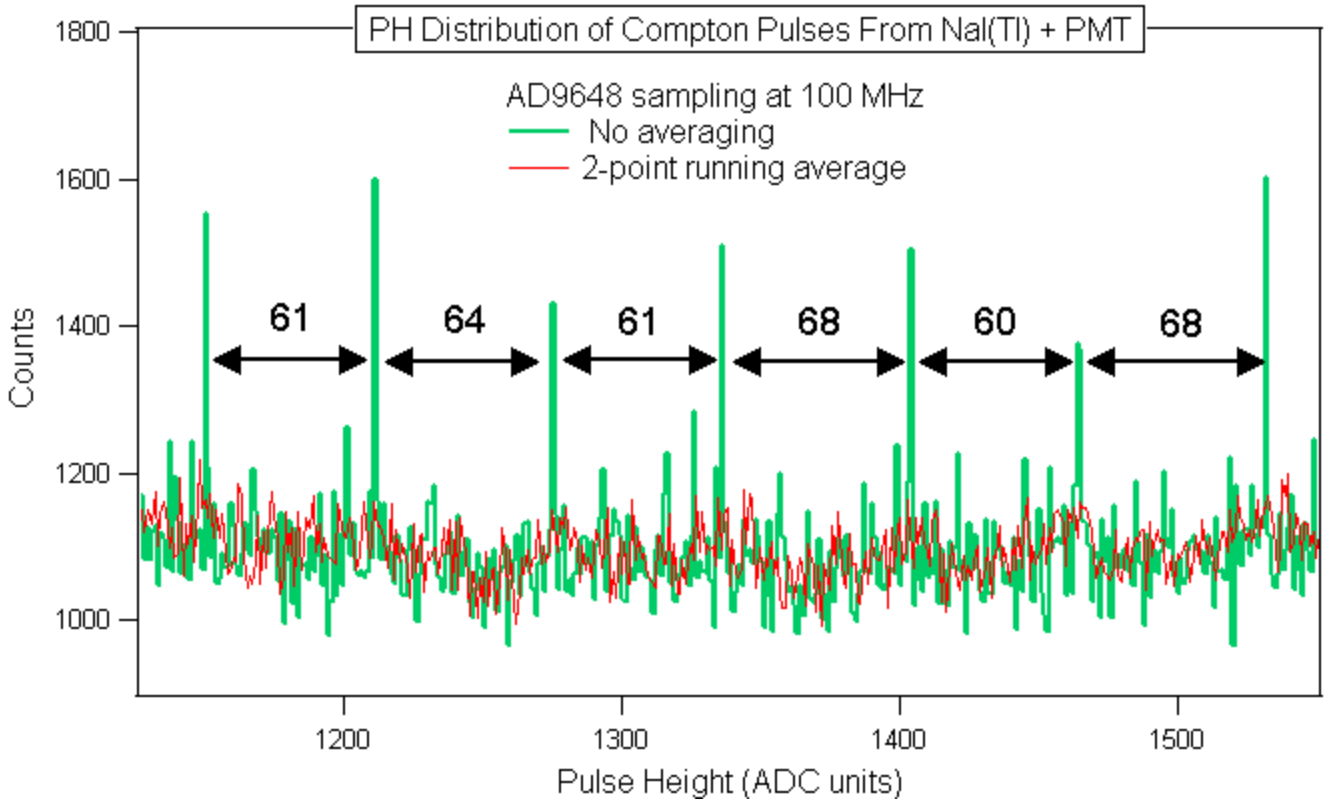
Nonlinear Response of the Pipelined ADC

Demonstrated with our standard DDC-10

The zoomed histogram is showing the semi-periodic Differential Nonlinearity (DNL).

The spikes may disappear after applying a running average (RA) to the waveforms. However, their effect still remains in high precision measurements with HPGe.

Spikes are caused by Differential Nonlinearity



Spikes indicate the ADC bin width variation from 1.0 LSB @ the baseline, to 1.6 LSB @ the spikes.

AD9648 Data Sheet, Table 1, page 4: DNL = +/- 0.5 LSB.

Running average (RA) is removing the spikes from the histogram.

Averaging will not remove the DNL impact on the HPGe resolution.

Fast / Slow Digitizer With 18-bit ADC & DAC

Implemented with our Dedicated Test Digitizer

1: Fast ADC, 2 channels, 14 bits
2: Slow ADC, 1 channel, 18 bits

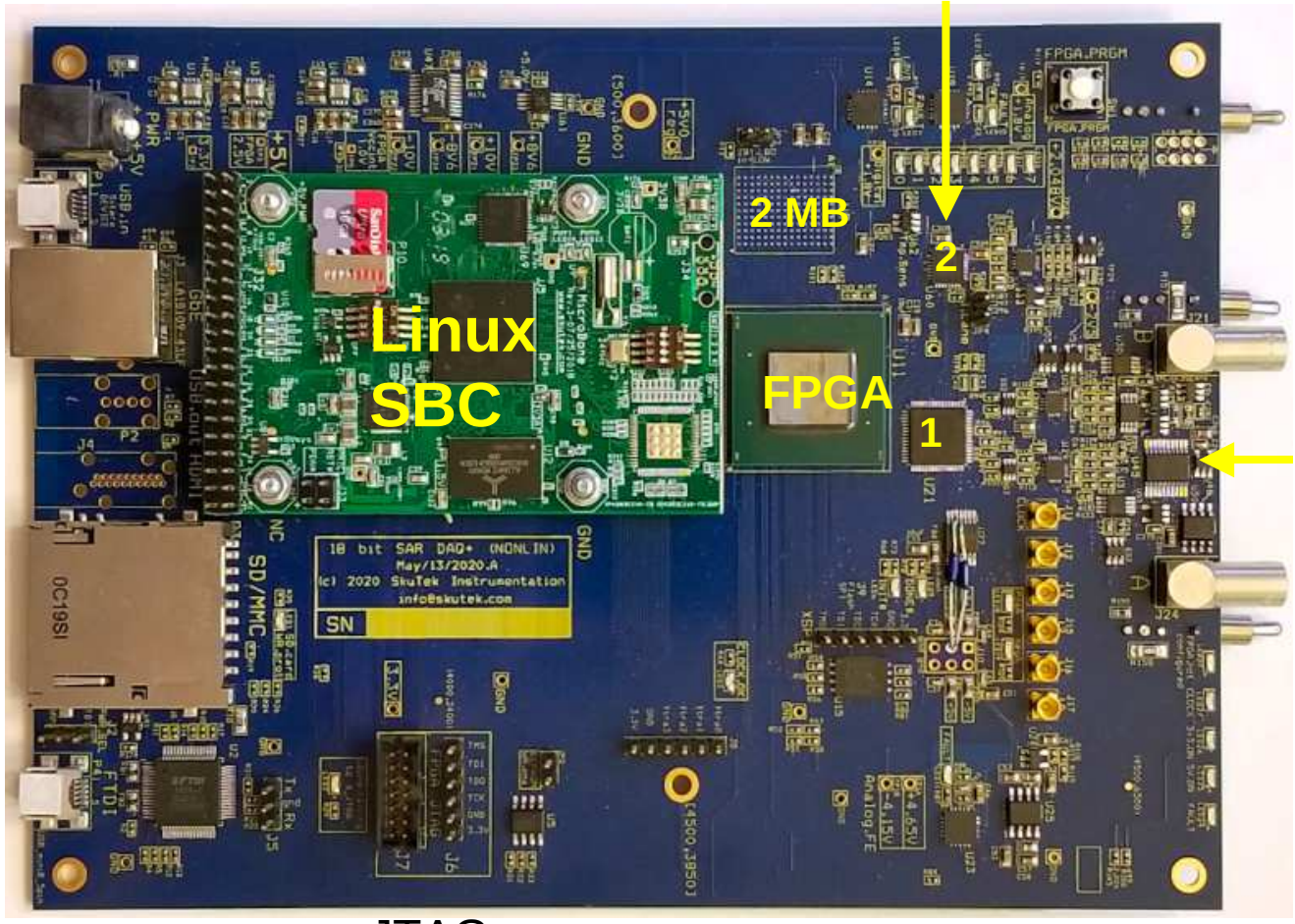
Voltage generators

+5V

Ethernet

SD card with Linux

JTAG & UART over USB



Input B

Calib. DAC

Input A

JTAG

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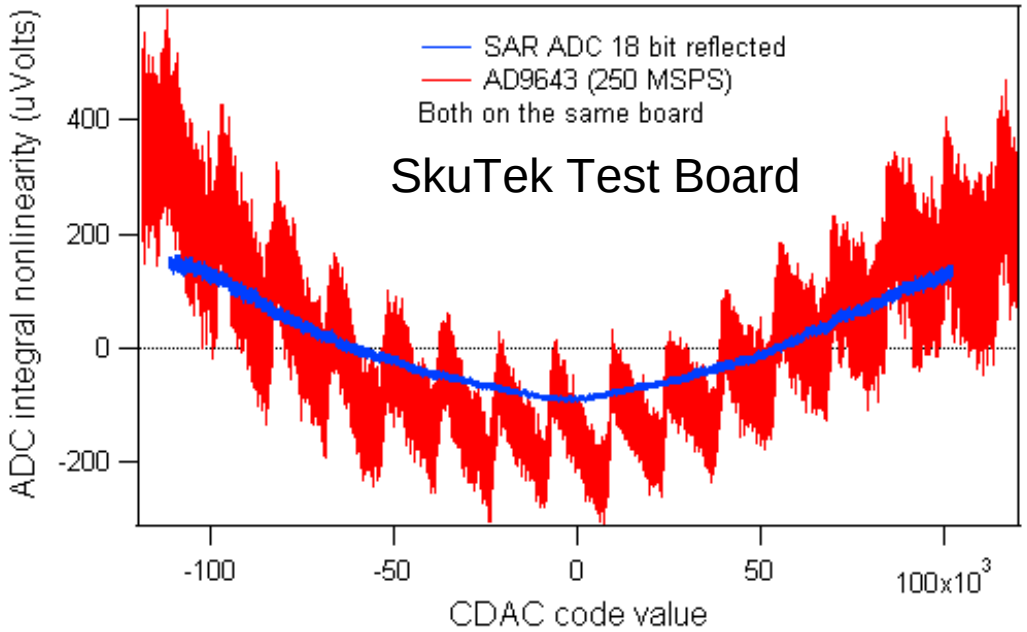
In Situ Nonlinearity Measurement

Performed with our Dedicated Test Digitizer

- For every 18-bit DAC voltage we recorded two ADC waveforms with 32k samples.
  - A waveform from the fast pipelined 14-bit ADC.
  - A waveform from the slow SAR 18-bit ADC.
- We calculated the averages of both waveforms and plotted against the DAC code.
- The slow SAR ADC was free of local nonlinearities (no sawtooth pattern).
- The fast pipelined ADC showed the sawtooth, as expected.
- The overall horseshoe pattern was caused by the operational amplifier at input.



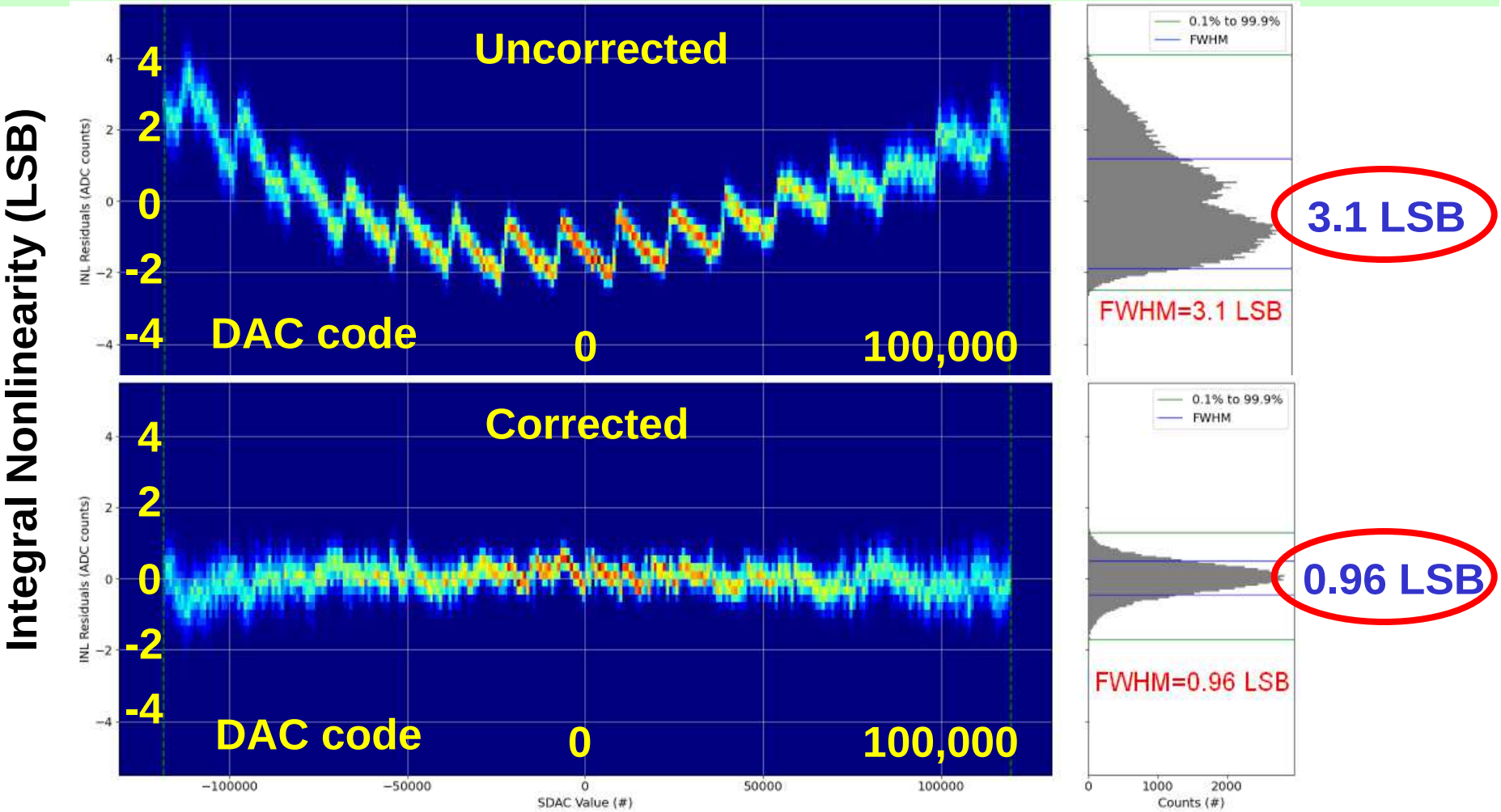
Blue: slow 18-bit ADC

Red: pipelined 14-bit ADC

Our Nonlinearity Measurement and Correction

Using our Dedicated Test Digitizer

- We measured the INL, using the on-board 18-bit DAC to drive the known voltage to the input.
- The stimulus voltage was verified using the 18-bit ADC in parallel with the 14-bit main ADC.
- After applying the correction, the 14-bit ADC response is at the limit of the ADC Data Sheet.



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Methods to Apply the Nonlinearity Correction

- Use the measured ADC value to index the correction table.
- The table provides a deviation of the measured value from the perfect ADC response.

- **How to apply the correction:**

1. Record the waveforms “as is” and apply the Majorana algorithm **offline**.
2. The correction can be applied **online** in real time to every ADC sample.
    - The correction tables can be stored in BRAM, whose amount is rather limited.
    - The lookup tables can be stored in external RAM, up to 512 MB in our case.
3. In low rate experiments the corrections can be applied by the on-board CPU.
    - This will be easy to program (in Python?), but execution will be slow.
4. In high rate experiments the correction can be executed by a firmware state machine.
    - Energy resolution is likely **not the primary objective** of high rate experiments.
    - Other factors may impact the resolution in high rate experiments, like event pileup or imperfect charge collection.

Supply Chain Crisis Mitigation

Example of Supply Chain… “Difficulty”

Thanks to part shortages we are unable to manufacture the boards.

The parts listed below are crucial for the MicroBone Linux Single Board Computer.

MicroBone critical parts lead time at DigiKey

None of the following parts were in stock on Aug/16/2022

AM3358BZCZ100	ARM® Cortex®-A8 1GHz	55 weeks*
TPS65217C	ARM Power generator 1.5 V	55 weeks*
TPS65217D	ARM Power generator 1.35 V	55 weeks*
LMZ10500SIL	Integrated DC-DC Converter	55 weeks*
DP83867CSRGZ	Ethernet PHY 1G	55 weeks*

* Manufacturer's standard lead time

Method of Supply Chain Mitigation

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- On-board Linux utilities and networking are very convenient and physicist-friendly.
- Building our Linux boards is now a challenge. Can we do without the Linux boards?
- We explored integration of an Open Source Soft CPU inside the FPGA. Advantages:
  - Fewer parts to procure and less exposure to critical part shortages.
  - Soft Core software is less resource hungry than Linux.

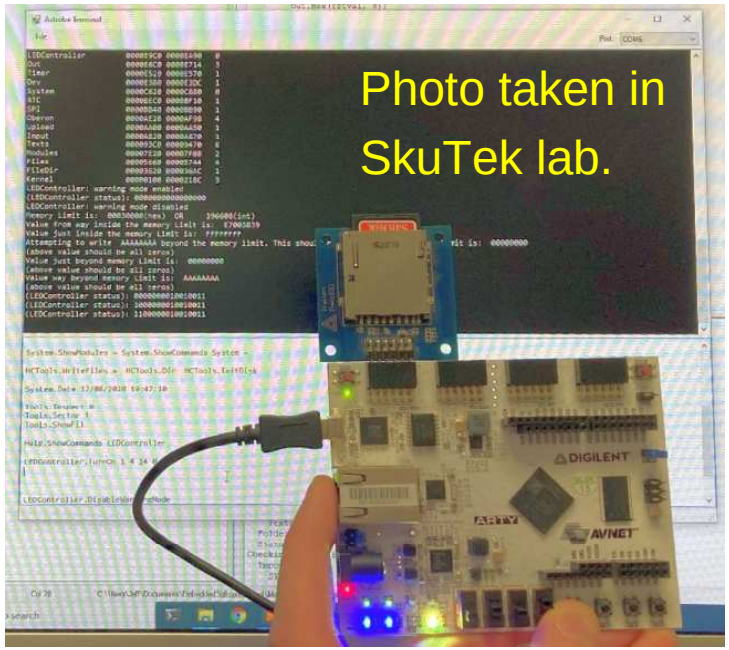
- Open source soft CPU named **RISC5** [ref. **1**], originally developed in 2013 for Xilinx Spartan-3. *RISC5 has nothing to do with the (now famous) RISC-V*.
- The core was ported to other FPGAs since then (Spartan-6, Spartan-7, Artix-7, …).
- The minimal RISC5 software runs in a single BRAM with 512 machine instructions.
- The core can also run a real time operating system in ~100 kilobytes.

[**1**] Niklaus Wirth, Xilinx's Xcell Journal, Issue 91, 2nd Quarter 2015. https://www.xilinx.com/publications/archives/xcell/Xcell91.pdf, page 30.

RISC5 Running Embedded OS in the FPGA

- Soft CPU is running an embedded real time Astrobe kernel inside the FPGA.
- Kernel provides for interrupts, multitasking, networking, and serial communication.
- Software is developed under Astrobe Development Environment. https://astrobe.com
- Compiled software modules are transferred to the board and stored on the SD card.
- Software is then loaded to the FPGA and executed on demand.

Digilent Arty A7 running Astrobe Kernel



Astrobe IDE running under Windows

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Summary and Status

- We developed **two** Linearity Test Boards with the 14-bit pipelined ADC, 18-bit stimulus DAC, and ancillary feedback ADC for verification of the stimulus test voltage.
- 250 MHz ADC (we showed the photo), and a 100 MHz ADC (not shown, looks similar).
- The boards let us measure the DNL and the INL without disconnecting the inputs.
- We measured the ADC response functions and derived the INL corrections.
- We applied the corrections both offline to recorded waveforms, and online in real time.
- We developed the firmware for applying real time corrections.
- The online correction tables were held in BRAM, whose amount is quite limited. We will move the tables to external RAM.
- The impact of the supply chain disruptions on this project.
- All the above work was performed with Phase I electronics.
- We could not build the planned Phase II electronics because parts are out of stock.
- The Phase II design work is delayed until it becomes clear which parts are available.
- We will be able to swiftly complete the designs after the part crisis subsides.
- We plan to eliminate nonessential parts to make our designs less prone to shortages.

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Future Plans

- Continue development of hardware, firmware, and software.
- Simplify our designs to decrease the exposure to electronic part shortages.
- Develop high linearity digitizers after it becomes clear, which parts are available.
- Contribute high linearity devices to Nuclear Physics experiments.
- Support the DOE mission through contributing to NP projects.
- Survive the part supply crisis till electronic parts are available again.

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