DOE SBIR/STTR Tech Exchange

STTR Phase 2 Topic 28b

A multi-channel radiation-tolerant, low-power, high-speed and resolution analog-to-digital converter for nuclear physics detectors

Presenters:

PI: Dr. Ping Gui, Professor, Southern Methodist University (pgui@lyle.smu.edu)

Kyle Schulmeyer, Principal Analog Designer (kyles@apogeesemi.com)

Outline

- Company Overview
- Measured performance on Multi-GS/s, Radiation-Tolerant Analog-to-Digital Converter
- Radiation resiliency tests on 28nm process (TID, SEE and Neutron)
- Conclusion

About Our Company

Our Mission:

- **Bridging the technology gap between commercial and high reliability components**
- **Significantly lowering the cost of rad-hard integrated circuits (ICs)**
- **Expanding our portfolio to support our customers needs**

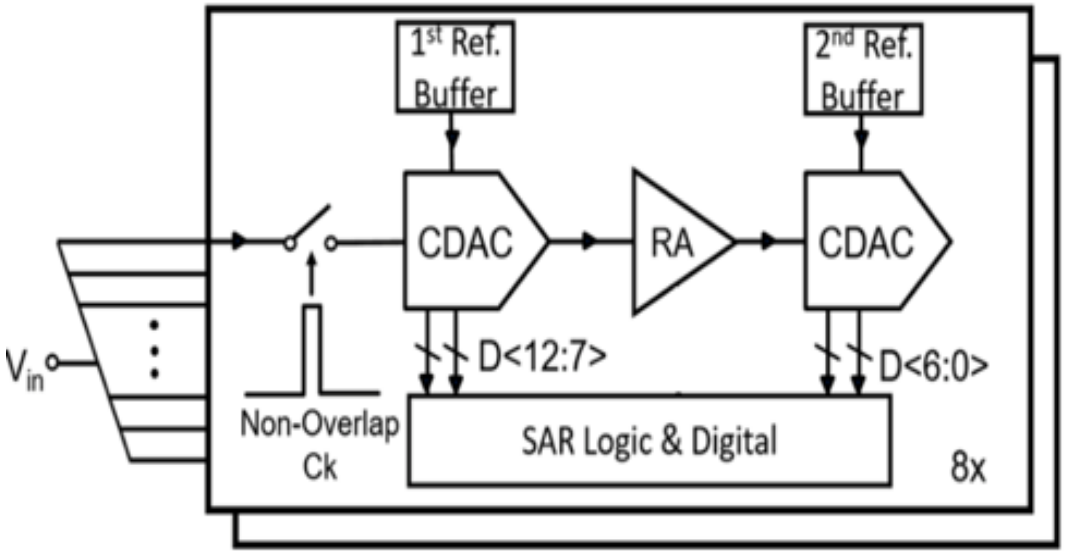
- Focused on rad-hard IC design and process development
- Developed TalRad™ rad-hard IC design process
  - TSI Semiconductors, is the trusted fab
- Growing portfolio
  - 9 products in production status today
  - 25 products to be released to production by end of 2022
  - Additional product releases in 2023
  - Today's offering is logic, interface and translation

Multi-GS/s Radiation-Tolerant Analog-to-Digital Converters (ADC)

Single-Channel 1GS/s 12-bit ADC - Main Features and Applications

Features

- Sample rate: ≥ 1GS/s in CMOS
- 12 bit resolution (~10b ENOB)
- 1st version in 28nm: 6.7mW per 1GS/s, area of 0.007mm^2
- 2nd Version in 28nm: 5.8mW per 1GS/s, area of 0.0062mm^2



Radiation Tolerance

- TID immunity > 2 Mrad (Si)
- SEL up to 86 MeV·cm^2 /mg (expected)

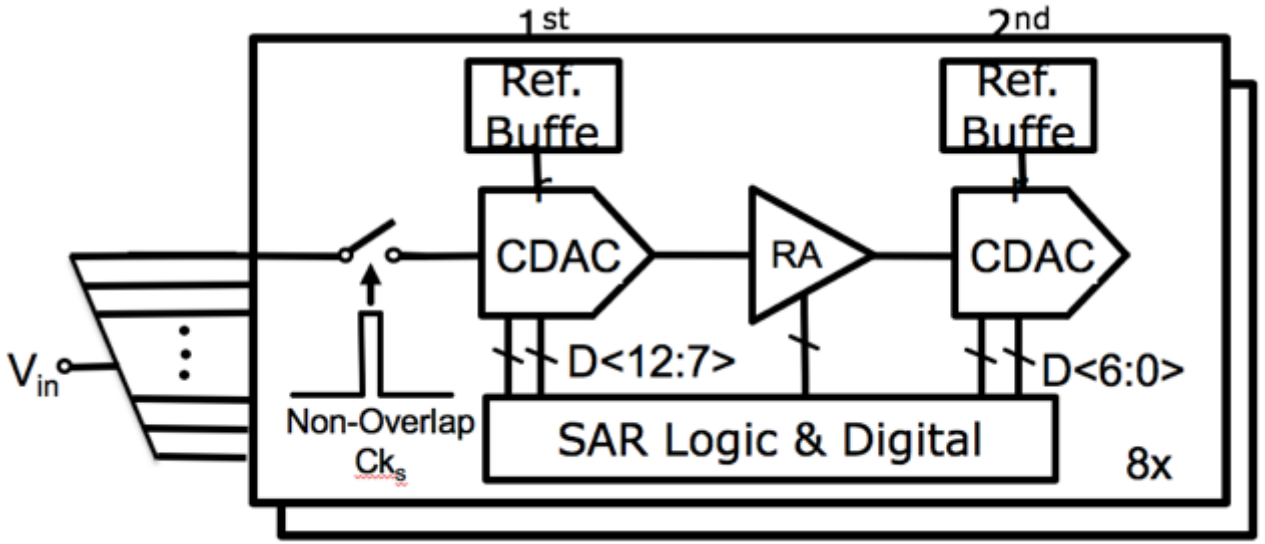
Applications

- Pixelated detectors
- Waveform sampler
- Real time oscilloscope

Multi-GS/s 12-bit ADCs Developed During this Project

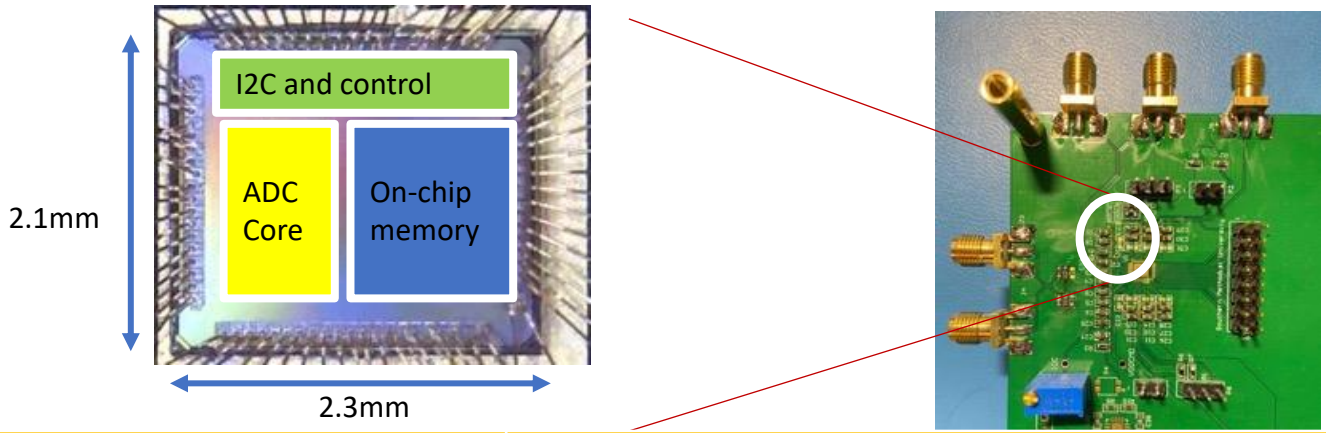
- Three 12-bit GS/s ADCs have been developed and measured on silicon
  - 2.56GS/s 8-channel interleaved ADC in 65nm
  - 1GS/s single-channel ADC in 28nm
  - Low-Power compact 1GS/s single-channel ADC in 28nm
- Total Ionization Dose (TID) radiation tolerance tested up to 2 Mrad (Si)

2.56GS/s 12-bit ADC
Interleaving 8 Single-Channel SubADCs in 65nm CMOS



- Design challenges:
  - High sampling rate while still maintaining high resolution
- Interleaving 8 channels (each channel at 320MS/s) in time-domain to get overall sampling rate of 2.56GS/s
  - Timing skew inter-channel mismatches
  - Intra-channel mismatches
- Various calibrations to minimize mismatches

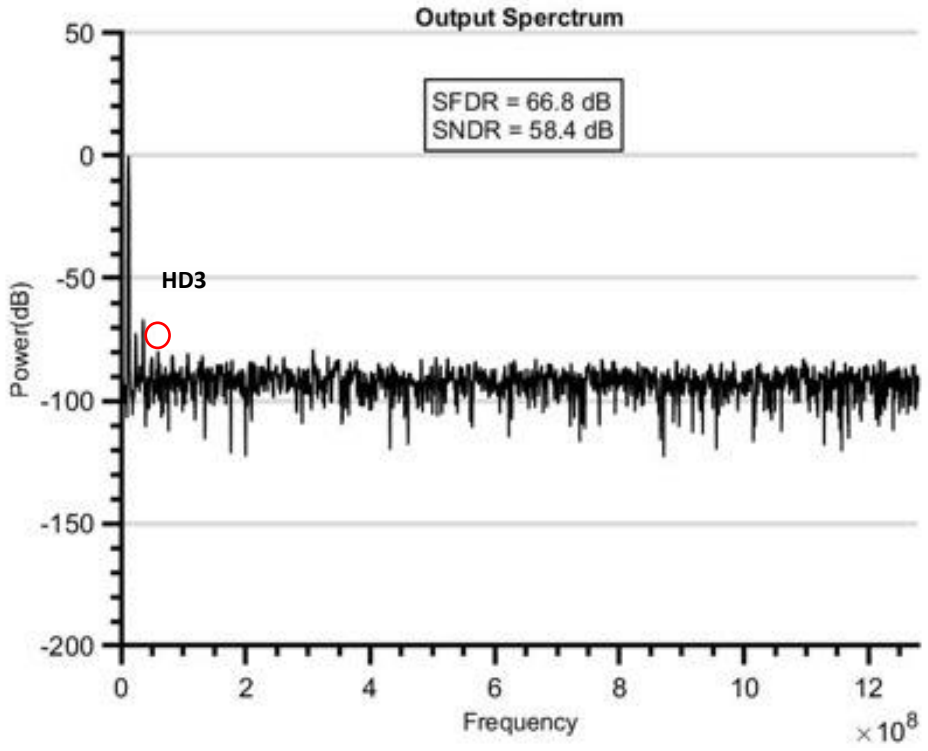
12-bit 2.56Gbps ADC Interleaving 8 Channels

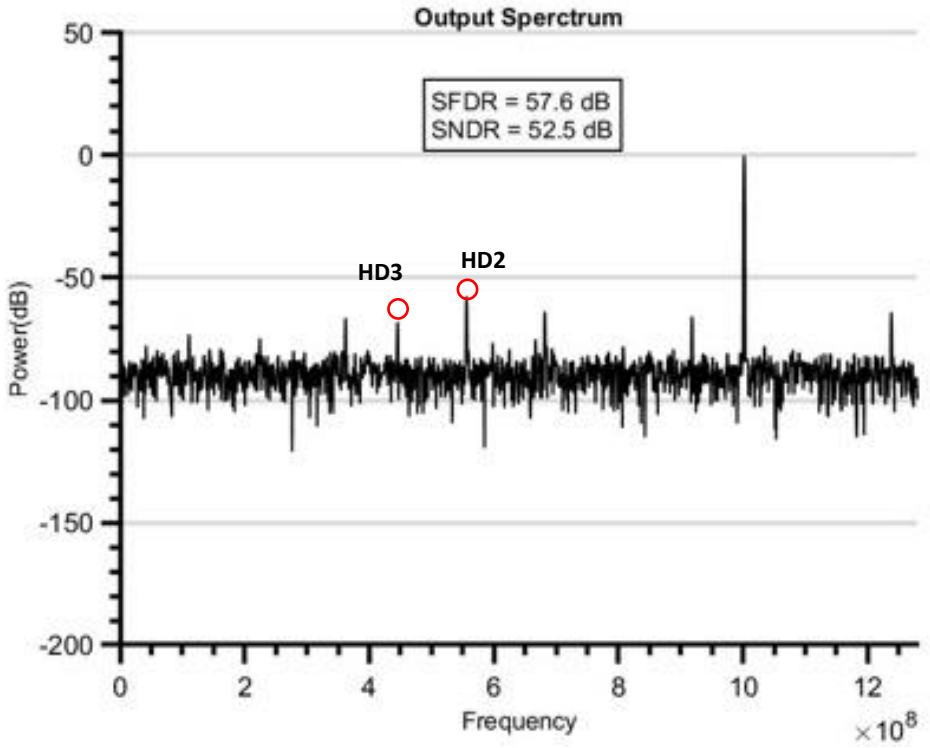


Specs	Measurement Results
Sampling Rate	Up to 2.56 GS/s
ENOB (Effective Number of Bits)	9.4 bits @ 13MHz and 8.4 bit at @1GHz input
Power Consumption	92 mW (in continuous operation), power on/off feature available
Core area	1mm x 0.8mm
Topology	Pipelined-SAR
Technology	65nm CMOS

L. Fang, P. Gui, et. Al, "A 2.56 GS/s 12-bit 8x-Interleaved ADC with 156.6 dB FoMs in 65 nm CMOS", *IEEE TVLSI*, vol. 30, no. 2, pp. 123-133, Feb. 2022.

2.56GS/s 12-bit ADC Measurement Results (frequency spectrum to evaluate SNDR/SFDR)



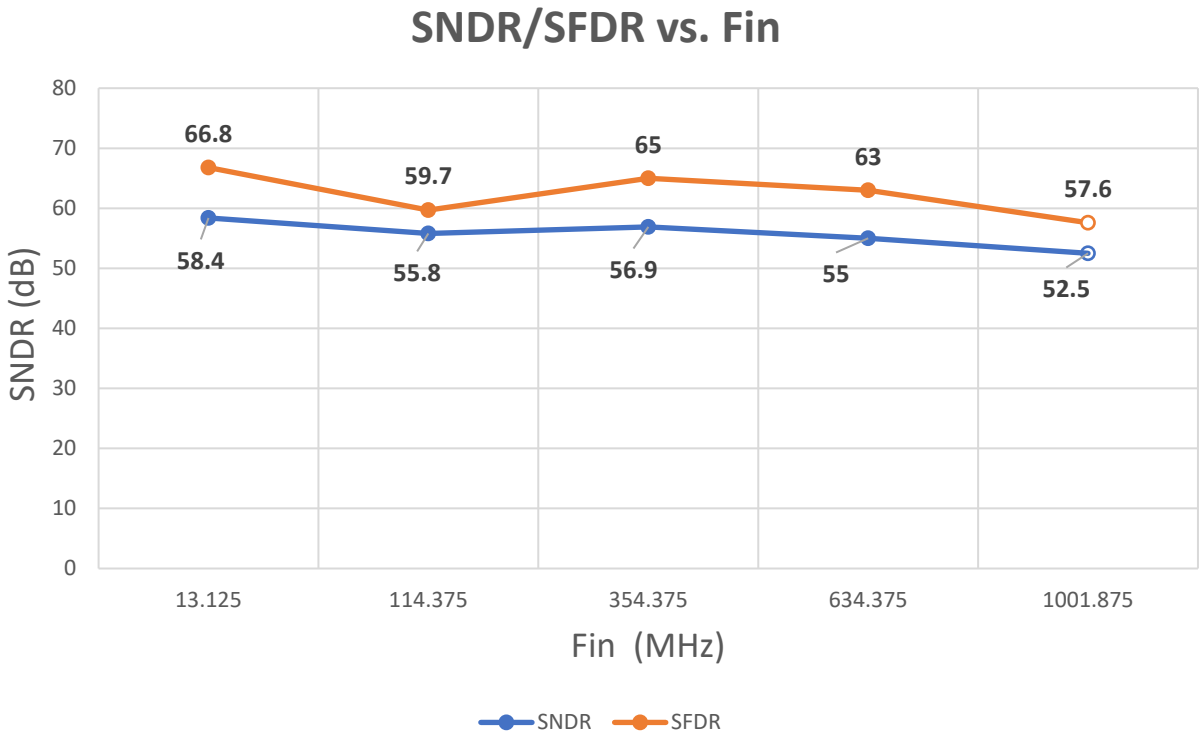


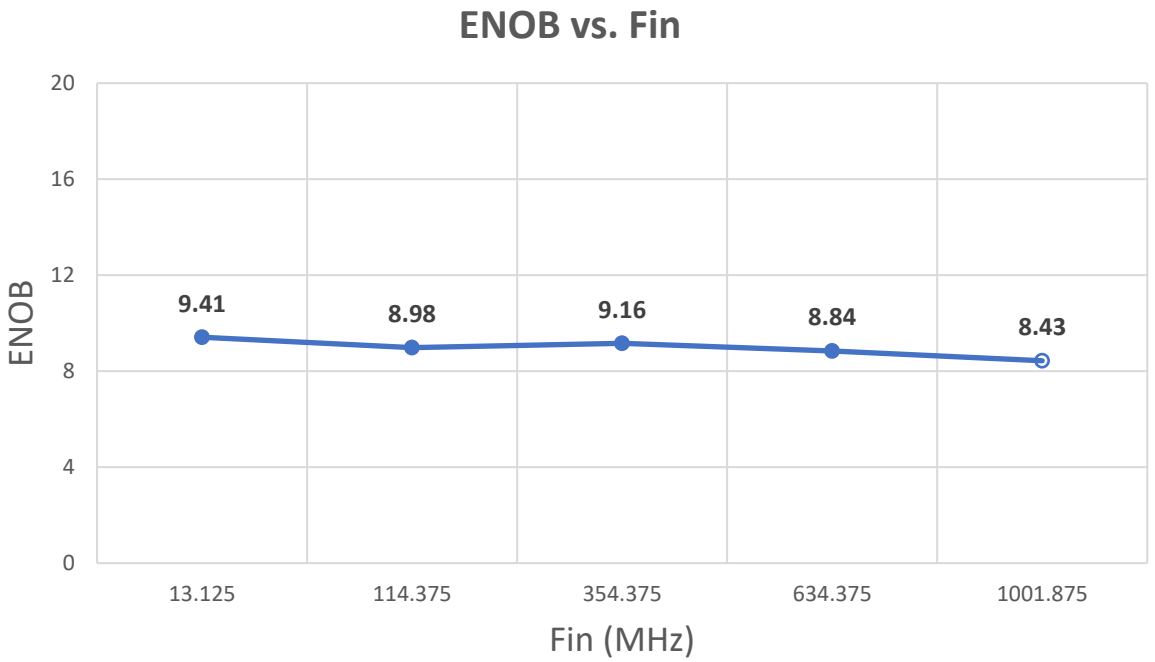
- Fin=13.125 MHz, Fs=2.56GS/s
- SNDR=58.4dB
- ENOB=9.41 bit

- Fin=1001.875MHz, Fs=2.56GS/s
- SNDR=52.5dB
- ENOB=8.43 bit

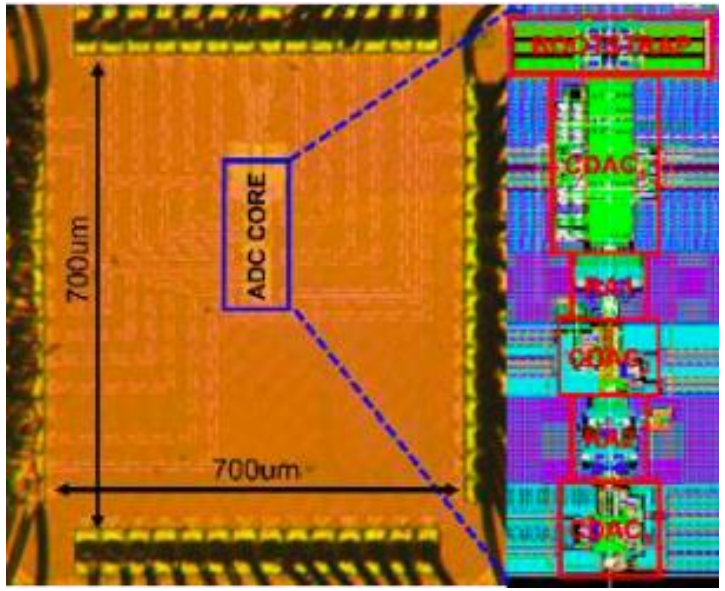
2.56GS/s 12-bit ADC Measurement Results (dynamic performance vs. f_{in} at sampling rate of 2.56GS/s)

- SNDR: Signal to Noise and Distortion Ratio
- SFDR: Spurious Free Dyanmic Range
- ENOB: Effective number of bits; ENOB = (SNDR-1.76dB) / 6.02

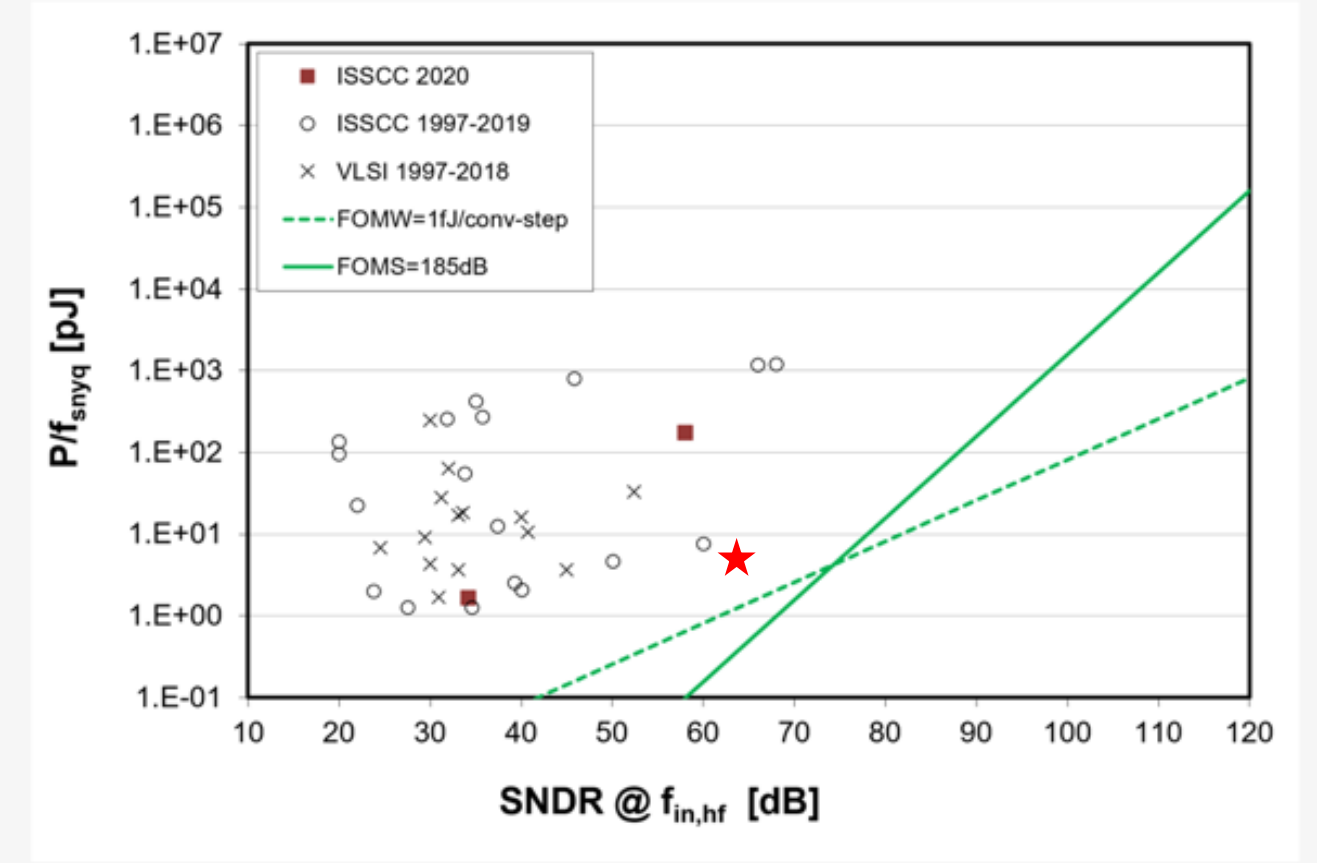




12-bit 1GS/s Single-Channel ADC in 28nm CMOS

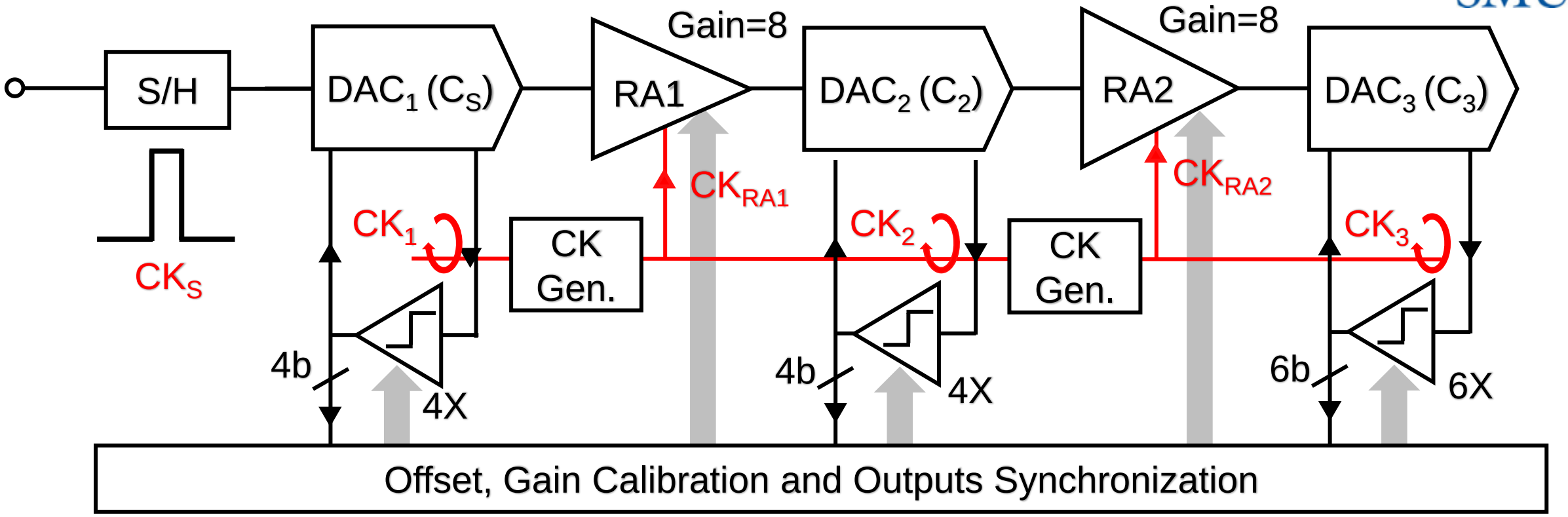


- 3-stage pipelined SAR architecture to achieve the targeted sampling rate and resolution with excellent power efficiency
- At Nyquist input, 1GS/s, SFDR ≥ 73dB, SNDR=61dB, ENOB=9.8 bits, total power of 6.7mW, area of 0.007mm^2



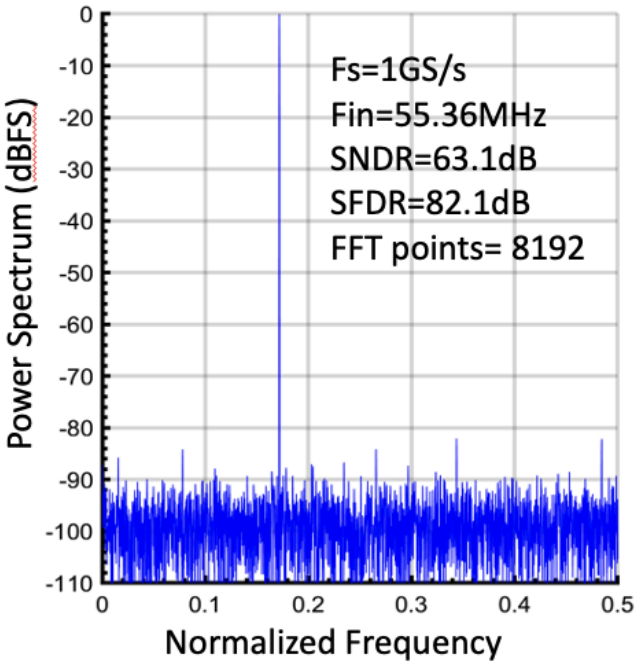
L. Fang, P. Gui, et. Al, "A 12b 1GS/s 61dB SNDR pipelined-SAR ADC with Inverter-based Residual Amplifier and Tunable Harmonic-injecting Cross-coupled-pair for Distortion Cancellation Achieving 6.3fJ/conv-step", IEEE Solid-State Circuits Letters, Vol. 5, 2022.

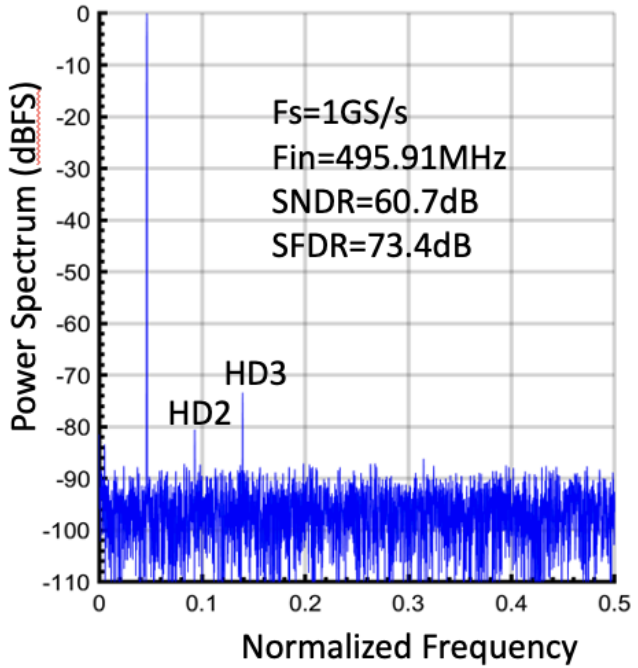
1GS/s 12-bit Pipelined SAR ADC Architecture

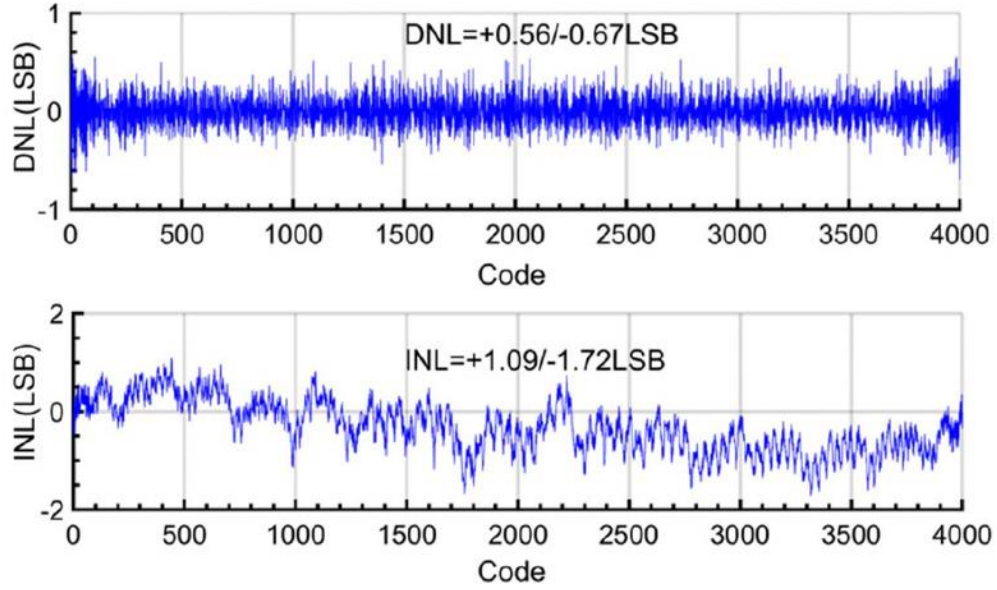


- Three stage asynchronous pipeline SAR ADC
- CDAC1/2/3: 4b/4b/6b (1b interstage redundancy)

12-bit 1GS/s ADC in 28nm CMOS Measurement – Frequency Spectrum and DNL/INL



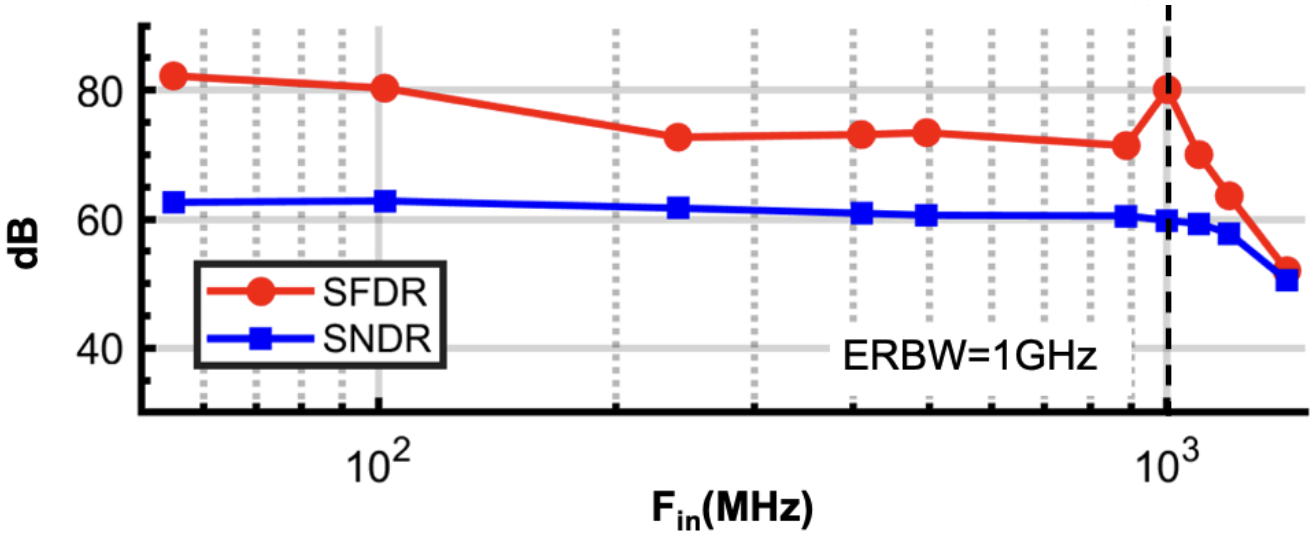


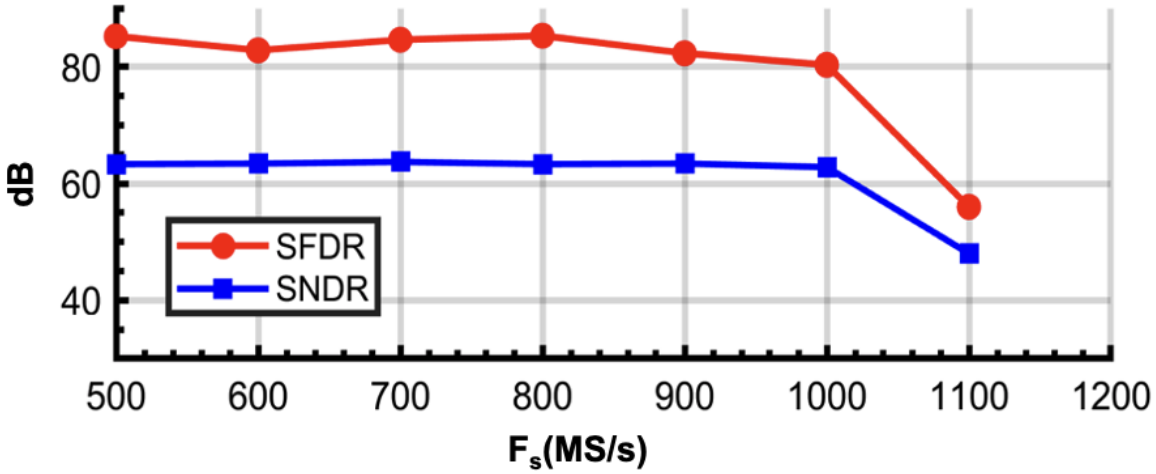


- @low Fin
- SNDR=63dB, SFDR =82dB, ENOB =10.1bits

- @Nyquist input
- SNDR=61dB, SFDR =73dB, ENOB =9.8bits

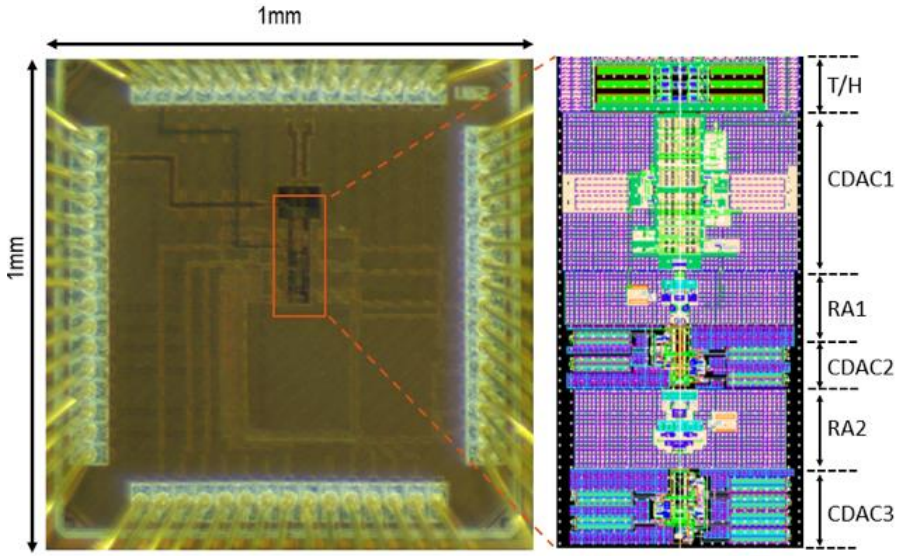
12-bit 1GS/s ADC in 28nm CMOS Measurement - SNDR/SFDR when sweeping F_{in} and F_s

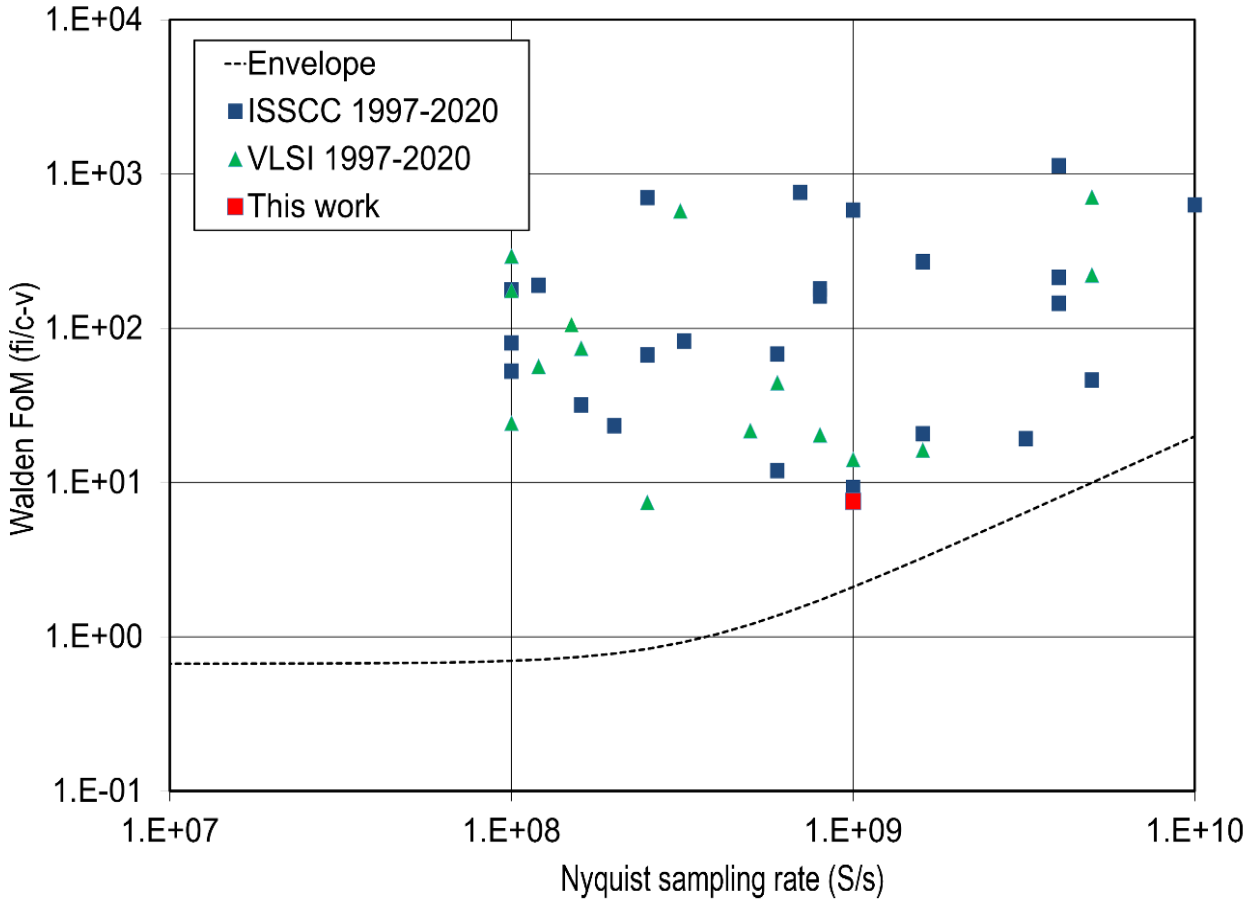




- @Nyquist, SFDR=73dB, SNDR=61dB, ENOB =9.8 bits

Optimized Low-Power Compact 12-bit 1GS/s Single-Channel ADC in 28nm CMOS

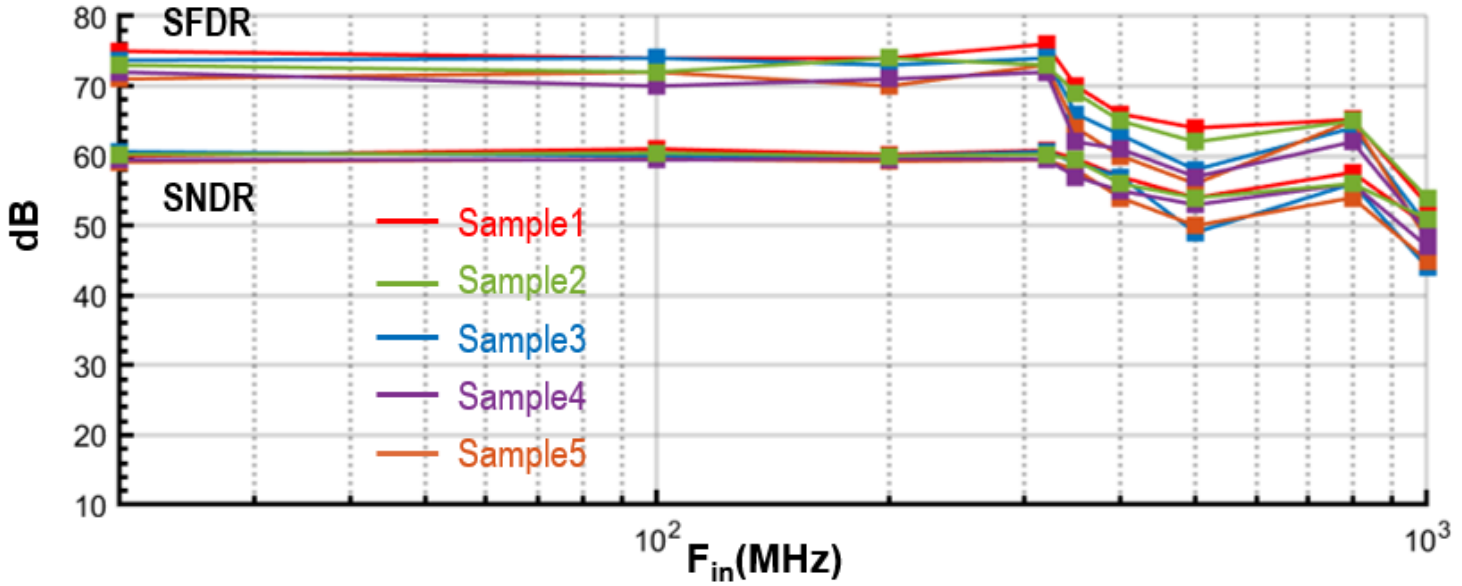


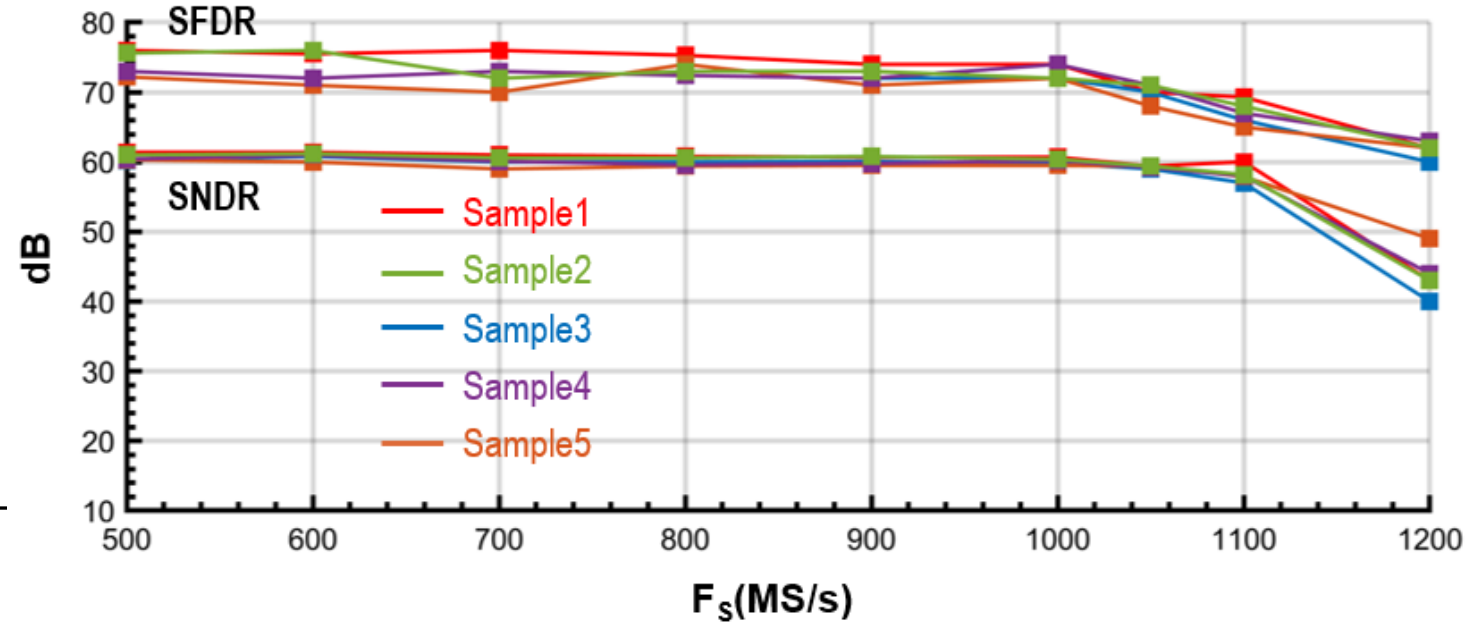


- At Nyquist input, 1GS/s, SFDR ≥ 76dB, SNDR=61dB, ENOB=9.8 bits, total power consumption of 5.8mW, area of 0.0062mm^2
- Low power and small area suitable for integrating multiple ADCs channels on chip in nanometer CMOS

L. Fang, P. Gui, et. al "A 12-Bit 1 GS/s RF Sampling Pipeline-SAR ADC with Harmonic Injecting Cross-Coupled Pair Achieving 7.5 fj/conv-step", IEEE Transactions on Circuits and Systems I - Regular Papers (TCAS-I), Vol. 69, Iss. 8, 2022.

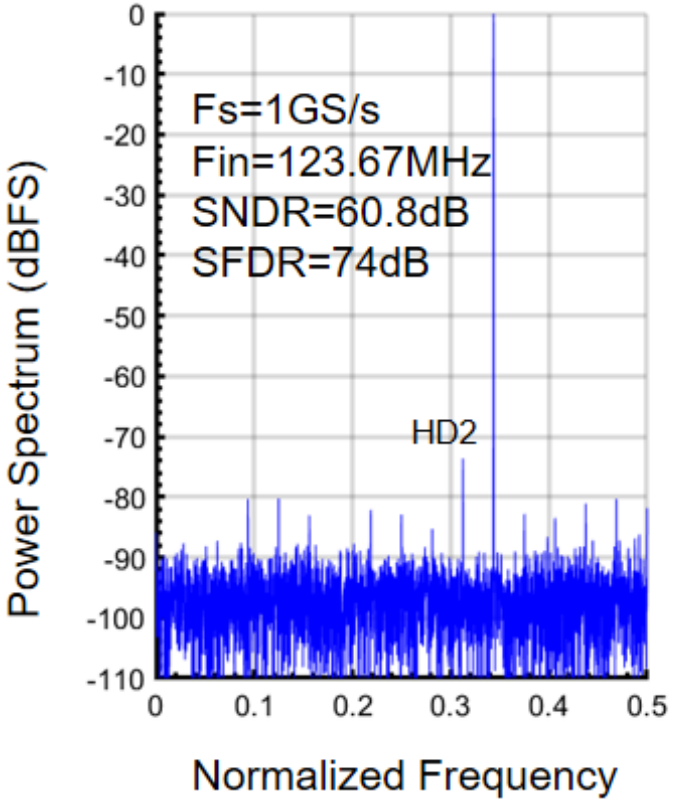
Measurement Results (SNDR and SFDR) with 5 Chip Samples

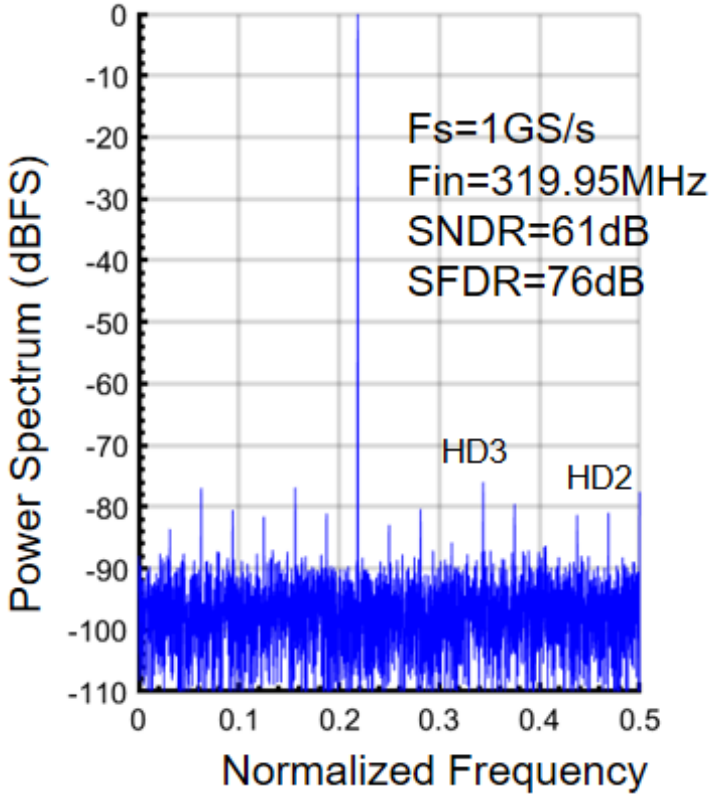


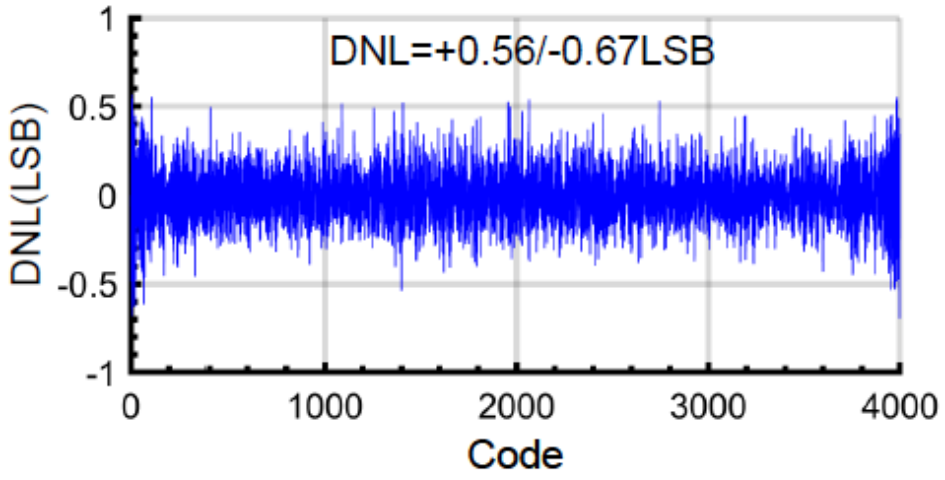


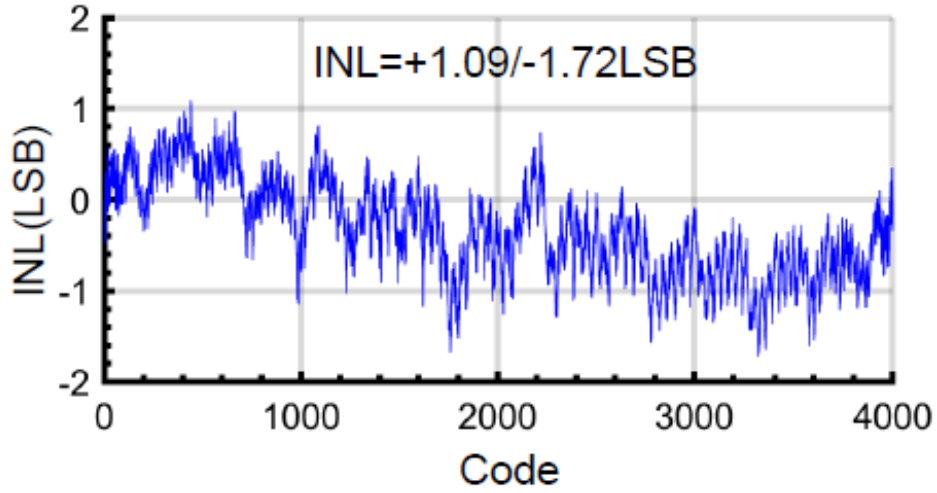
APOGEE SEMICONDUCTOR

Measurement Results (Frequency Spectrum and DNL/INL)

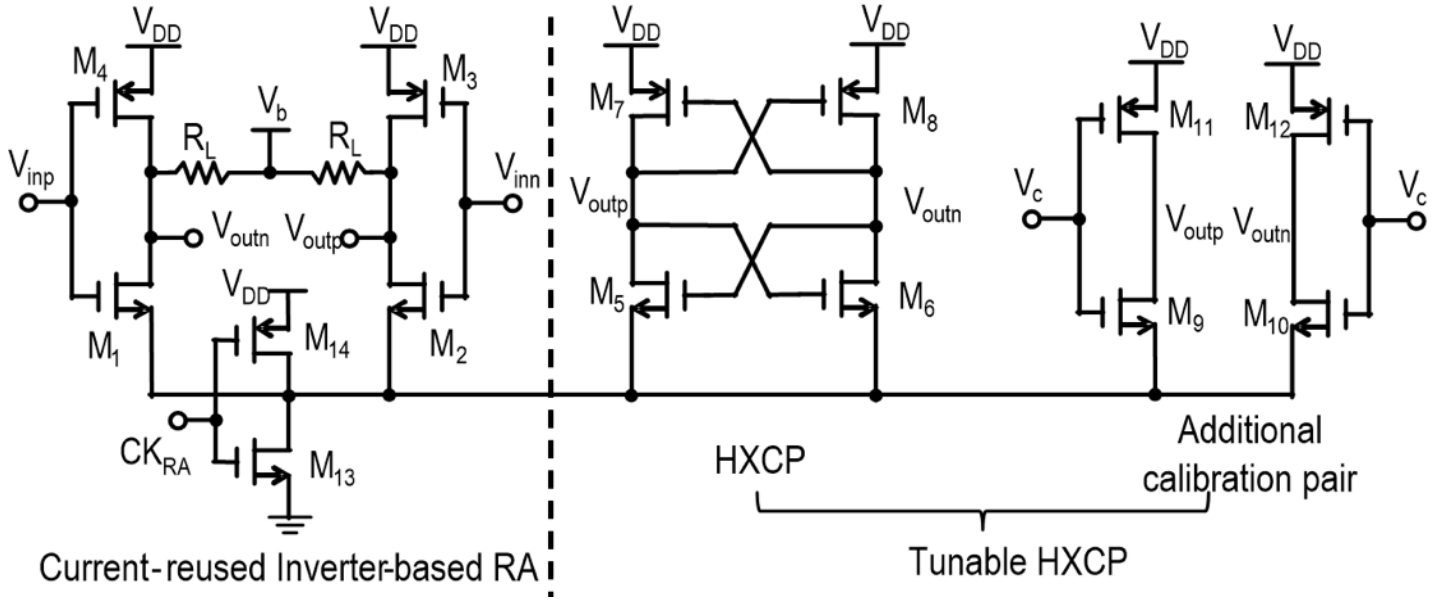


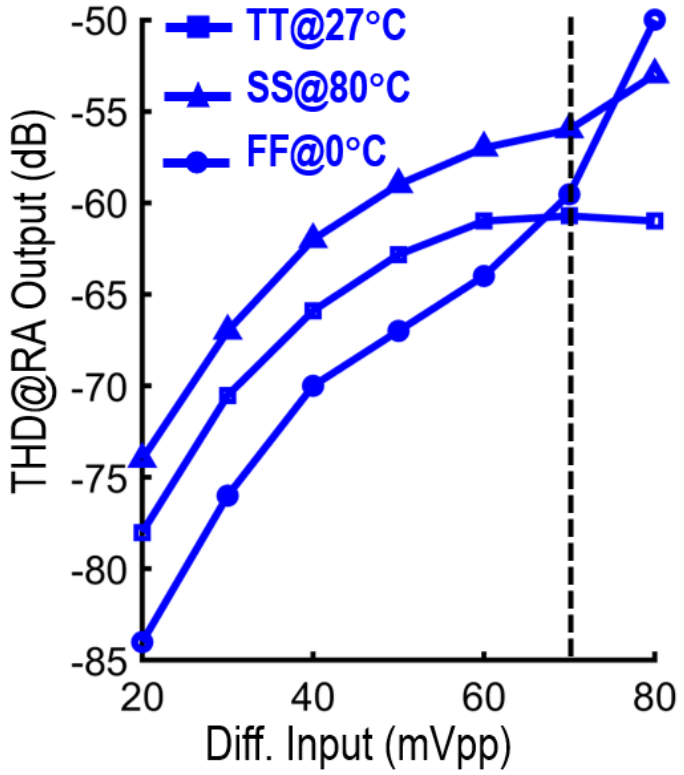






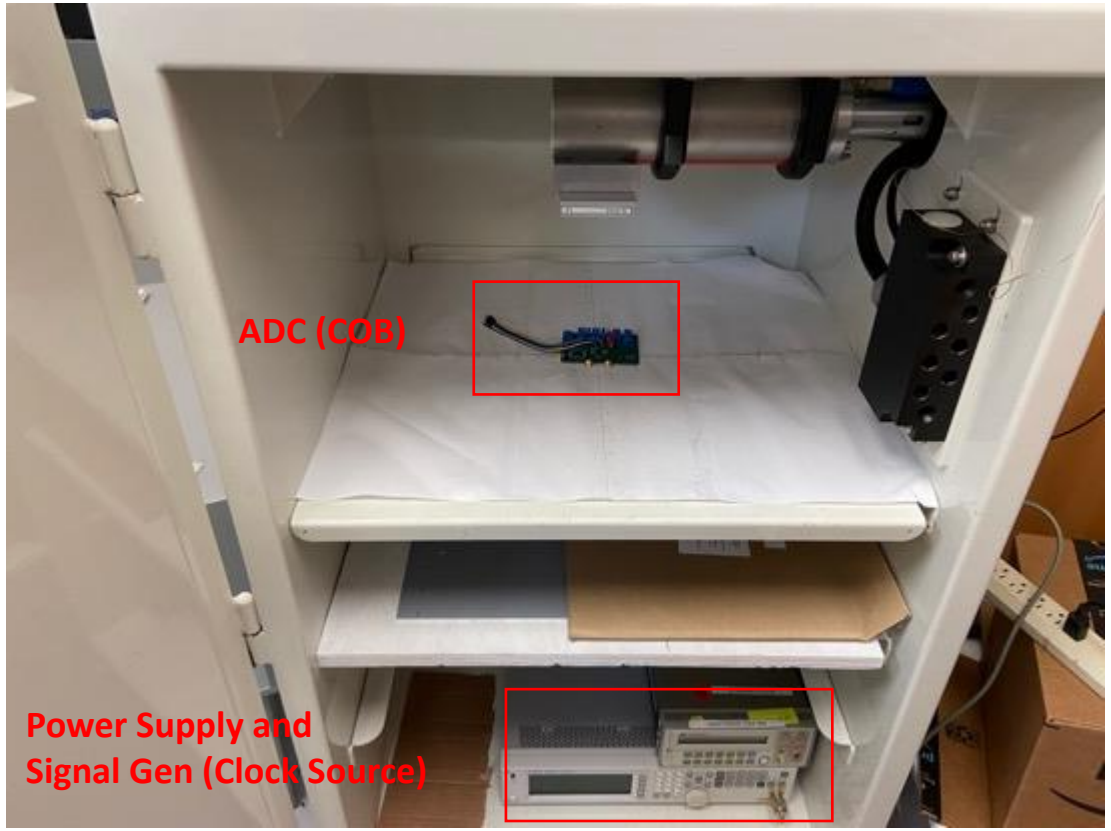
Novel Inverter-Based Residue Amplifier Design in the 2nd ADC





- Inverter-based residue amplifier design
  - Low power consumption
  - Compatibility with low-supply-voltage nanometer CMOS
  - Good PVT tolerance

Total Ionization Dose (TID) Testing Setup



- The ADC COBs were put in the X-ray radiation chamber at SMU with maximum dose rate (18rad/s).

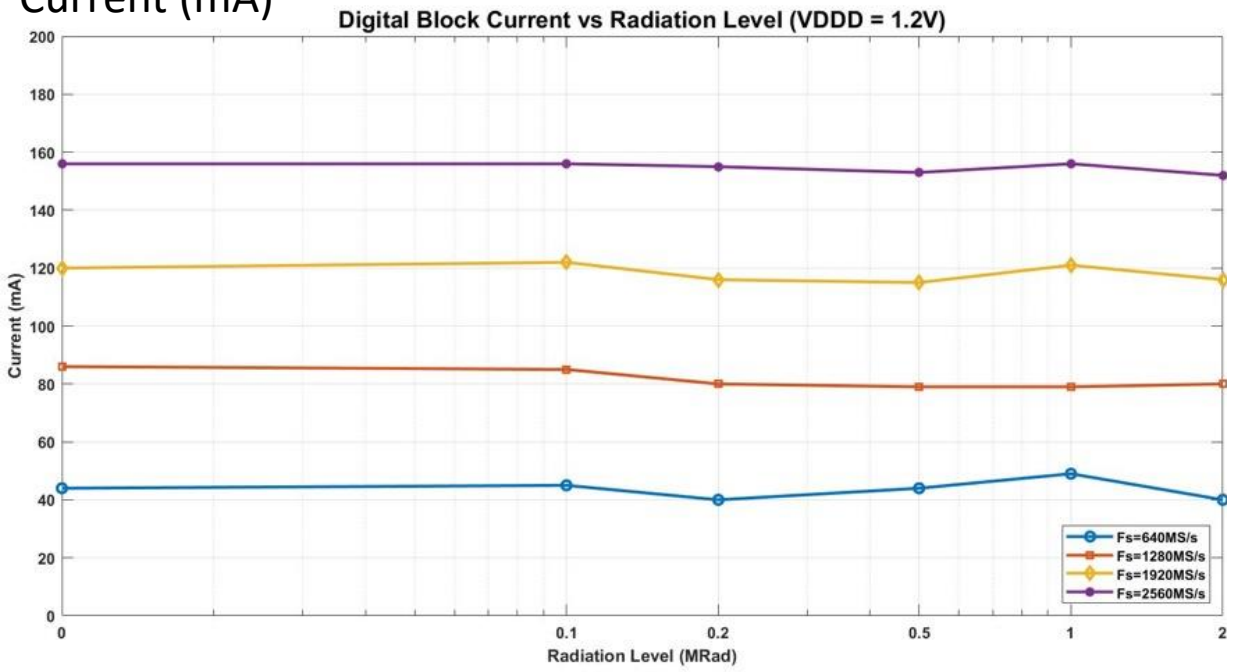
- The ADC chips were powered on and a fast sampling clock was provided during the radiation test
  - Inside the chamber:
    - power supply for DC biasing of the chips
    - The signal generator that provides the fastest sampling clock
  - Other power supply for the ADC was put outside of the chamber for current monitoring.

- Radiation Test points:
  100krad, 200krad, 500krad, 1Mrad, 2Mrad

65nm 2.56GS/s ADC: Current vs. Radiation Level

Digital Power Domain with VDDD = 1.2V, 1,08V and 1.32V

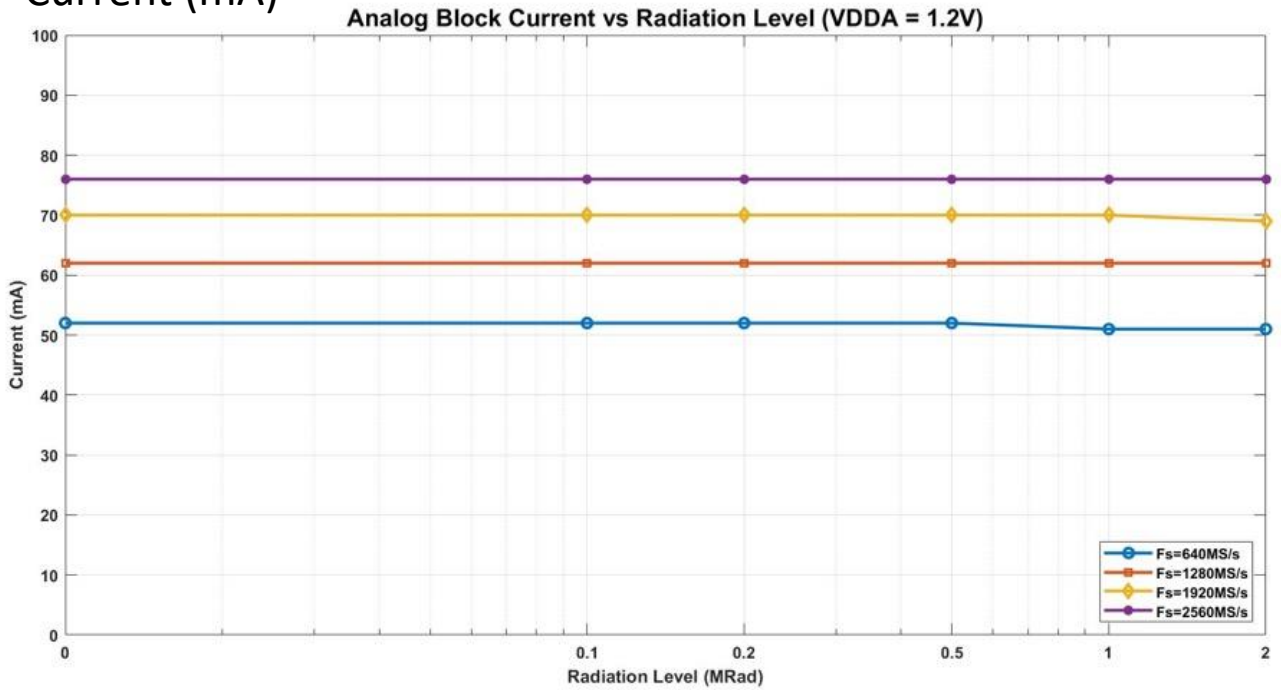
Current (mA)



TID (Mrad (Si))

Analog Domain with VDDA = 1.2V, 1,08V and 1.32V

Current (mA)

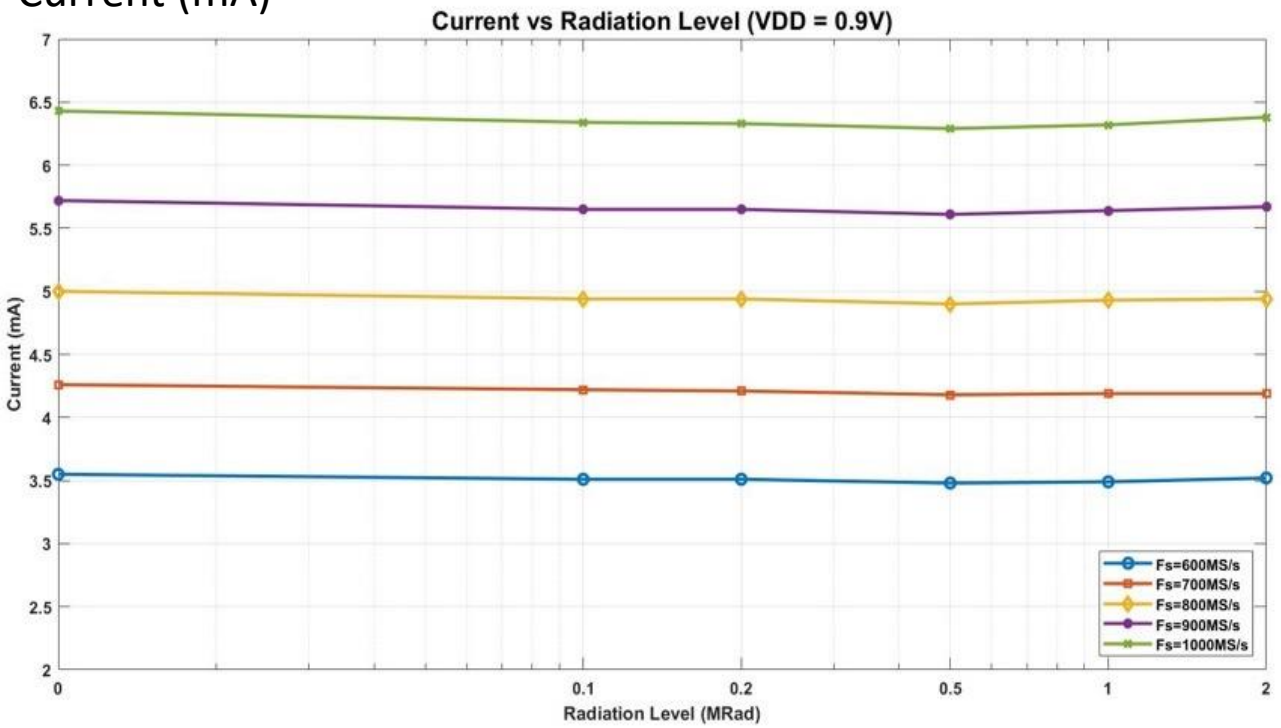


TID (Mrad (Si))

Negligible variation on the current drawn from either the digital domain or analog domain from pre-rad to 2Mrad

28nm 1GS/s ADC TID Measurement

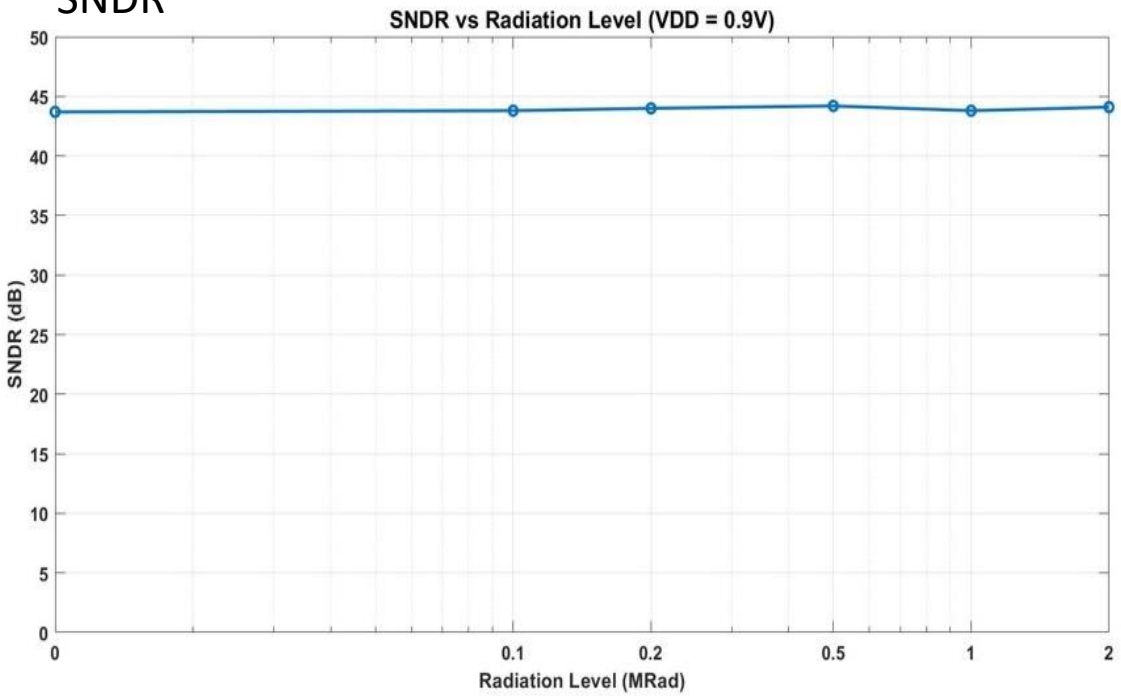
Current (mA)



TID (Mrad)

Negligible variation in the total current drawn from the chip with TID radiation tested up to 2Mrad (also tested at various sampling clock frequencies)

SNDR



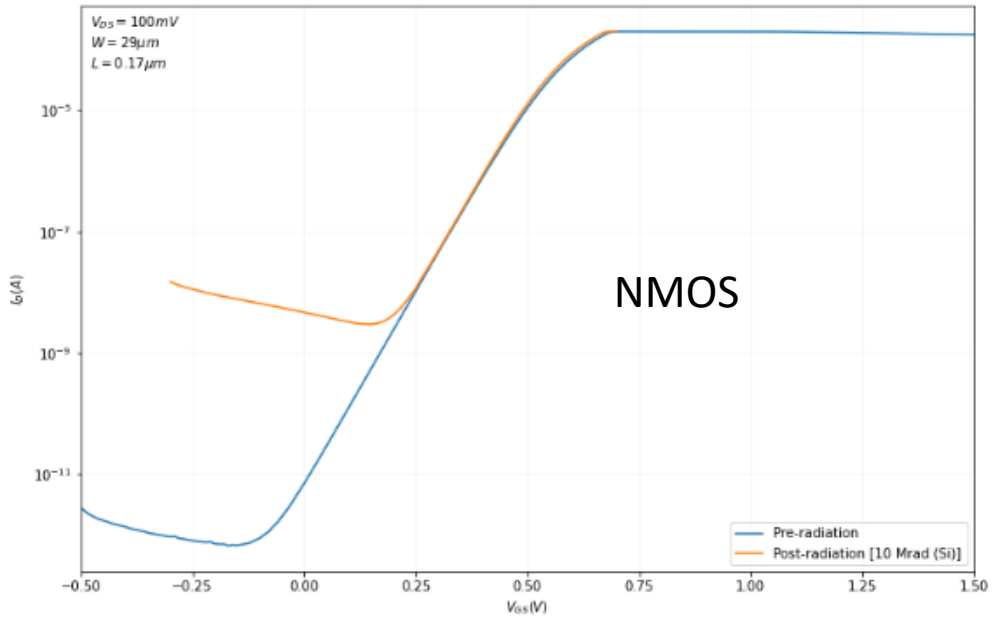
TID (Mrad)

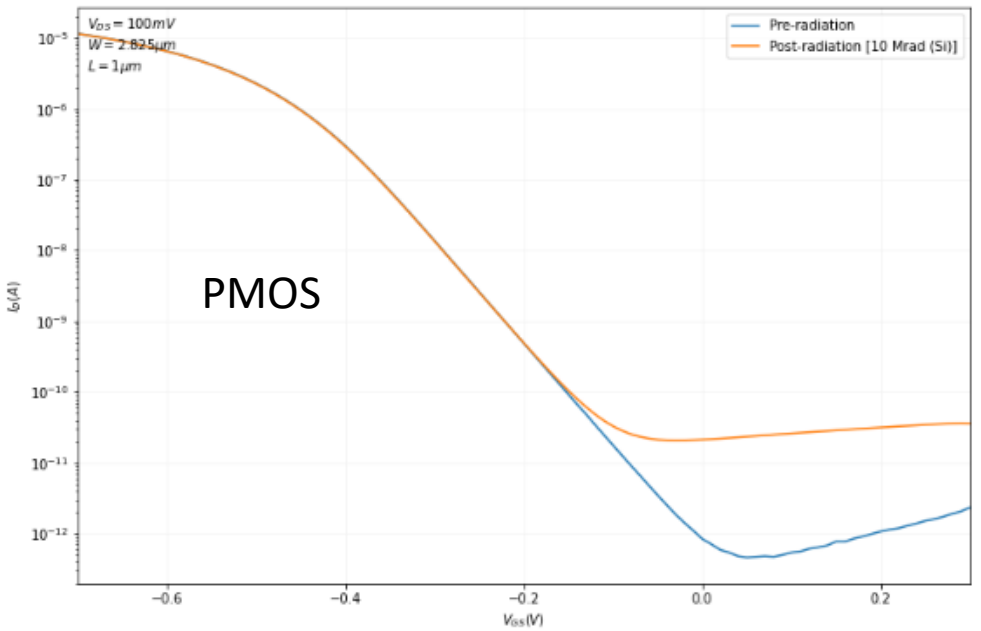
No degradation on the SNDR performance (without calibration) with TID tested up to 2Mrad

Radiation resiliency tests on 28nm process (TID, SEE and Neutron)

TID Radiation Testing for 28nm CMOS Process

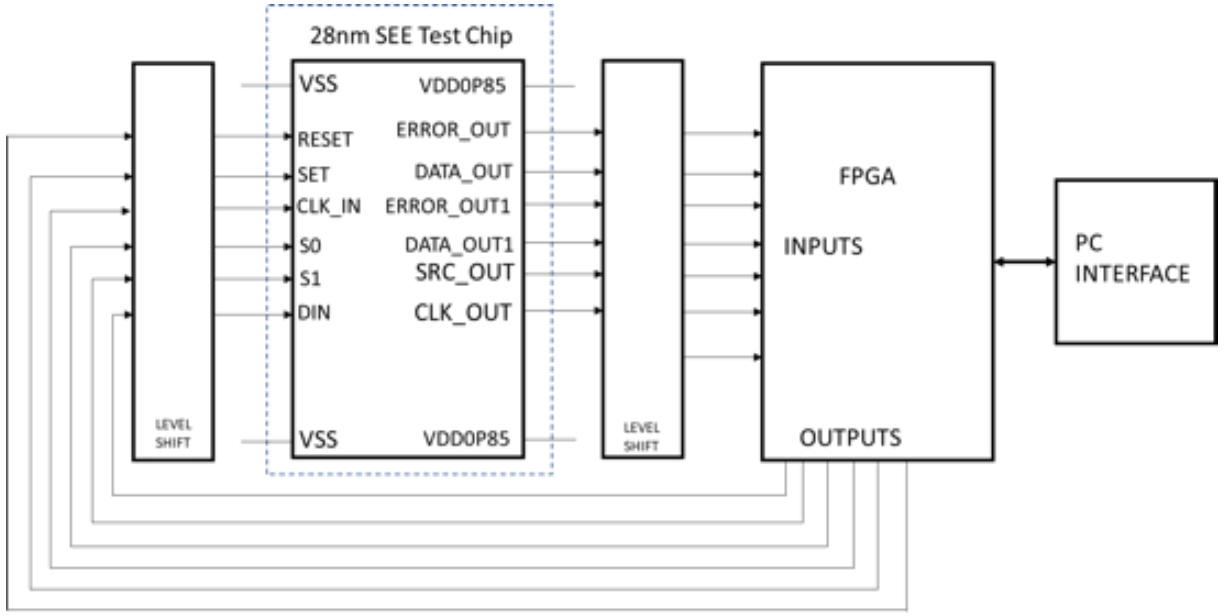
- Test-chips were fabricated with structures for **TID** evaluation, which included NMOS and PMOS devices, as well as diodes.
- TID irradiation was performed at VPT Rad and devices (shipped in dry ice) were characterized in an automated setup at Apogee Semiconductor
- Below are examples of I_D vs. V_{GS} curves for NMOS and PMOS devices before and after radiation (showing low leakage current for subthreshold conditions even after 10Mrad TID).



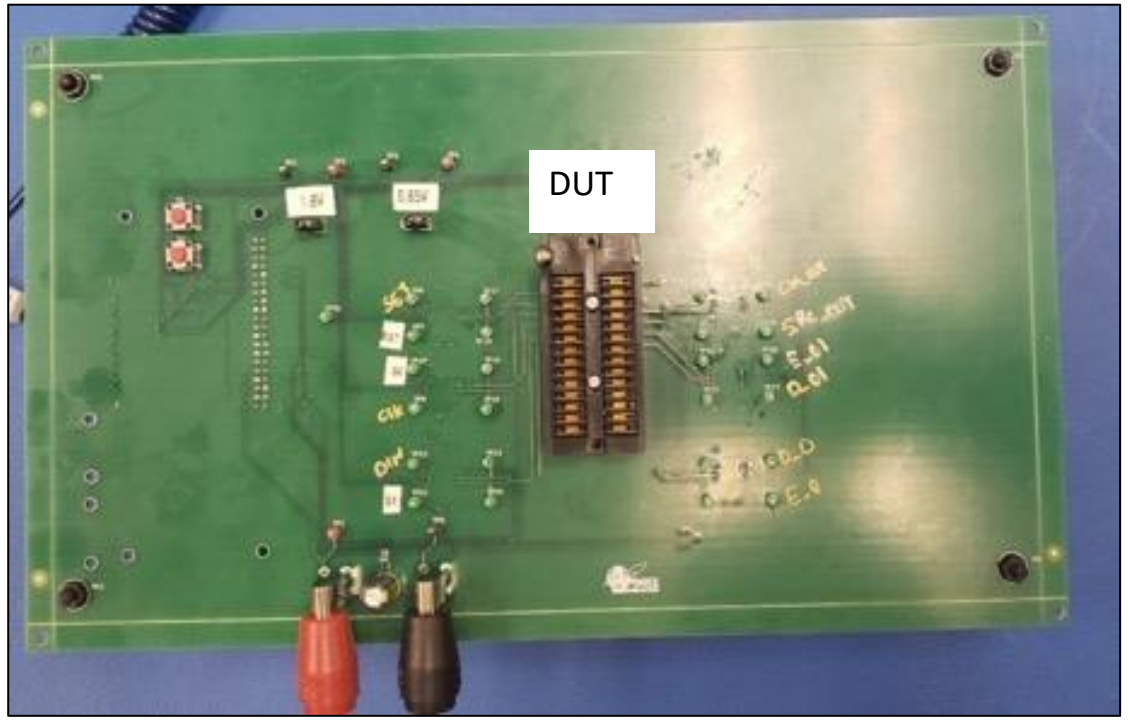


SEE testing on test-chip in 28nm CMOS process

- Test-chip for **SEE** testing based on a chain of over 8000 flip-flops (shift register) and a system for error counting were built and prepared for testing at Texas A&M particle accelerator.
- Testing conducted May 2022.



Block diagram of system built around test-chip for evaluation of SEE performance



Socketed test board for SEE testing of 28nm DUT (FPGA board that interfaces between the DUT and PC is on bottom)

SEL Summary

- Facility Summary:
  - Texas A&M Cyclotron Institute, May 2022
  - 15 MeV/u beam in air
  - Kr at incident (0°) - LET_{eff} = 30.3 MeV·cm^2/mg
- 11 runs @ 80 °C with 2 DUTs
- Flux of 1.0E+05 ions/cm^2·s up to a fluence of 1.0E+07

- Cumulative Fluence across all biasing conditions at 80°C
  - Small Array: 11E+07 (similar to standard cell placement)
  - Large Array: 6E+07 (more substrate and well taps)

- No Latchup observed

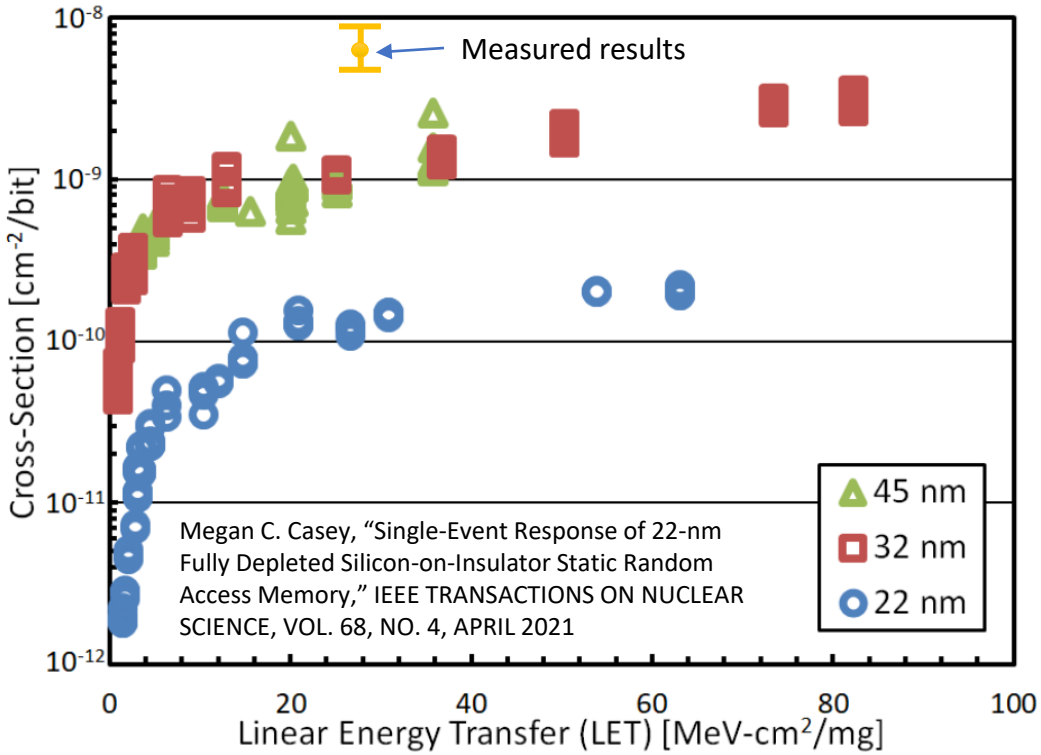
Unit	Run #	Array Exposed	Forcing Conditions	Result
S1	2	Small	Low	No Latchup
S1	3	Small	Checker	No Latchup
S1	4	Small	Inv checker	No Latchup
S1	5	Small	LFSR Cont	No Latchup
S1	6	Small	Inv cont	No Latchup
S3	12	Both	High	No Latchup
S3	13	Both	Low	No Latchup
S3	14	Both	Checker	No Latchup
S3	15	Both	Inv checker	No Latchup
S3	16	Both	LFSR Cont	No Latchup
S3	17	Both	Inv cont	No Latchup

SEU Summary

Unit	Beam	Array Exposed	Forcing Conditions	Errors Small Array	Errors Large Array
S3	8	Small	LFSR	20	Not exposed
S3	9	Small	LFSR	20	Not exposed
S3	10	Small	Checker	44	Not exposed
S3	11	Small	InvChecker	30	Not exposed
S3	12	Small	0's	40	Not exposed
S3	13	Small	1's	32	Not exposed
S3	21	Both	LFSR	32	42
S3	22	Both	Checker	54	35
S3	23	Both	InvChecker	61	41
S3	24	Both	0's	32	31
S3	25	Both	1's	32	28

- All runs conducted at 27°C with Kr ion at effective LET of 30.3 MeV·cm^2/mg
- 8191 bit sequence. Cross-section calculated per bit
- 10 runs, flux 1.0E+04 ions/cm^2·s to a fluence of 1.0E+06

Plot below is for 32nm SRAM is IBM PDSOI – we expect 28nm bulk to be 5 -10x worse, so the result matches well (it is 6x worse well within the margin of error)

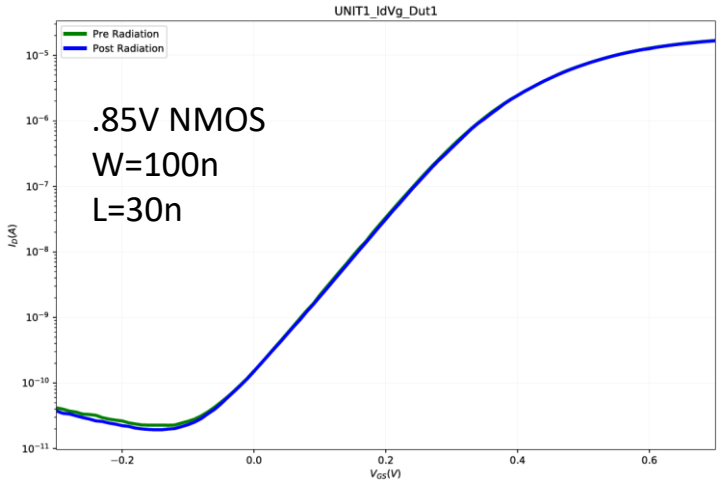


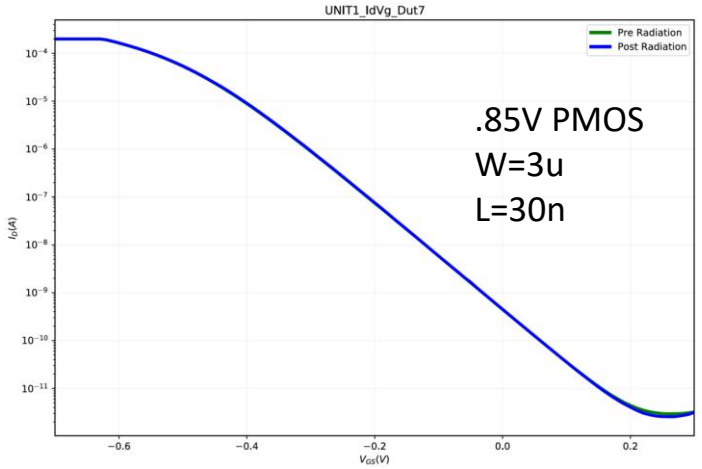
- Small array cross-section across all patterns: **6.94E-09 cm^2/Bit**
- Large array cross-section across all patterns: **6.67E-09 cm^2/Bit**
- Pattern-wise Cross-Section
- Results align with historical data, assumes bulk silicon

Test Chip Neutron Displacement Damage Data

		TEST CHIP 1	TEST CHIP 2	TEST CHIP 3	TEST CHIP 4	TEST CHIP 5
PRE-NEUTRON TESTING	Iddq (mA)	0.2576	0.27176	0.22353	0.18793	0.16064
	Functionality	Pass	Pass	Pass	Pass	Pass

		TEST CHIP 1	TEST CHIP 2	TEST CHIP 3	TEST CHIP 4	TEST CHIP 5
POST-NEUTRON TESTING	Iddq (mA)	0.2466	0.2691	0.2081	0.1765	0.1592
	Functionality	Pass	Pass	Pass	Pass	Pass





- 1MeV Eq. Fluence = 2E+12
- Performed by VPT Rad at UMass Lowell
- No degradation observed

Summary

- Three GS/s 12-bit ADCs have been developed and measured on silicon
  - 2.56GS/s ADC interleaving 8 channels in 65nm
  - Two 1GS/s ADC in 28nm with very low power consumption and silicon area, suitable for integrating multiple channels on a single chip
- The ADC chips have been tested under TID using X-ray up to 2Mrad (Si)
  - Chips were radiation tolerant with no noticeable leakage current increase or performance degradation
- SEE, Co-60 and Neutron tests were conducted on 28nm test chip structures, with positive results.
- Certain targets were not realizable within the budget/schedule, such as the extension to 16 channels and the implementation of a high-speed interface
- Single-channel ADC chip available for evaluation for the NP labs
- Thank you Dr. Shinn, Dr. Manouchehr Farkhondeh, and DOE for the opportunity and support!