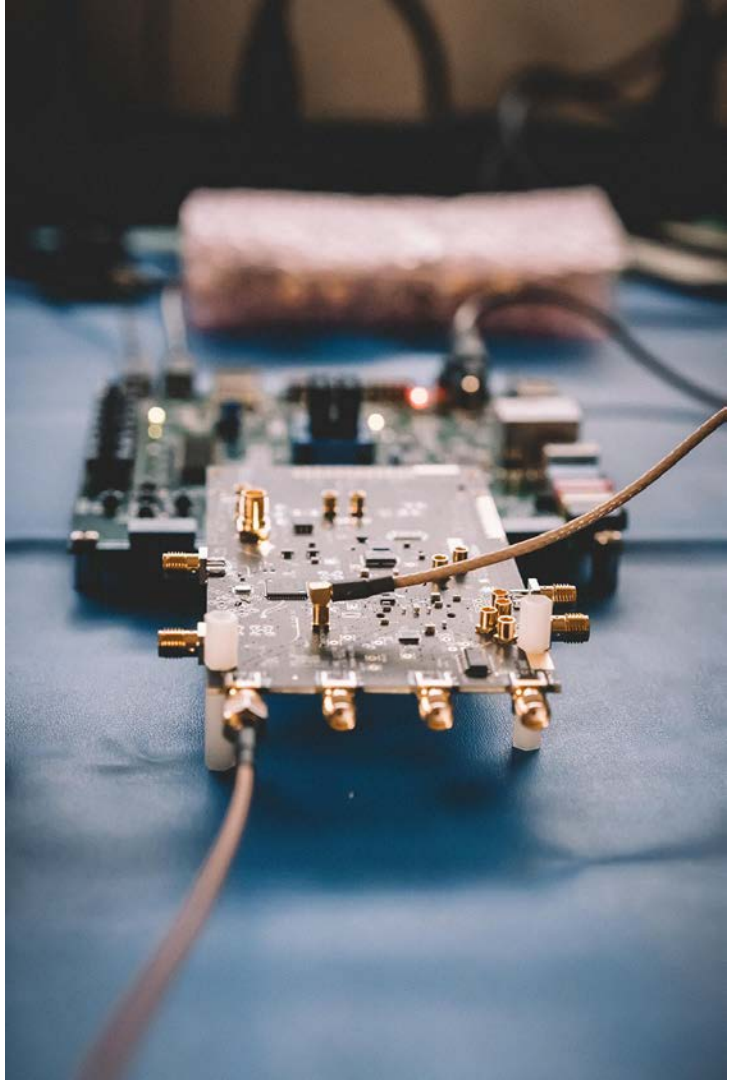


NALU SCIENTIFIC
ENABLING INNOVATION

Design and Fabrication of the HDSoC- High Density Digitizer System-on-Chip

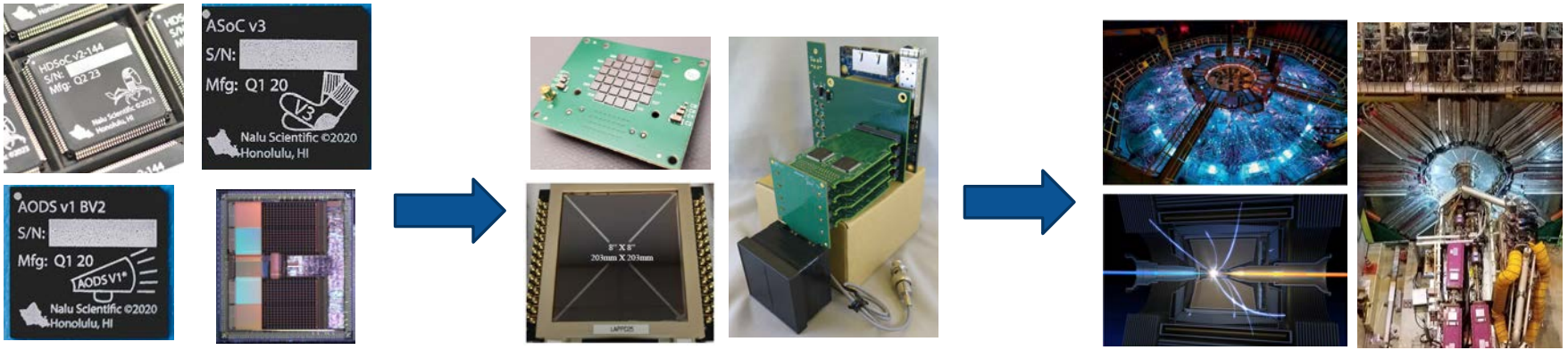
A High channel-density Waveform Digitizer for direct interfacing of optical sensors Application Specific Integrated Circuit (ASIC).

Aug 16, 2023
Luca Macchiarulo, Ph.D.
Senior Engineer at Nalu Scientific LLC

Work funded by DE-SC0020457

NCE: 12/31/23

Core Technology:
Data Acquisition Microchips



1. Front-end Chips:

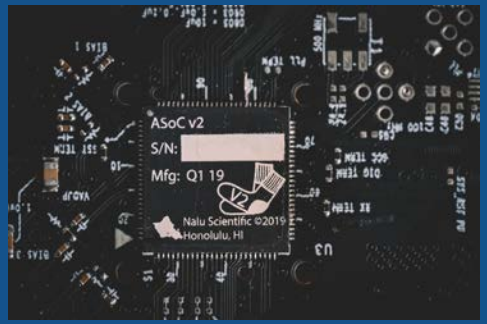
- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

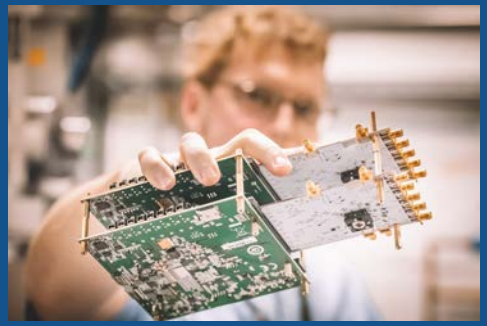
2. Integration:

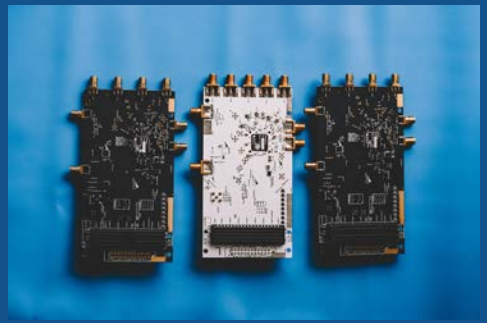
- SiPM
- PMT
- LAPPD
- Detector arrays

3. Applications:

- NP/HEP experiments
- Astro particle physics
- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging







ABOUT NALU SCIENTIFIC

Agile Small Business in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members: 7 PhDs, 5 MSc, 8 BSc
- Access to advanced design tools
- Rapid design, prototyping and testing

Vertically Integrated Team:

Microelectronics	Analog + digital System-on-Chip (SoC)
Hardware	Complex multi-layer PCBs
Firmware	FPGAs, CPUs, Embedded
Software	Data science, GUI, documentation
Scientific	Plasma, medical, physicists, space

Exclusive Distributor Agreement for North America CAEN Technologies Inc.

- Sales of ASICs, eval boards
- Enhanced OEM opportunities

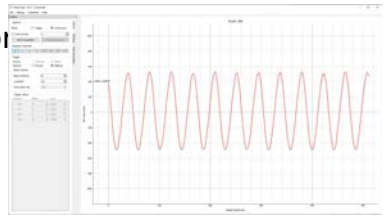
Nalu = 'wave' in native Hawaiian language

NALU SCIENTIFIC
ENABLING INNOVATION

Current ASIC Projects

Project	Sampling (GHz)	BW (GHz)	Buffer (Samples)	Number of Channels	Timing Res. (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-2	0.6	2k	32	80-120	Rev 1 avail
AARDVARC	8-14	2.2	16k	8	10	Rev 4 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5	4k	16	10	Rev 1 avail

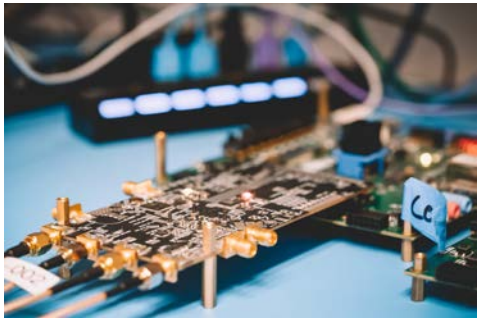
- DOE Phase I/II SBIRs
- Low SWaP-C specialty digitizers for
  - Radiation detection
  - Photonic sensors
  - Time of Flight (ToF)
  - Medical imaging
  - Space
  - Rad hard and harsh
- Evaluation PCBs available
- Extensive suite of software tools
- All microchips and tools available through CAEN Technologies USA



Software

Eval PCB

Microchips



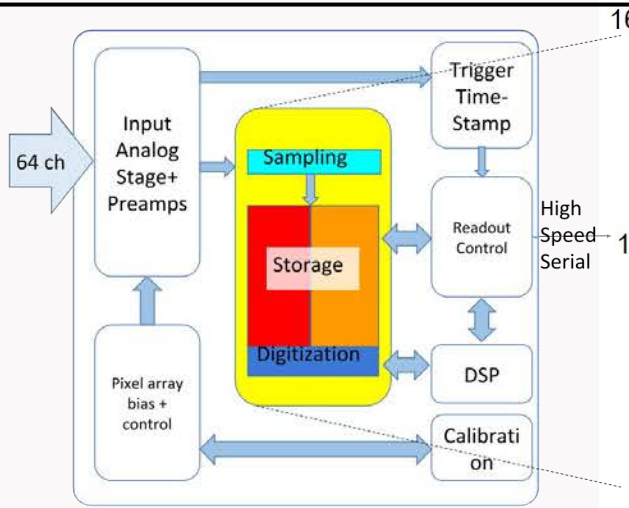
HDSoC project - Summary

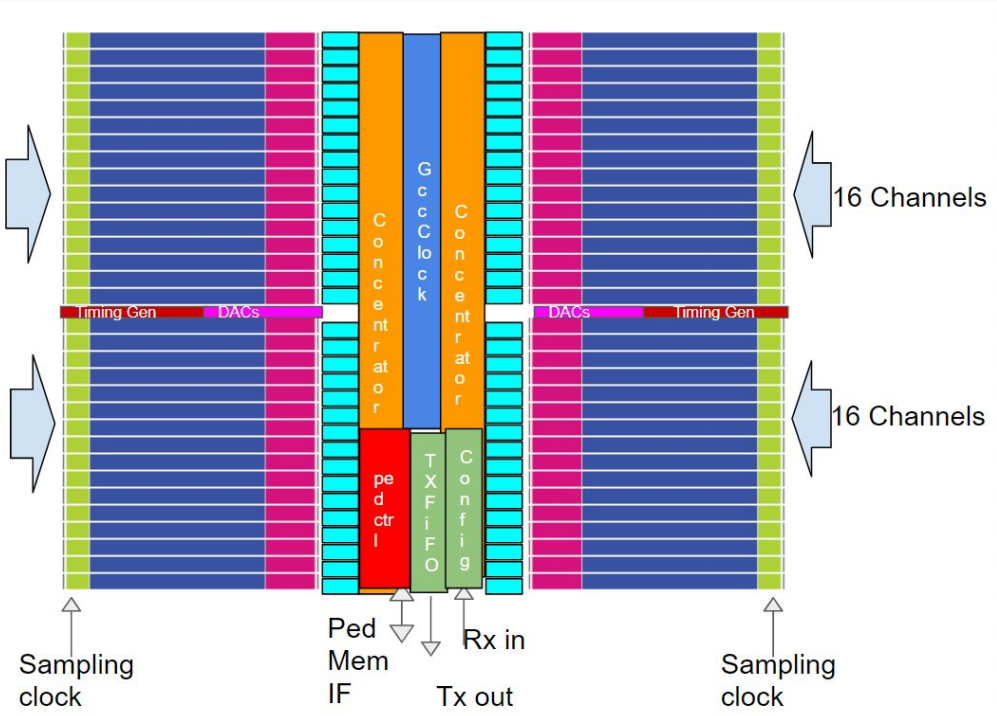
- Part I:
  - Topic Introduction - The need
  - HDSoC concept
  - Rev. 1 design and Fabrication
- Part II:
  - Rev. 1 testing fixtures
  - Rev. 1 initial evaluation
  - Rev. 1 extensive testing
- Part III:
  - Rev. 2 Design
  - Rev. 2 Fabrication
  - Packaging and testing

Part I:
High Density Digitizer SoC - concept and Design

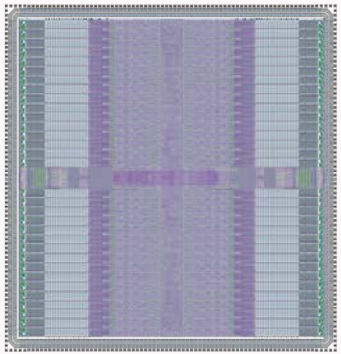
64-Channel HDSoC Block Diagram

"HDSoC": High channel count ASIC with full waveform sampling and data reduction, targeting the increase of readout integration for very high-density detectors such as Silicon PhotoMultipliers (SiPM), MA-PMTs, and LAPPDs - low-cost, low power, solution for experiments with very large channel counts.

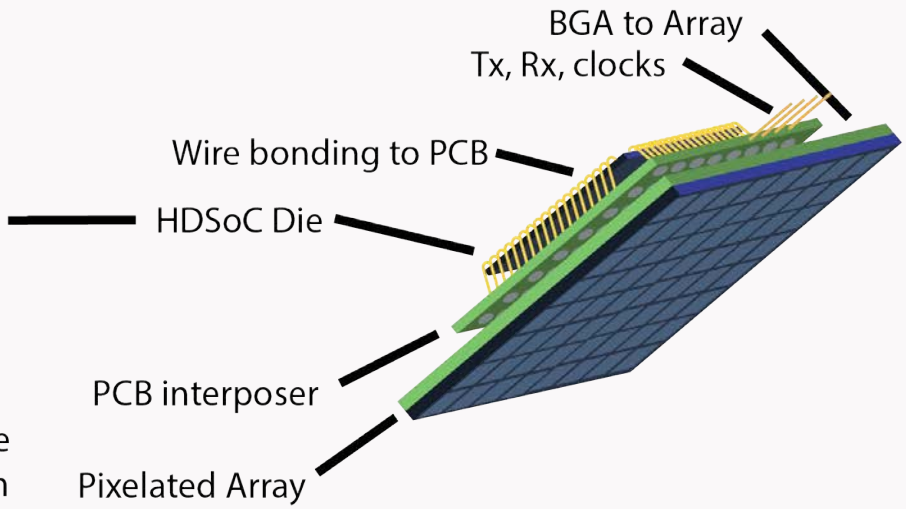




64-Channel HDSoC concept



Nalu Scientific
HDSoC V1 64 channel estimate
64 channel = 7.2 mm x 7.4 mm



HDSoC DESIGN CONCEPT DETAILS

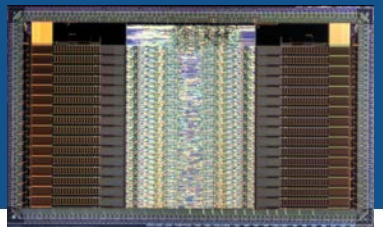
High density waveform digitizer

- High Density: 64 channels (V1:32, V2:64)
- Full waveform sampler and digitizer
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

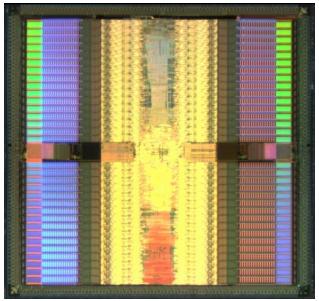
Parameter	Target Spec
Sampling Rate	1-2 GSps
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~2 us (@1Gsps)
Deadtime	0**
Channels	32/64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	20-45mW/ch

- On chip TIA
- Serial interface (up to 500 Gsps)
- Discriminator for self-triggering and zero suppression - exported in dedicated serial stream
- Virtually dead-timeless (buffer virtualization)
- Feature Extraction
- 32 ch and 64 ch proto chips fabricated
- Phase II SBIR almost complete

**If average rates compatible with maximum limits - currently 220kEvents/second



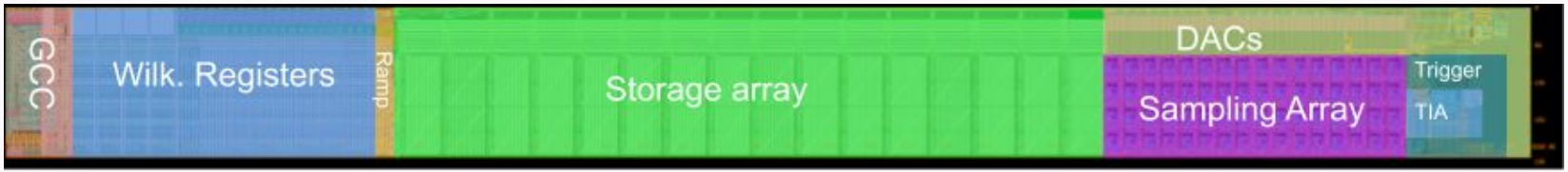
HDSoC v1 die shot

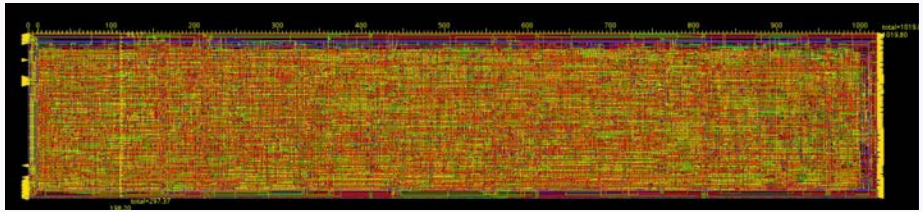


HDSoC v2 die shot

HDSoC Rev. 1 Layout - 32 ch proto

HDSoC Rev. 1 Channel Layout (Mixed signal and digital control)



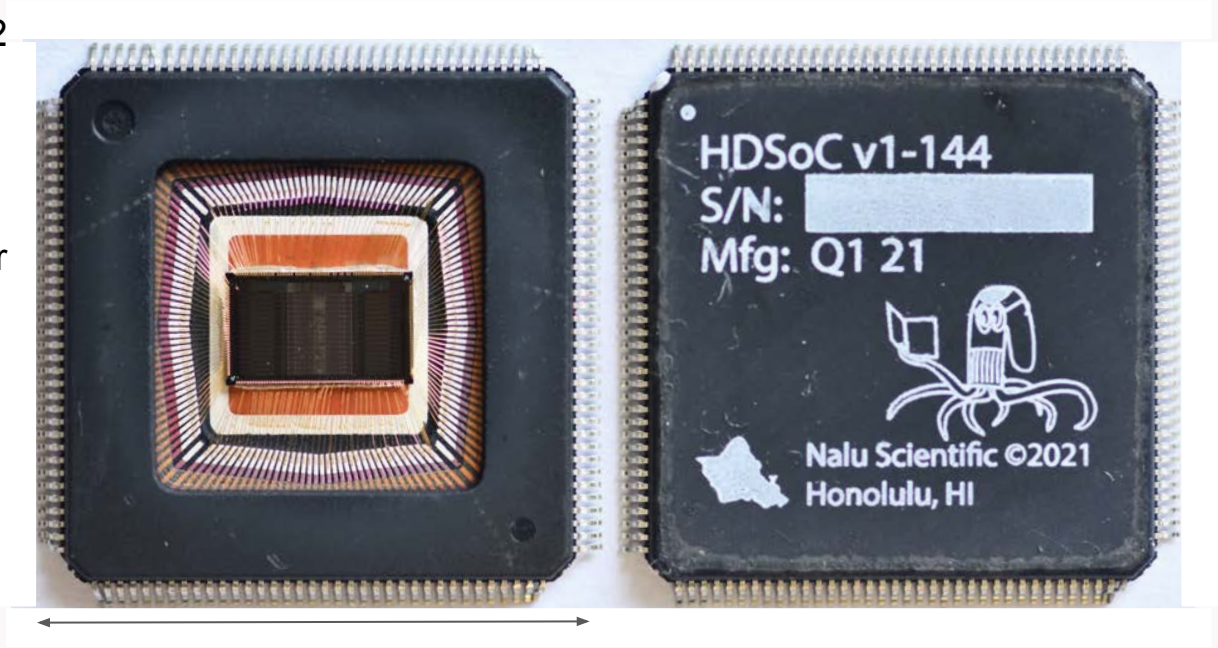


HDSoC Rev. 1 Package

Packaged in QFP144 (22 mm side)
All I/Os connected:

- Serial IF
- Parallel IF

After validation, a smaller package (LQFP128 - 16mm side) with only serial interface can be used. 144 pins are sufficient for the 64 channel device.
A custom package could be used to reduce the footprint.



Part II:
High Density Digitizer SoC Revision 1 Testing

HDSoC v1 specs and Measurements

Specifications	
Sampling Rate	1-2 GSPS
ABW	0.6GHz
Depth/channel	2048 Samples
Trigger Buffer	~2 us
Max rate	14kHz/all channels 220 kHz/hits
Channels	32
Supply/Range	2.5V/0.5-2.0V
ADC bits (stated res.)	12
Timing accuracy	<90ps
Technology	250 nm CMOS
Serial Interface	500MHz
Power	47mW/ch

Confirmed at 1-1.5 GSPS

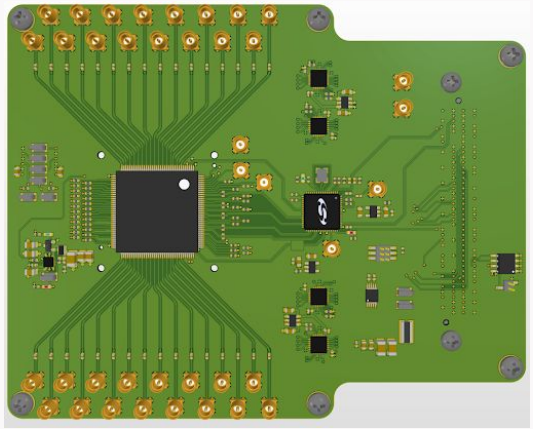
Measured

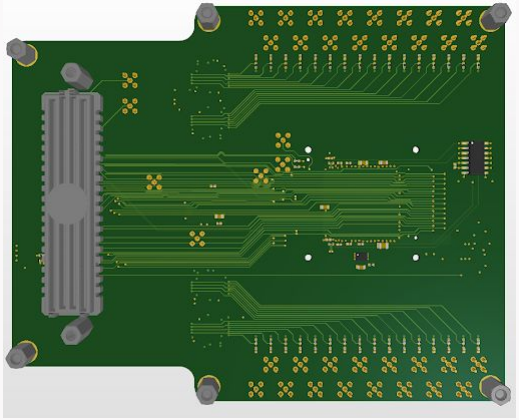
Maximal including header and 8b10b encoding overheads - assumes full readout of 1 window (32 samples) and operation at maximum speed for serial interface (500 Mb/s) and system clock (125 MHz) - current tested limit 13.2kHz @312.5MHz serial interface and 31.25MHz system clock.

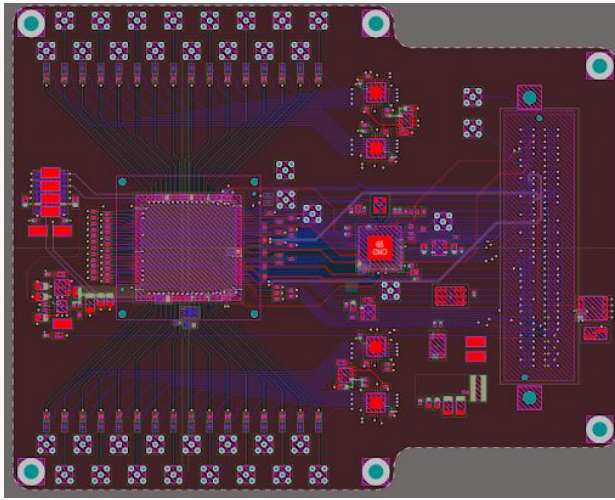
Linear range with ~5 ADC count sigma = 0.8-2.0V

Measured with pulses - currently testing with SiPM
Measured to 312.5MHz
Some sources of extra power identified - reduced in V2
Includes: sensor bias, amplifier, trigger, data transfer.

Test boards Design

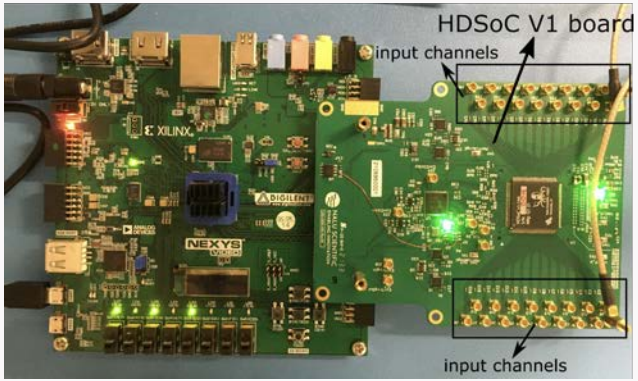






- All 32 channels accessible via MMCX connectors
  - Individual channel biasing
- On board clock generation
- Interface to readout board via standard FMC connector
  - Permits testing of all modes, including serial interface

Test boards setup

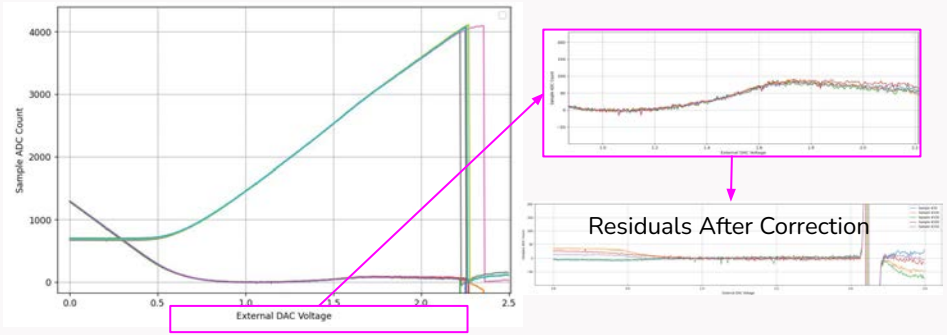


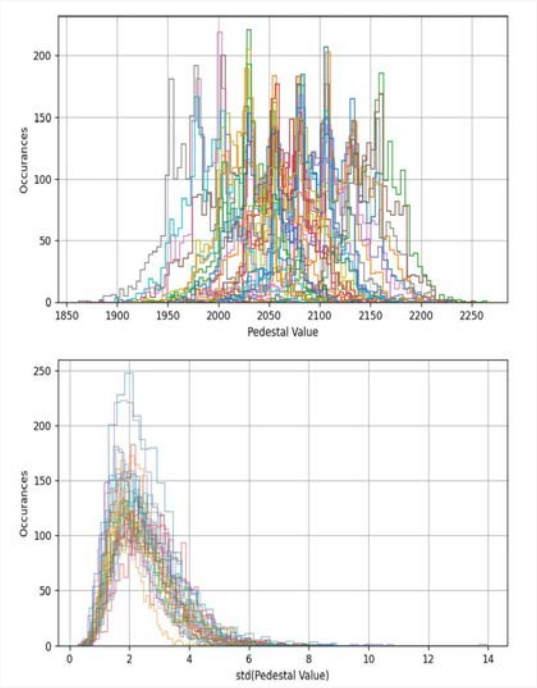
Evaluation Board - now available to interested customers through CAEN - connects to inexpensive readout board with Ethernet connectivity

Test Rig at Nalu - full remote access to boards, including signal sources - a lifesaver during COVID days....

HDSoCv1 Static accuracy

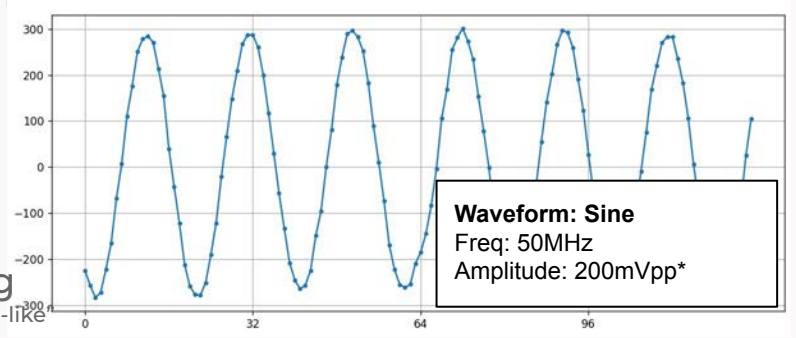
- "Pedestal" evaluation:
  - Due to internal offsets the individual sample values need to be calibrated
  - Statistics on the individual readout for the calibration can be used to estimate the "static error" at bias level -> ~2 ADC count standard deviation
- Varying the input bias to the chip allows studying the overall non-linearity of the conversion - pattern can be calibrated in a large range (1.2V) with residual of ~5 ADC counts (3 ADC counts for a central range of ~200mV)

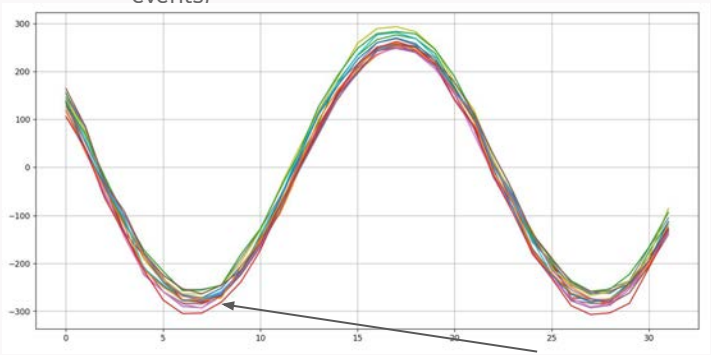


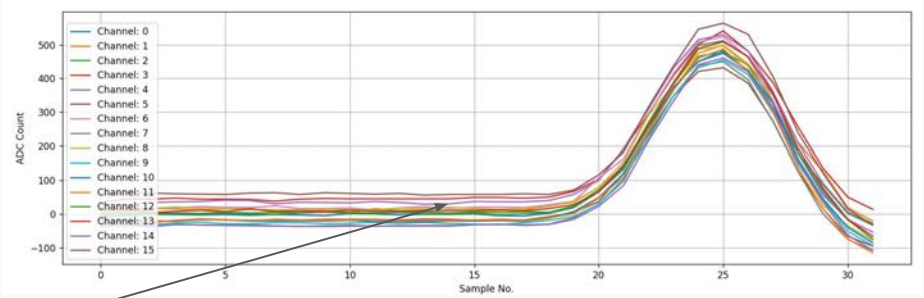


Waveform collection

- Waveform collection, initial calibration
  - Single channel acquisition
  - Sine wave input case
  - Proper timing (“stitching”) across windows
  - First order amplitude calibration
  -
- Multi-channel: synchronized data taking
  - Same signal split into multiple channels (sine and “pulse-like” events)

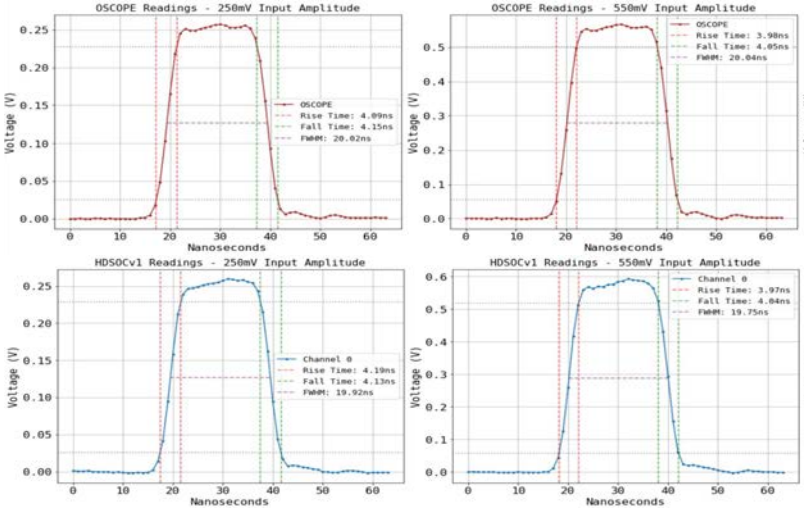




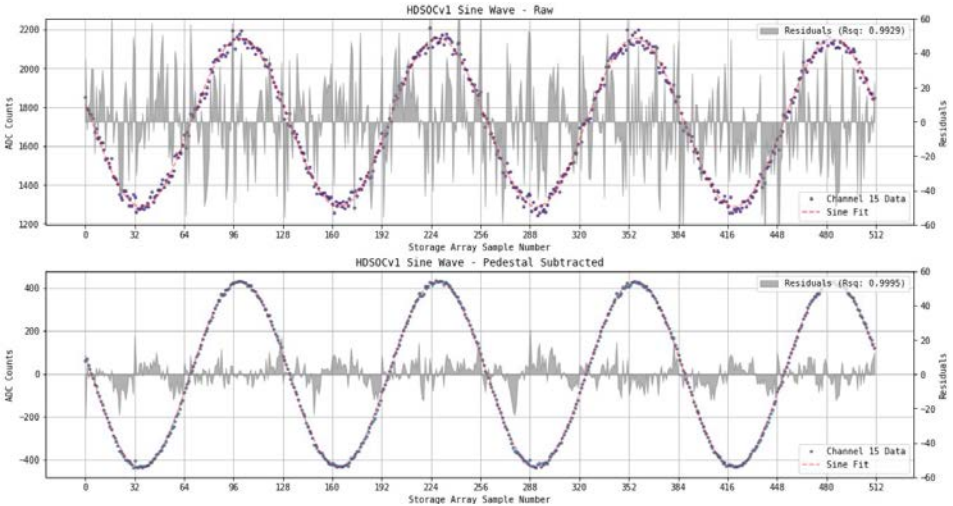


Signal drift resolved - issue with board biasing network

Square Pulse and Sine wave Response



Comparison of square waves captured on an oscilloscope and on a HDSoC channel, with general shape and key parameters (rise time/width/delays) well preserved

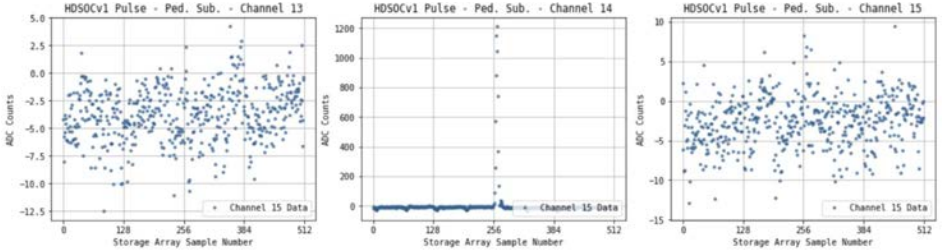


Voltage calibration (Pedestal subtracted) corrects major errors, as shown by wave fitting, though residuals are still present.

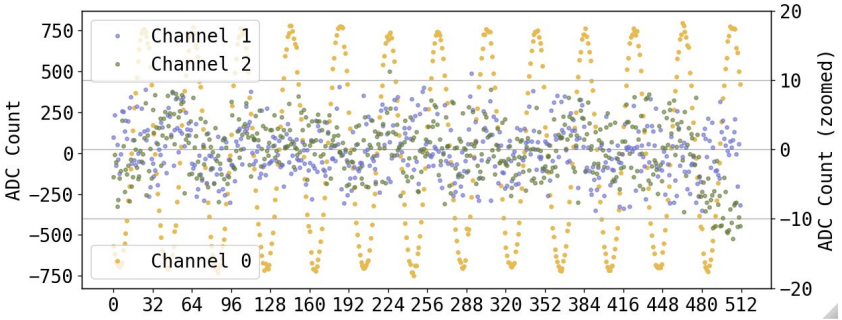
Crosstalk: Pulse and Sine Wave Inputs

No signs of significantly visible crosstalk on neighbor channels

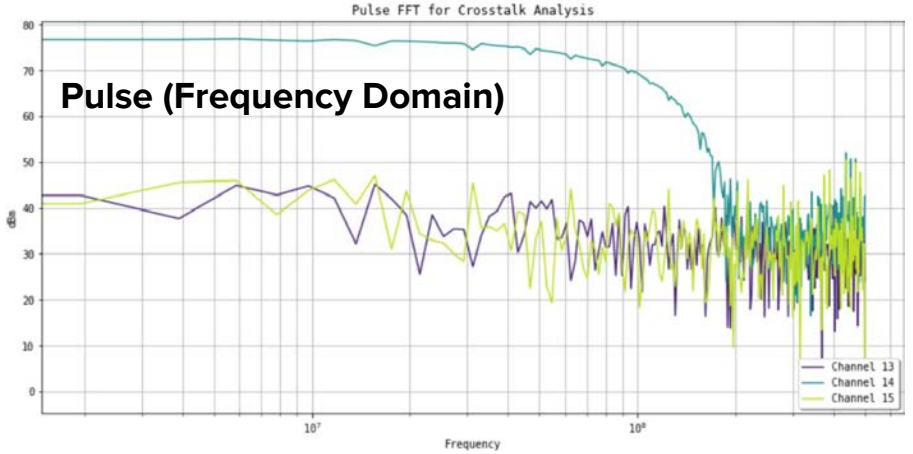
Pulse (Time Domain)



Sine Wave



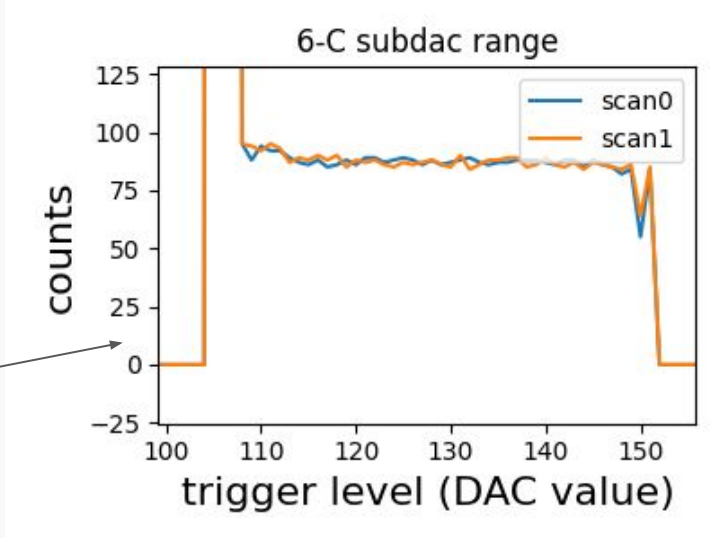
Pulse (Frequency Domain)



Note: signal and noise on difference scales

Digital Partition Features testing

- Different acquisition modes (ROI, self-triggering)
  - Self triggering
  - RoI (zero suppression based on internal thresholds)
- Max sampling rate -> data to 1.5
- Verification of output trigger streaming
- Internal Scalers to perform threshold scans
- Serial interface (functionality and speed)
- Max event rate: 14kEvents/s for all channel readout, 220kEv/s for single channel

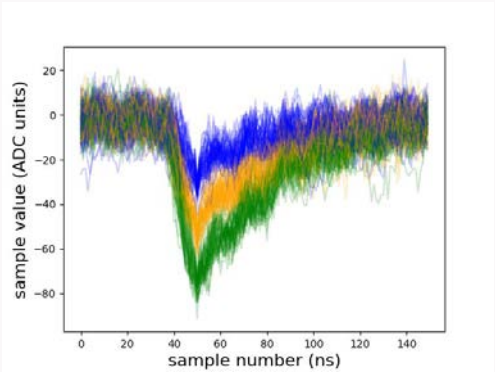


SiPM readout experiments

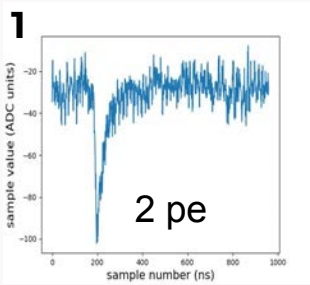
HDSoC V1 connected to a SiPM array. Onsemi J-Series 4x4 array of 3 x 3 mm2 SiPMs. HDSoC V1 channel 0 was set to trigger on signals corresponding to two PEs and above

1. SiPM pulses acquired via HDSoC self-triggering capability
2. SiPM pulse template (via averaging) calculated.

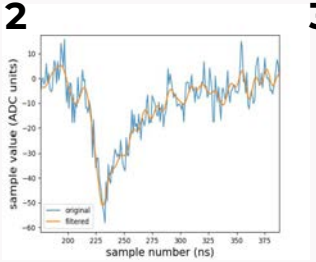
   A spline fit was used to smooth the averaged pulse.
3. Template fit to estimate the amplitude of the pulse peak.
4. Pulse peak histogram shows maxima for 2 PE, 3 PE depending on the trigger threshold - (2, 3 and 4 PEs resolved at 24.4 ± 4.7, 48.2 ± 4.9 and 72.3 ± 4.7 ADC units)



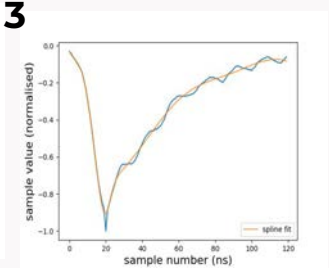
1



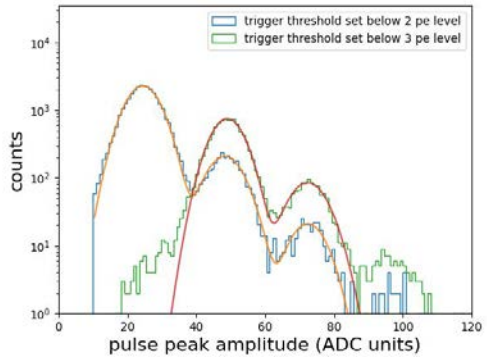
2



3



4



Timing Measurements and calibration

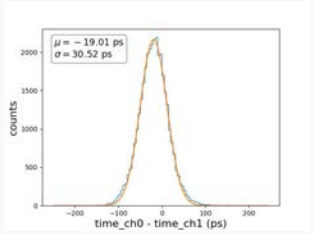
Estimating timing accuracy:

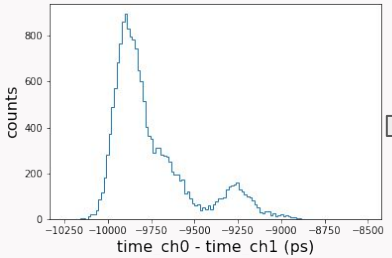
1. Identical Split pulse to two channels: ~30ps - (100 MHz 450 mV unipolar sine burst)

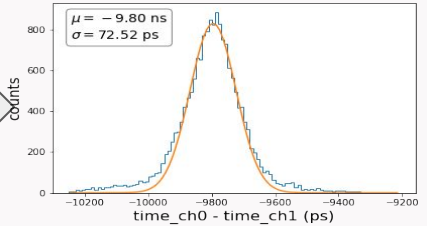
2. Intra-channel accuracy: signal delayed ~10ns: with timing calibration ~ 72ps

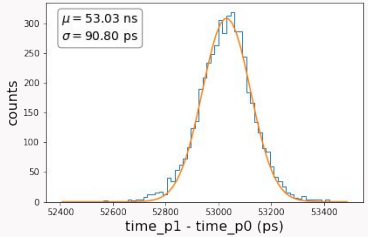
Note: Timing calibration performed using bin-occupancy fraction method on channels 0 and 1

3. Inter-channel accuracy with “far” signals and timing calibration ~90ps





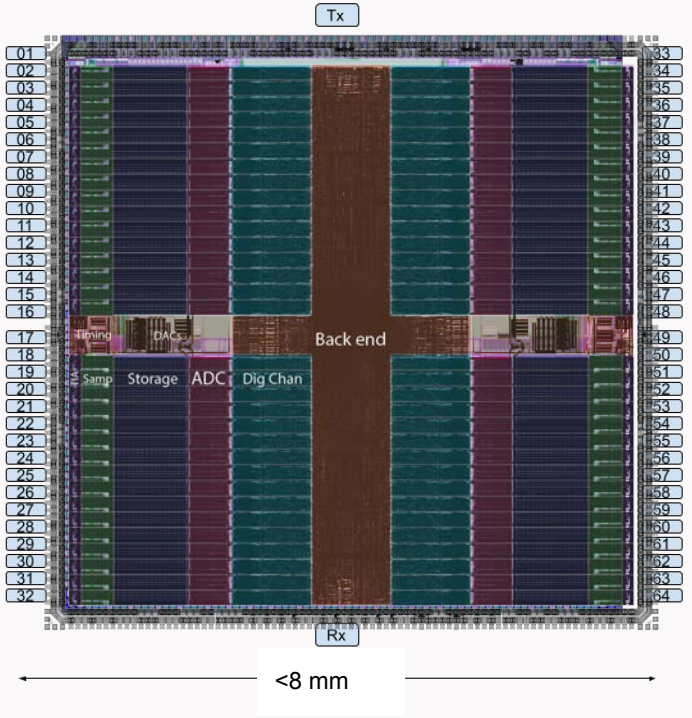




Part III:
High Density Digitizer SoC Revision 2 Design and Fabrication

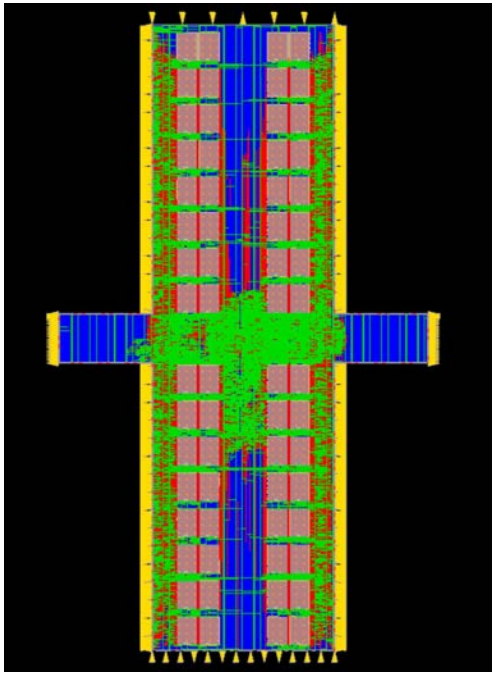
HDSoCv2 design

- HDSoC v2
  - Main improvements:
    - 64 channel device
    - Proper timing up to 2 GSPS
    - Reduced power consumption/chan
      - DAC uniformity
      - Clock gating
      - Triggering and Scalers reduction
    - Improved TIA
      - Correct low BW issue (input stage)
      - Complete redesign to target better integration with SiPMs, controllable internal and SiPM biasing
    - Improved signal quality:
      - Analog/digital isolation
      - Biasing control (current- based)
      - Comparator biasing
      - Power domain separation

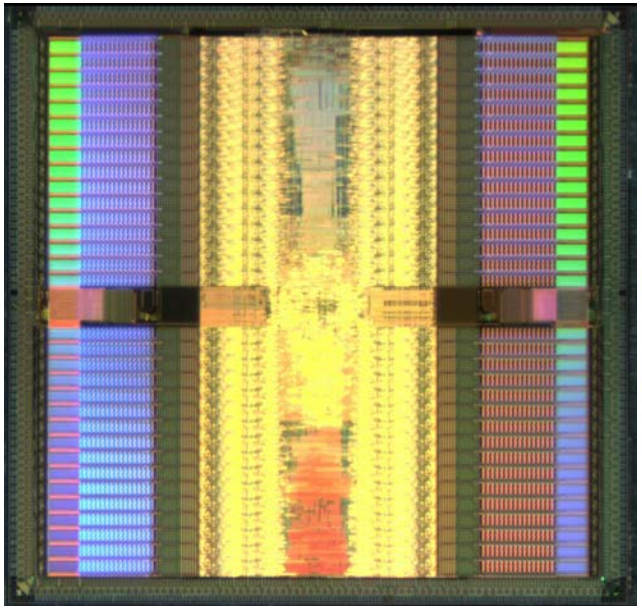


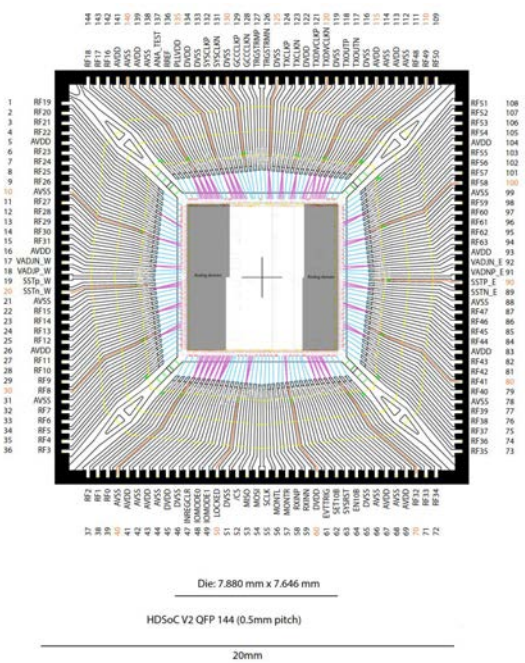
HDSoCv2 - digital Improvements

- PLL for internal generation of clocks:
  - Only one reference clock required for sampling, conversion, readout
- Simplified SPI-like interface for configuration:
  - Rev. 1 - fast LVDS proprietary interface (still available)
  - Rev. 2 - slower single-ended and simpler interface with chaining to reduce system constraints
- Design of internal calibrations SRAM and Feature extraction mechanism to reduce rates - not included in production due to scheduling constraints, but available for next revision.
- Some minor corrections:
  - Added Header information for ROI mode.
  - The internal scalers changes to avoid double counting
  - Added programmable masking for channel
  - External triggering changed from level trigger to edge trigger to simplify the system level requirements.
  - Command to trigger and request a single event

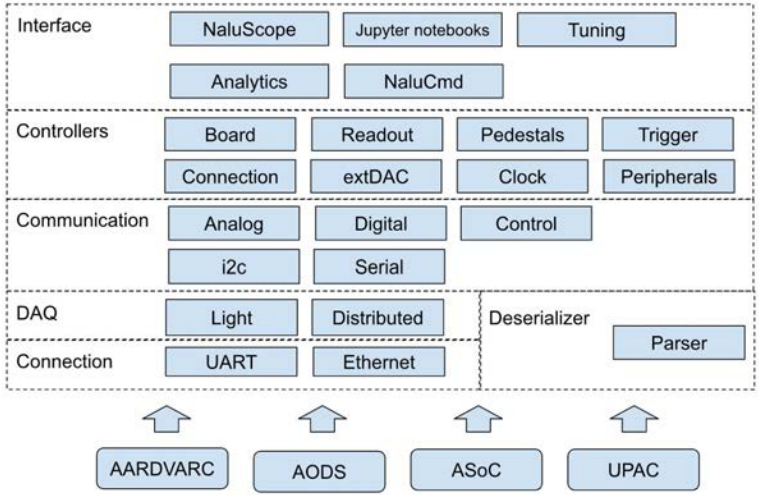


HDSoCv2 Layout - Fabricated die



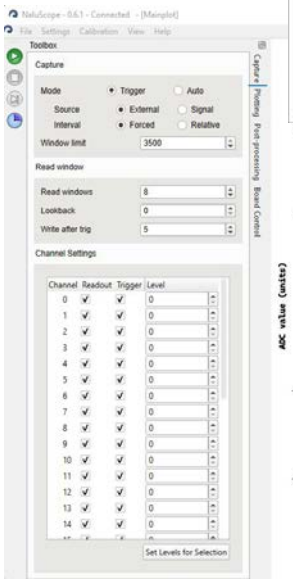


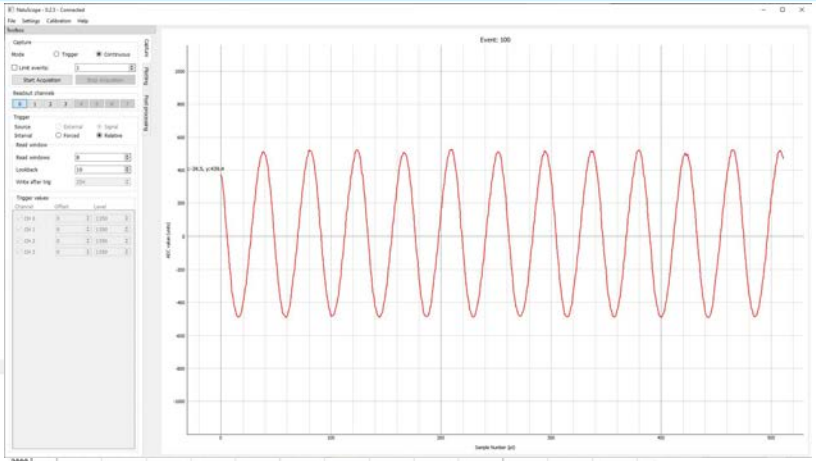
NaluScope Common Software and GUI

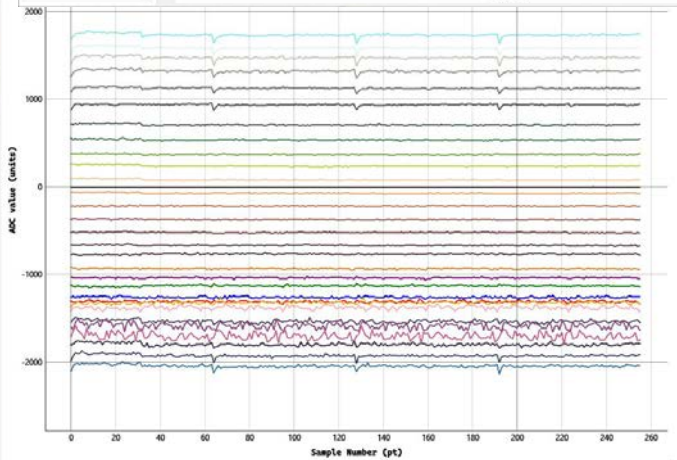


The Nalu software is built around reusable modules, allowing multiple use cases and UIs.

- Windows/Linux PC
- USB interface
- 1GB Ethernet
- GUI, CLI interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage







Conclusions and future work

- **HDSoC v1**
  - All channels functional
  - Proper multi-window, multi-channel acquisition, self triggering, output streaming
  - Some issues with noise and power/ TIA BW
  - Test boards available through our U.S. distributor, CAEN - together with FW/SW/GUI and support.
- **HDSoC v2**
  - Fabricated - currently gearing up for testing
  - HDSoC v1/2 may be used in beam tests for various EIC sub detectors
  - Opportunity to implement EIC specific (sensor, backend) needs in future revisions or branches
- **HDSoC is a novel streaming readout capable, waveform- sampling ASIC**:
    - Low Cost, low power, scalable
    - Works with a variety of sensors arrays: GEMS, TPCs, SiPMs, MA/PMTs, MCP PMTs
    - Tracking and PID
    - Portable radiation imaging systems
    - Compact, high-efficiency neutron scatter cameras for non-proliferation national security missions.
  - Various conference presentations and live demos

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