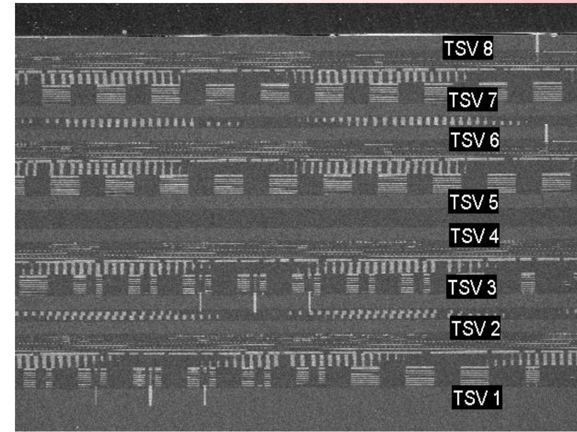
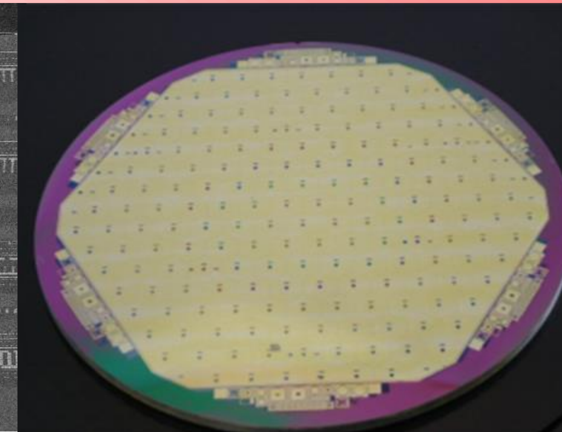
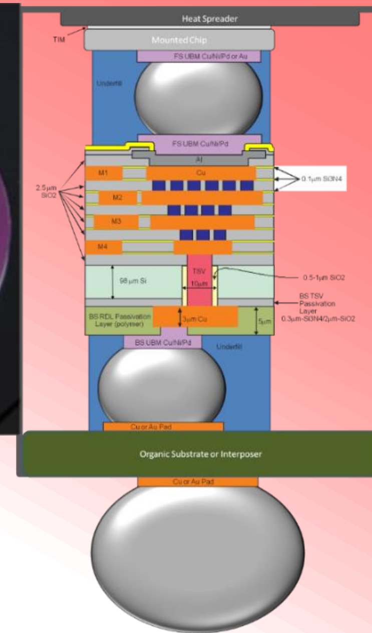
NHanced Semiconductor – Foundry Services







Robert Patti
NHanced Semiconductors, Inc.
1201 N Raddant Rd.
Batavia, IL 60510-4213
(630) 561-6813 Cell
rpatti@nhanced-semi.com

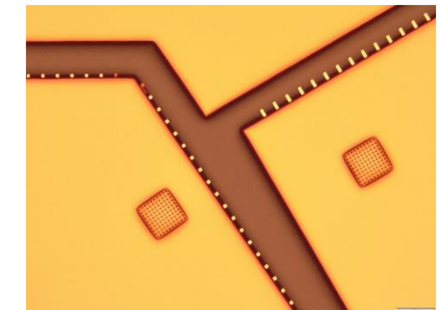
NHanced Product Services:

- 2.5D/3D assembly (die to wafer, die to die, and wafer to wafer)
- Combining Si, GaN, GaAs, GaSb, SiC, InP, LiNbO3, InGaAs, and other materials
- Oxide and hybrid bonding
- High performance silicon, glass, fused silicon, and metal interposers with up to 8 RDL layers
- Quilt packaging
- Transfer printed 2.5D
- TSV insertion
- Thick and thin wafer processing
- Si sensor fabrication
- Microfluidics for medical and liquid cooling applications
- Wafer UBM, bumping, and copper pillar
- Custom foundry BEoL

Site Capabilities:

- 25,000 sq ft facility
- 7,000 sq ft clean space (class 100)
- Fab processes include photo, etch, metallization, dielectrics, bonding, wafer thinning, and CMP
- 75mm, 100mm, 150mm, and 200mm wafer processing
- I-Line and 1X lithography in-house
- Copper, nickel, aluminum, tungsten, titanium, and numerous other special metals
- Oxides, nitrides, and other specialty dielectrics
- Wafer-to-wafer, die-to-wafer, and die-to-die bonding
- Certifications

  ITAR
  ISO 9001-2015
  DMEA TRUST in progress



SC0020461
CMOS Integrated With Float Zone Pixel Sensor
Topic No: 32.c – Next Generation Pixel Sensors

08/16/2023

Robert Patti

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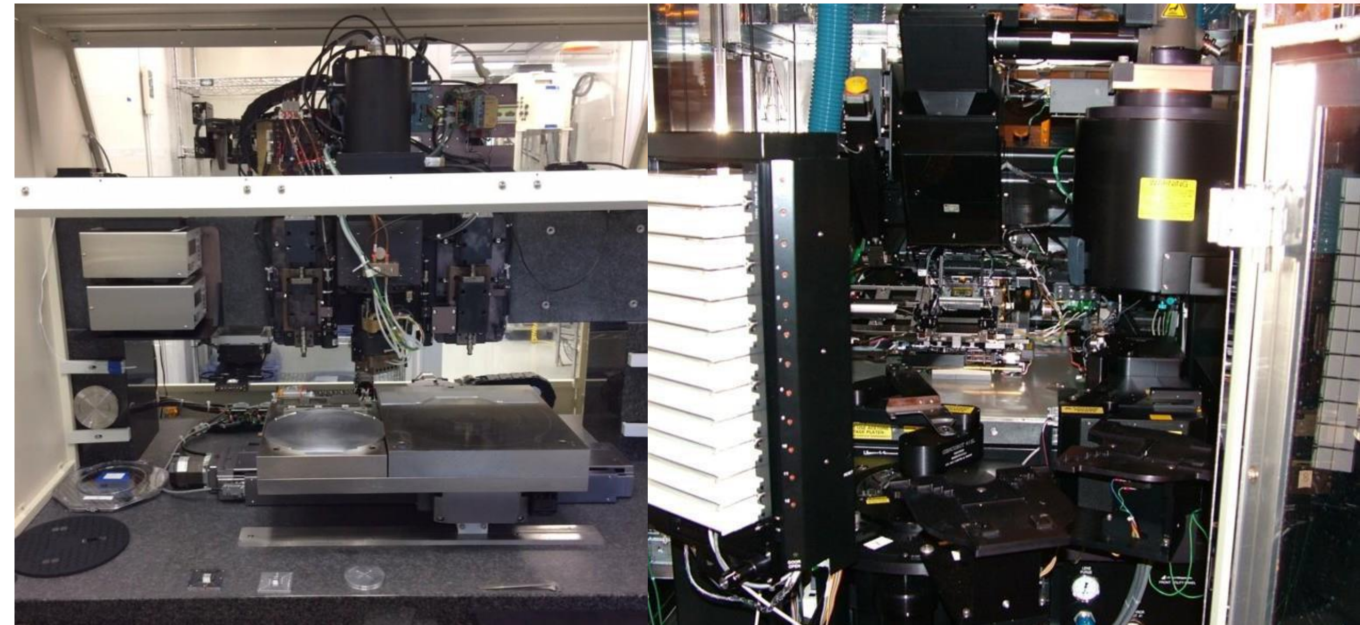
NHanced Semiconductors

- Batavia, IL: Design and Test
  - Complete front end and backend design down to 12nm
  - Supports AI and HPC systems development
- Morrisville, NC: Foundry
  - 3”-200mm
  - Copper, Al, Ni BEoL
  - Interposers
  - 2.5/3D Integration
- Odon, IN: Packaging
  - Packaging
  - RadHard Microelectronics
- New Fab: L/MVM
  - 55,000 sqft cleanroom
  - ~5,000 wafers/month



NHANCED SEMICONDUCTORS

Background: Next Generation Pixel Sensor

NP has a growing need to develop particle tracking devices with:

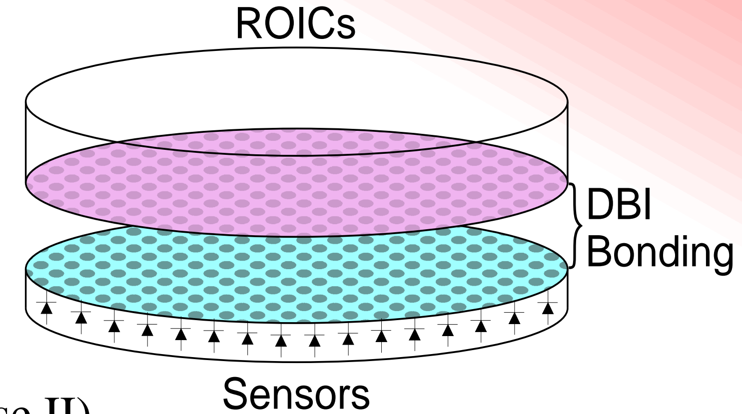
1. Improved position and timing resolution for more accurate tracking
2. Faster speed to limit event pileup
3. Lower mass sensor to minimize electron scattering, leakage (increased shot noise) and trapping distance (decreased signal)
4. High radiation tolerance to survive the conditions of high luminosity colliders
5. Lower power and lower fabrication cost

Background: Technology Overview

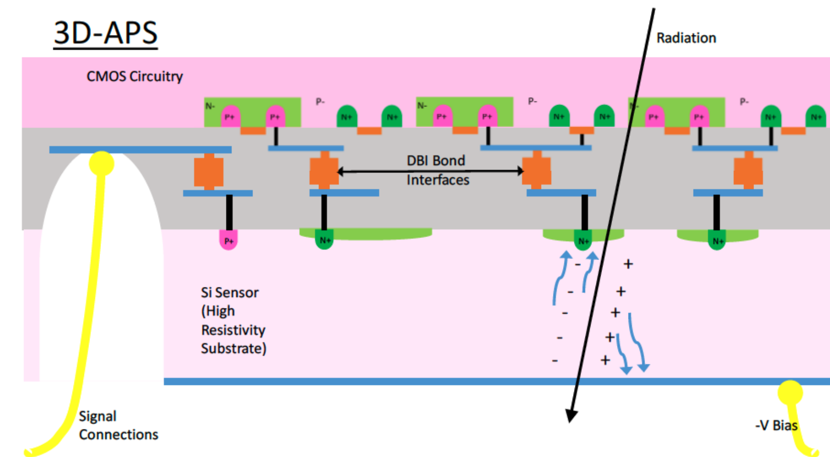
Technologies	Pros	Cons
Monolithic Active Pixel Sensors (MAPS)	Simple and cheap	• The sensor device can't be fully depleted • Can't use high resistivity material • Lower granularity
SOI-MAPS	• ROIC and sensor separation • High granularity • Fast	• Expensive process • Back diode effect • Sensitive to TID
LGAD	• Complete separation of ROIC and sensor • picosecond timing resolution (only limited to Laudau noise) • Lower power	• Low fill factor • Low granularity • Gain sensitive to radiation
3D Advanced Hybrid Detector (3D-AHD)	• Complete separation of ROIC and sensor • High granularity • High fill factor • Could achieve picosecond timing resolution	• Higher power than LGAD • Need to be demonstrated

Background: 3D-AHD Development

Sensor tier:
Physical implementation (Phase I)
Fabricated at NHanced on high resistivity silicon wafer (Phase II).
Thinned down to 100um to 20um at NHanced (Phase II).

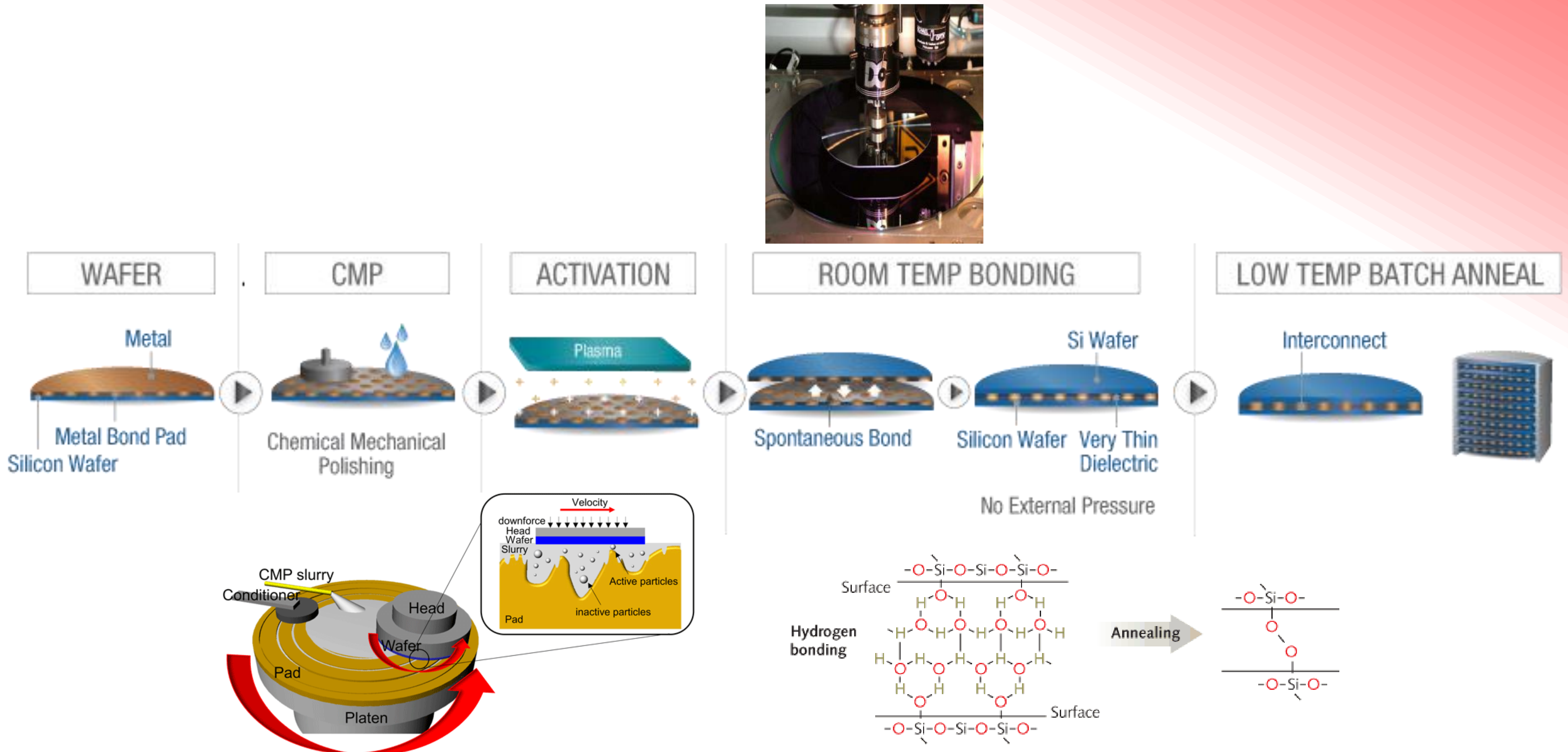


ROIC tier:
Proof of concept and designed by NHanced and Fermilab (Phase I and Phase II)
Physical implementation (Phase II)
Fabricated with RHBD (Phase II)



3D-AHD detector:
Final integration at NHanced fab (Phase II)

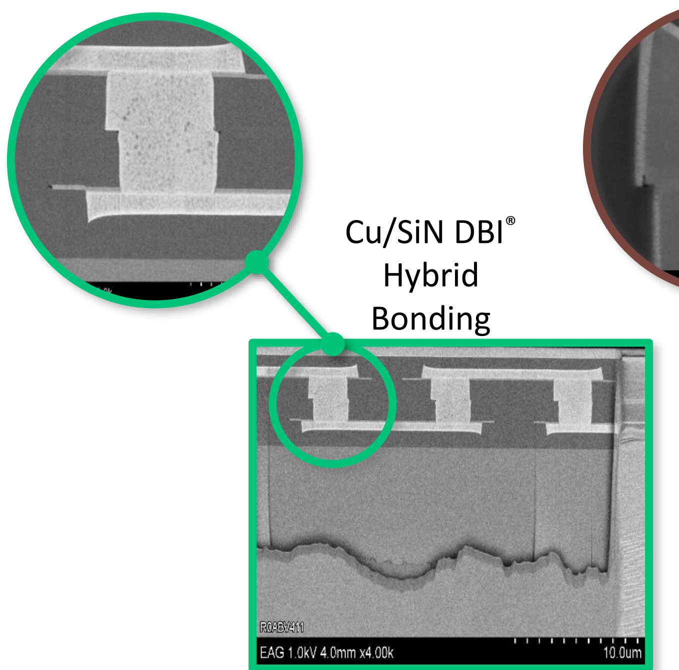
DBI®: Low Temperature Hybrid Bonding Process



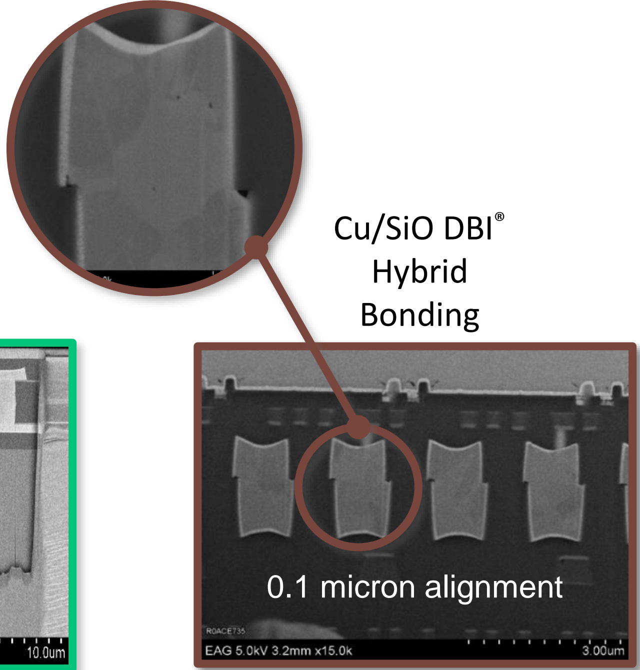
Jihoon Seo / Materials Research Society

NHANCED SEMICONDUCTORS

Hybrid Bonding Interconnect Pitch Scaling

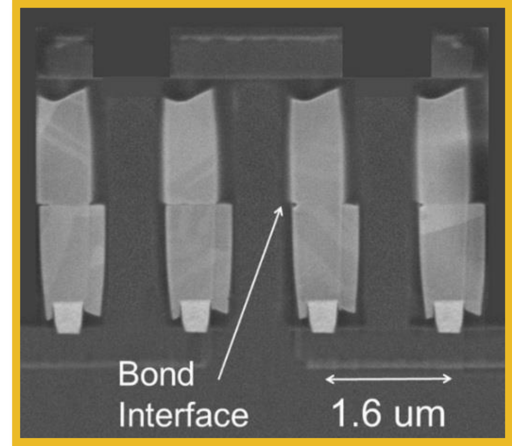


10 μm DBI® pitch, 300℃



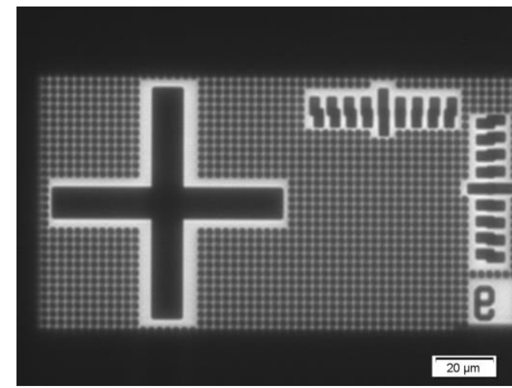
1.9 μm DBI® pitch, 300℃

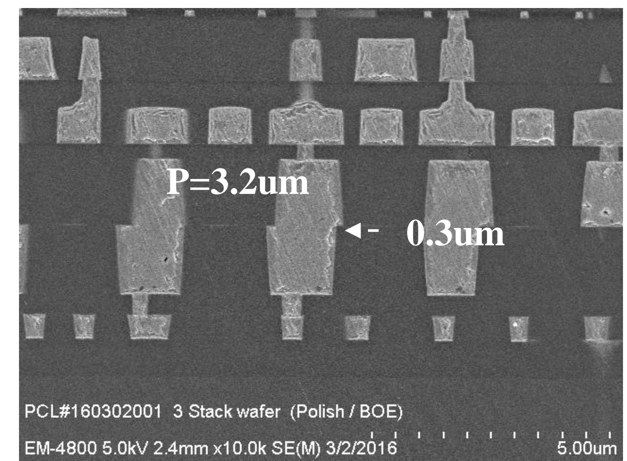
Scalable To < 1um Pitch



1.6 μm DBI® pitch, 300℃

- 3sigma < +/- 1um misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding





Induced current – Simple example – X-rays

The current pulse reflects charge motion deep in the detector

Data from 3dPixel_2m_400.log

Central pixel

Current #1 (A)
Current #4 (A)
Current #5 (A)

Initial Current Spike

Edge neighbor (diffusion collected charge)

Corner neighbor 0 collected charge

1.4×10^{-05}, 1.2×10^{-05}, 1×10^{-05}, 8×10^{-06}, 6×10^{-06}, 4×10^{-06}, 2×10^{-06}, 0, -2×10^{-06}

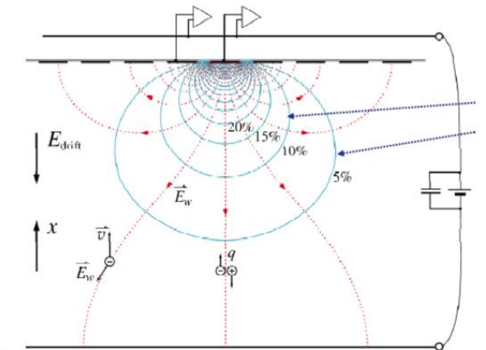
0, 1×10^{-09}, 2×10^{-09}, 3×10^{-09}, 4×10^{-09}, 5×10^{-09}, 6×10^{-09}, 7×10^{-09}

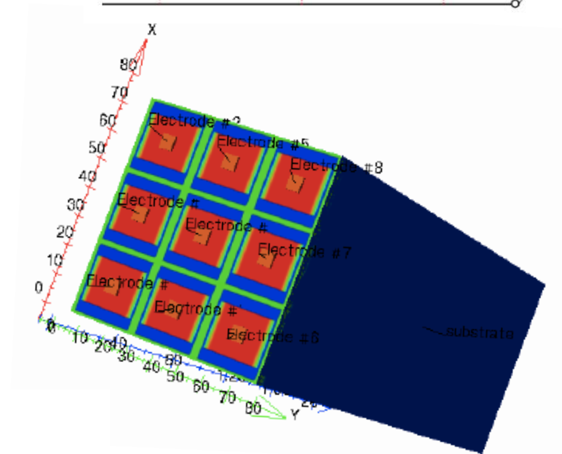
Ramo's theorem

$$i = -q\vec{E}_w \times \vec{v}$$

$$Q_s = \int i\,dt = q\int \vec{E}_w d\vec{x}$$

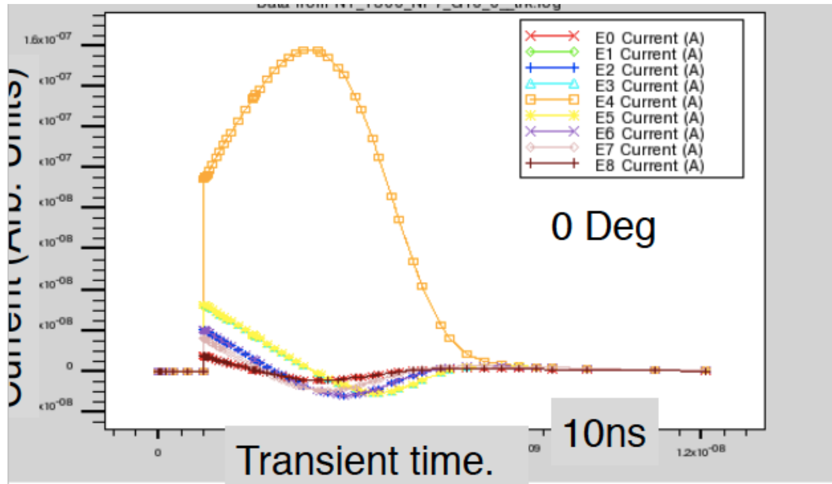
$$Q_{1\to2} = q(V_{w2} - V_{w1})$$

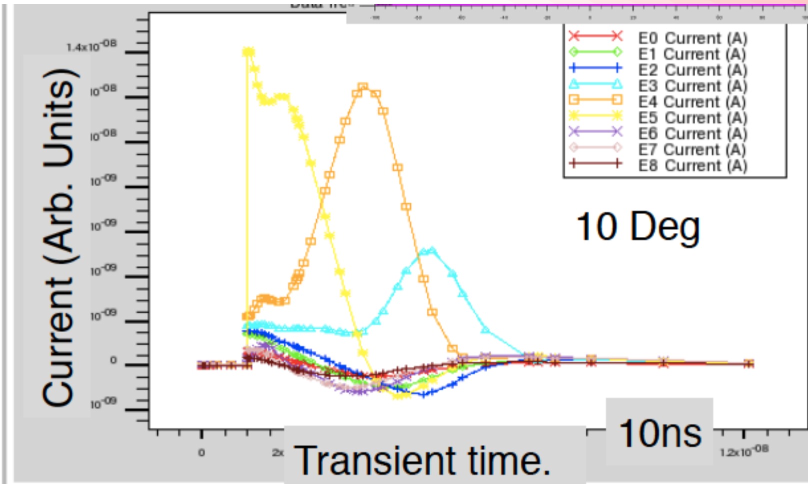




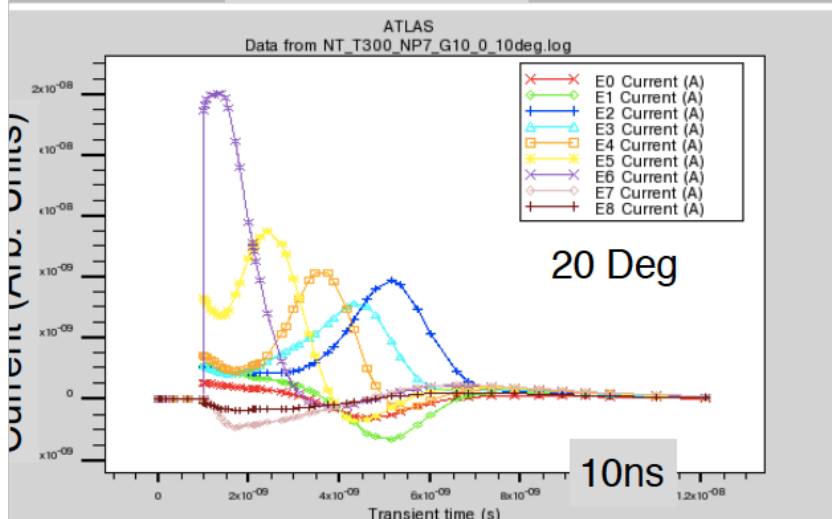
NHANCED SEMICONDUCTORS

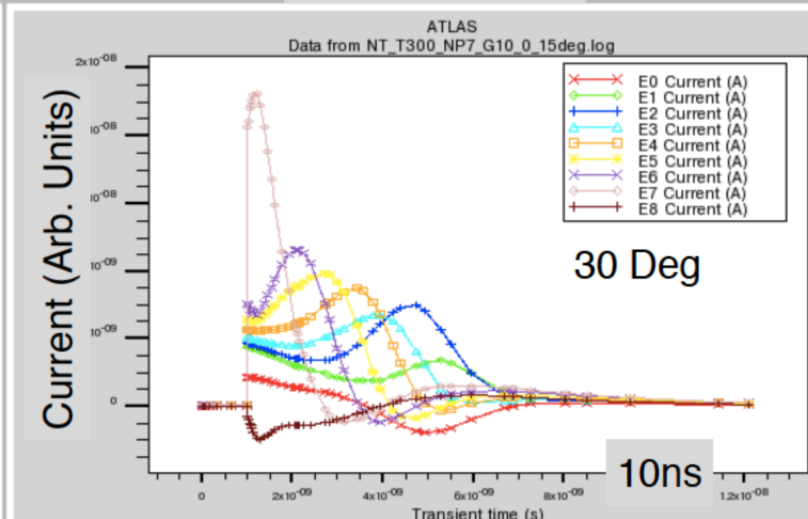
Induced current - MIPs at various angles:





Ron Lipton
FermiLab





NHANCED SEMICONDUCTORS

Proof of Concept of Angular Resolution possibility

- We found angular resolution is possible for high enough pixel area/thickness ratio

  -> Increasing the pixel size specification to 25um x 200um (smaller size along the axis perpendicular to the field).

  -> Increasing the thickness of our simulated substrate to 200um to maintain good S/N ratio for every electrodes and angles.

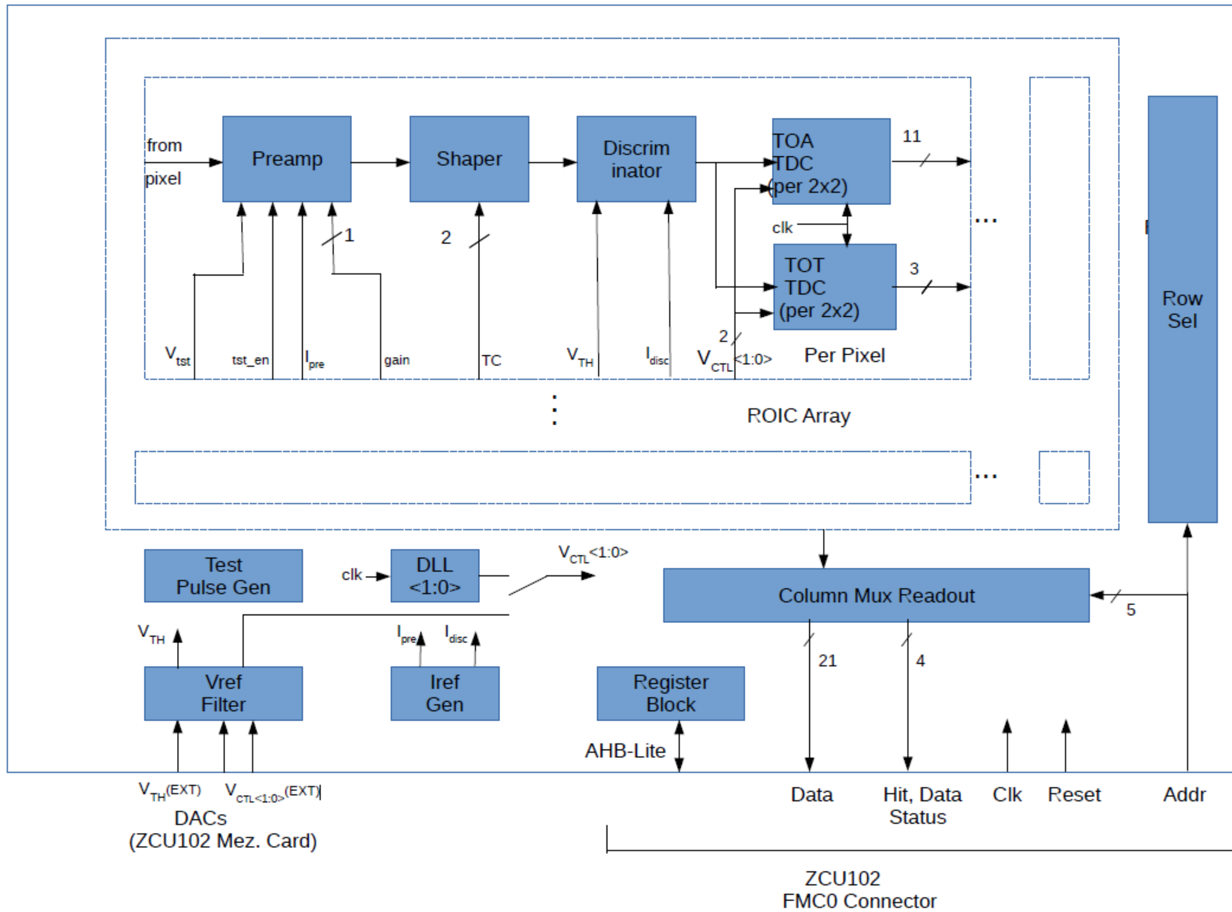
- Angular resolution is only possible if we maintain the integrity of the shape of the current pulse. This concept is fundamentally enabled by the new trans-impedance amplifier as opposed to the more typical Charge Sensitive Amplifier (CSA) scheme.

  -> Requires a more complicated front end design (stability, speed, noise)

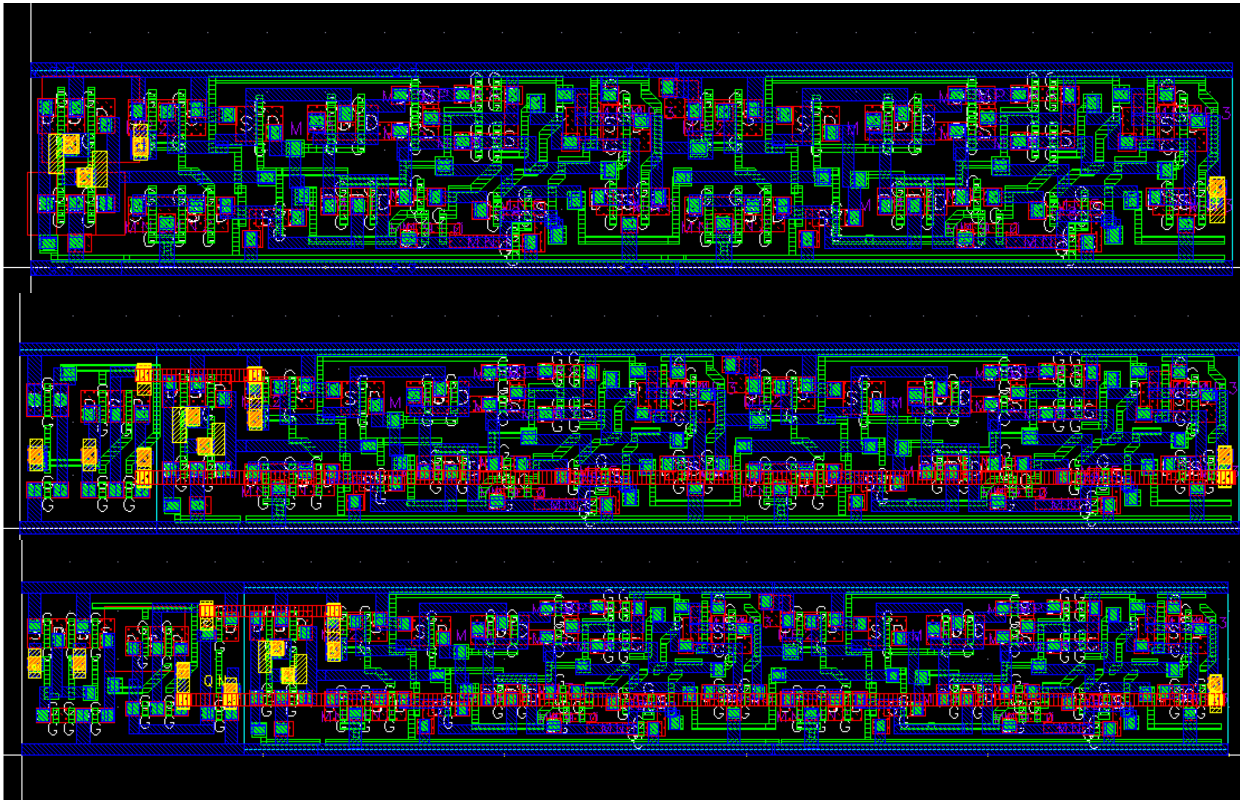
  -> Allows to process two consecutive pulses in a row

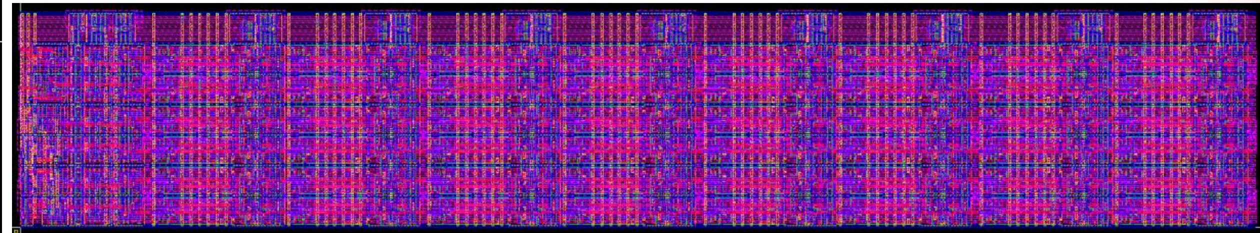
- Angular resolution will require a more sophisticated data processing scheme and perhaps an AI approach might work well

Top Level Design



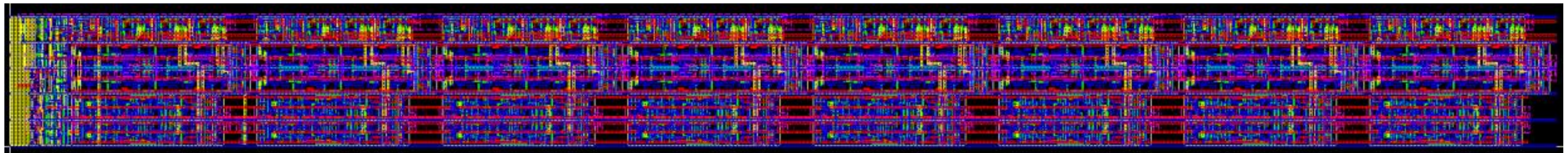
RHBD Dice Registers





Register File

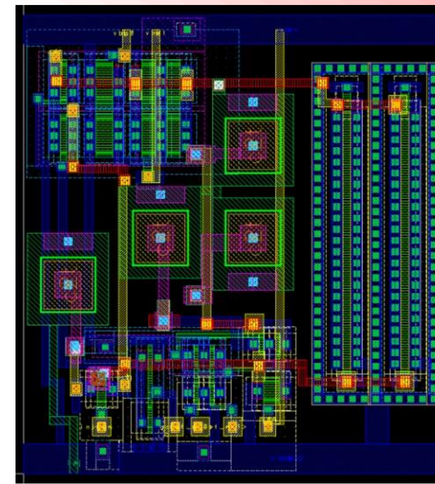
Radiation Test Block



NHANCED SEMICONDUCTORS

New HP Analog Designs

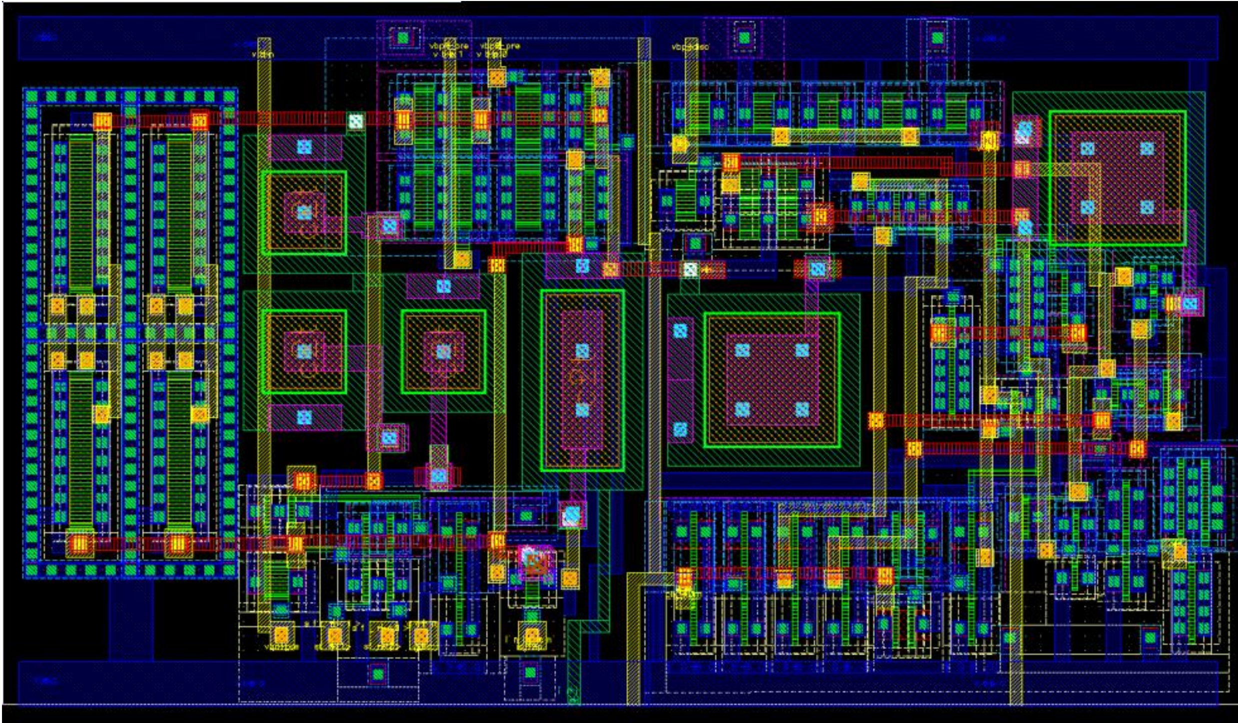
Preamp0



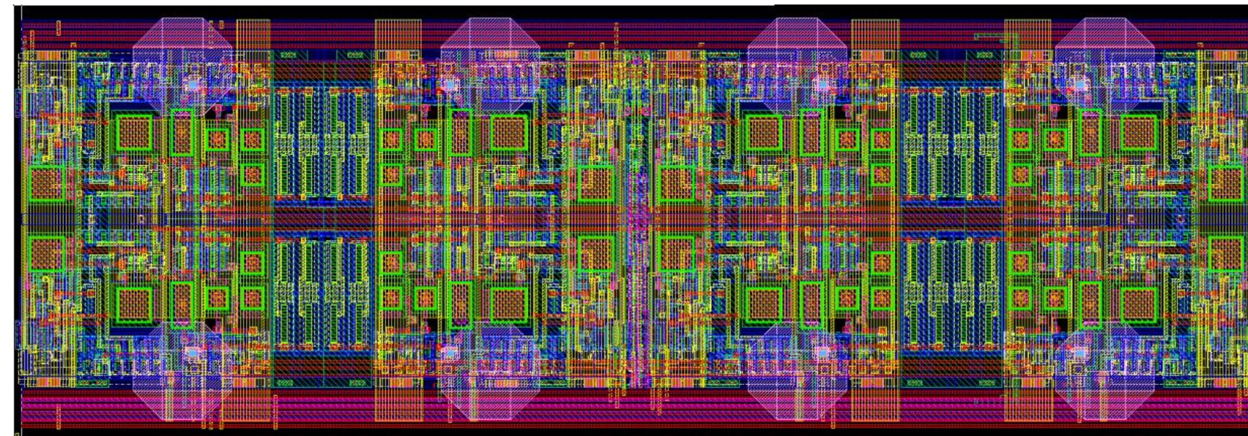
Front-End

Preamp

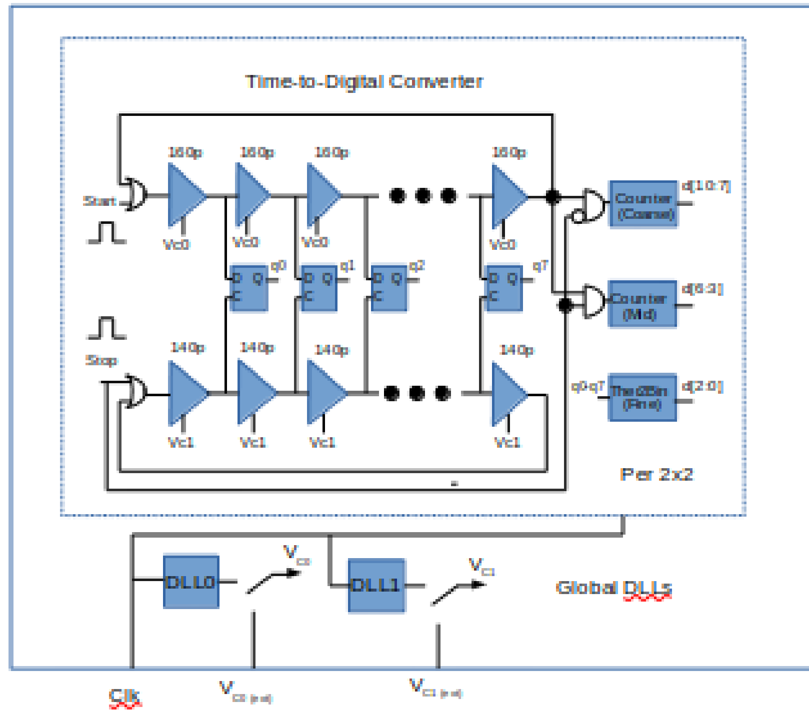
Discriminator

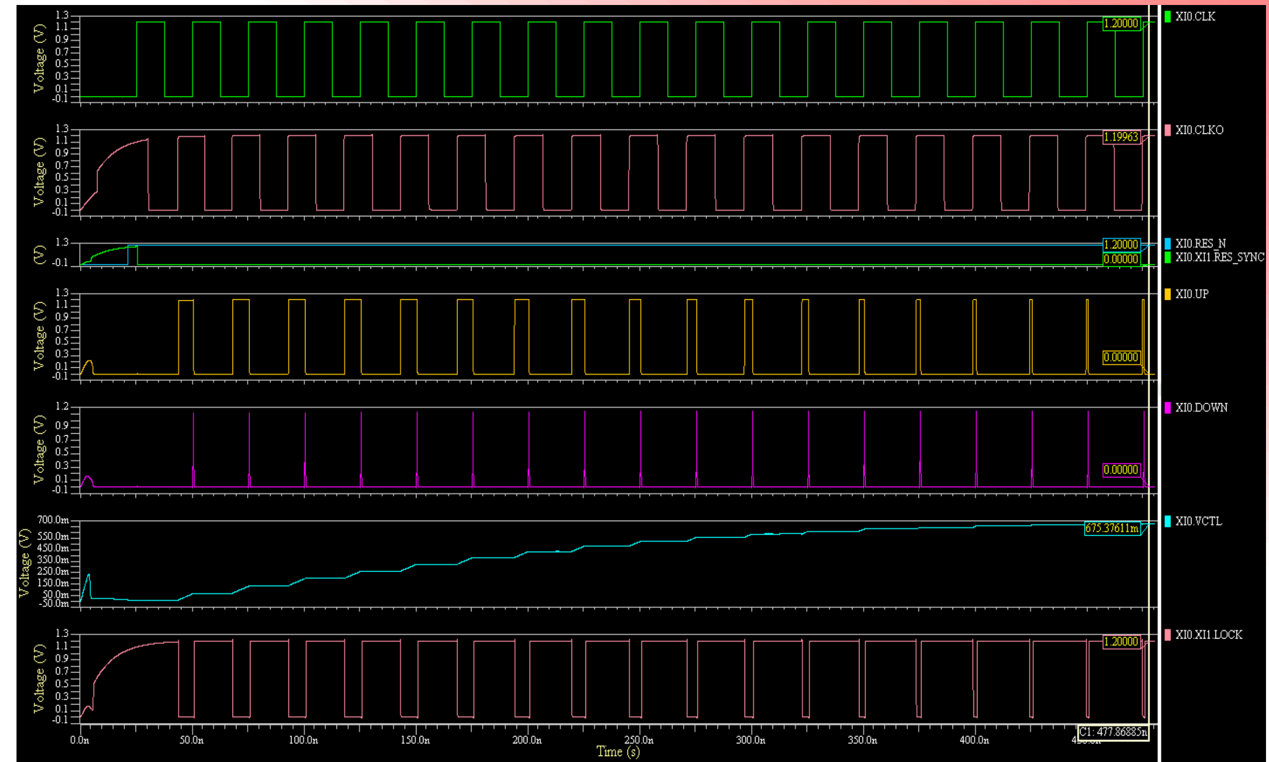


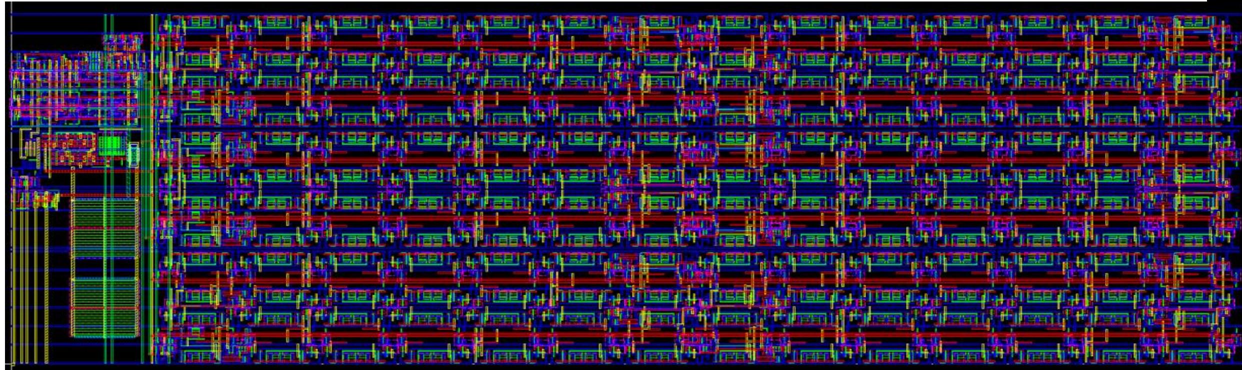
2x4 Array



DLL Chains: Core of LP Picosecond Resolution







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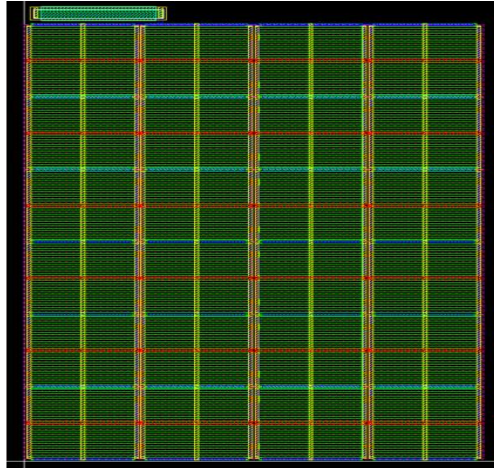
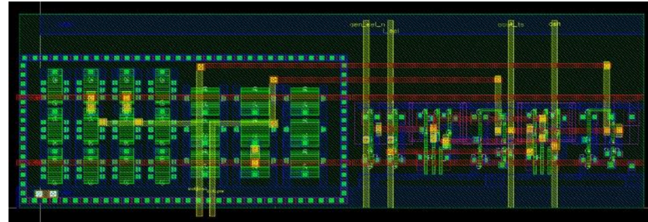
Time to Digital Converter (TDC) And Some of the “Other”

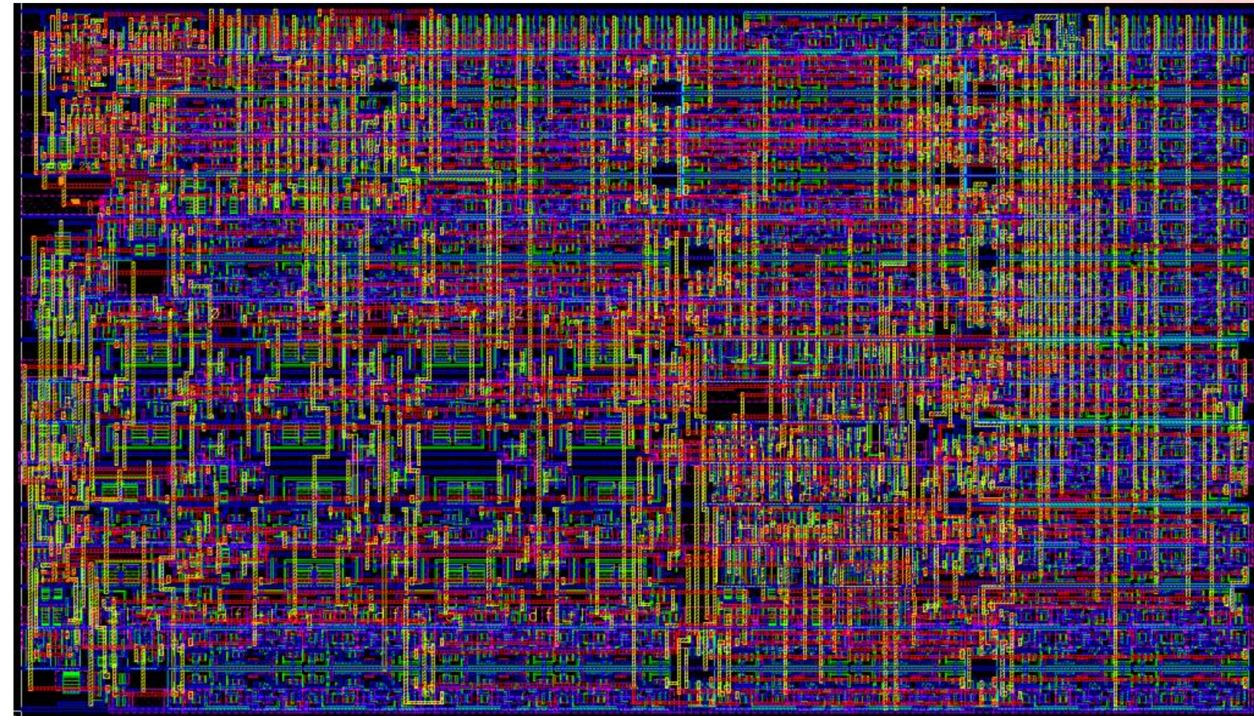


RC Ref Filters, I Generators



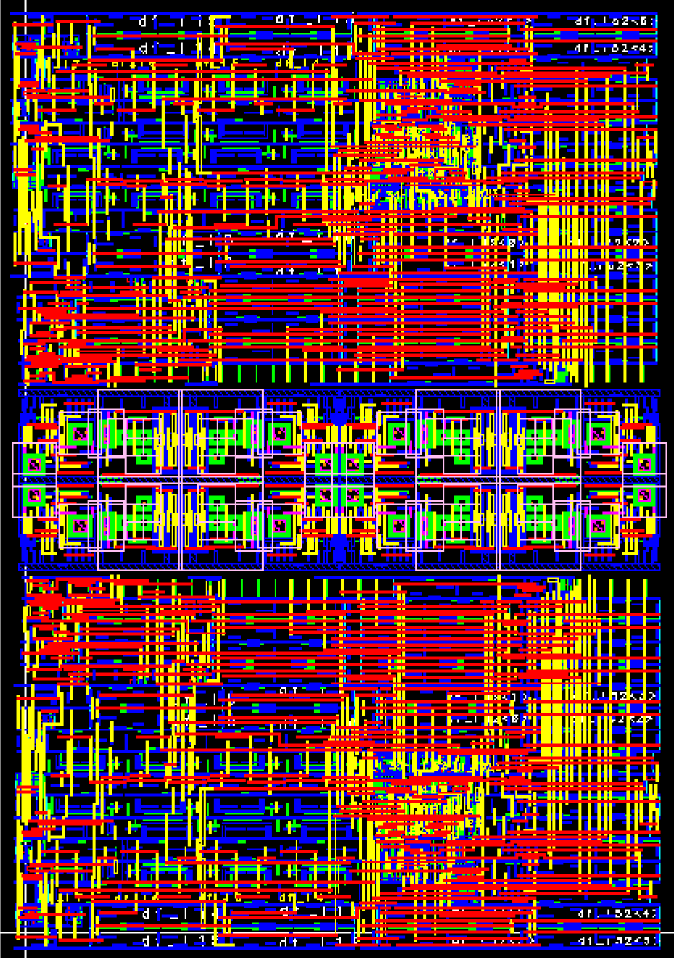
AMBA, I Refs, Analog Support, Trigger Logic

TDC Top Level

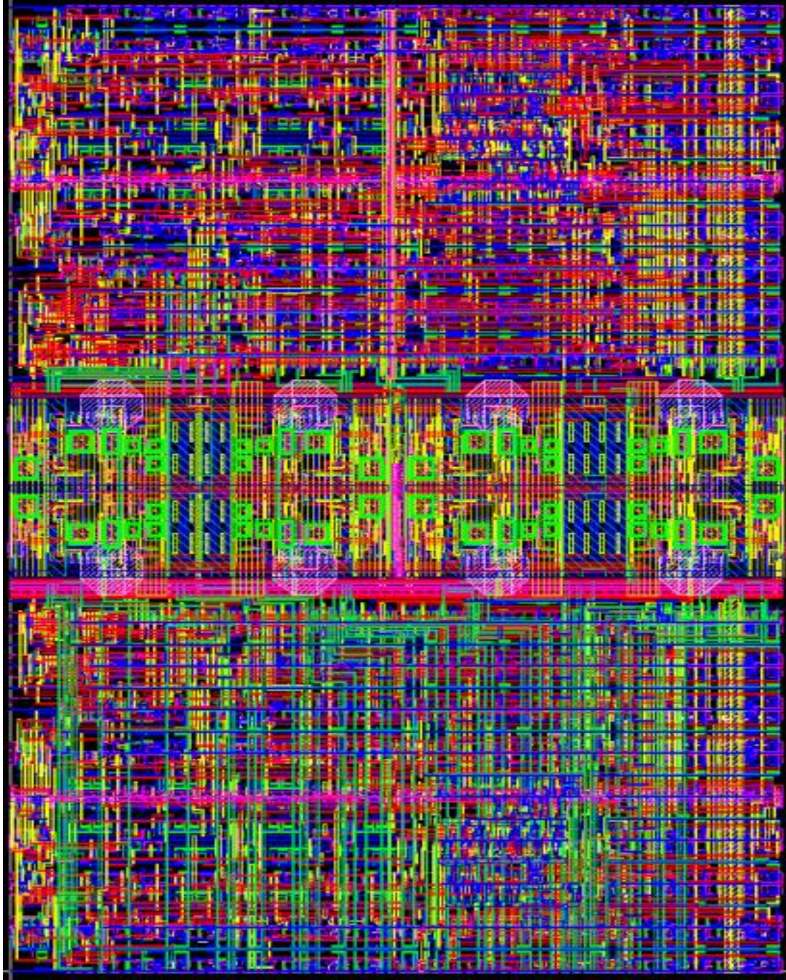


Top Level ROIC Design

2x4 ROIC Pixel Group Preliminary



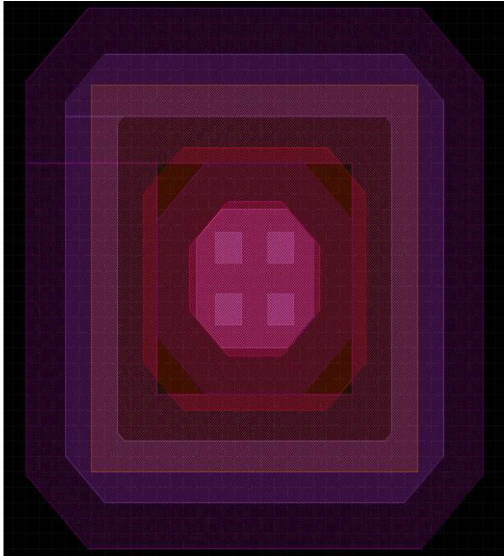
2x4 ROIC Pixel Group Final



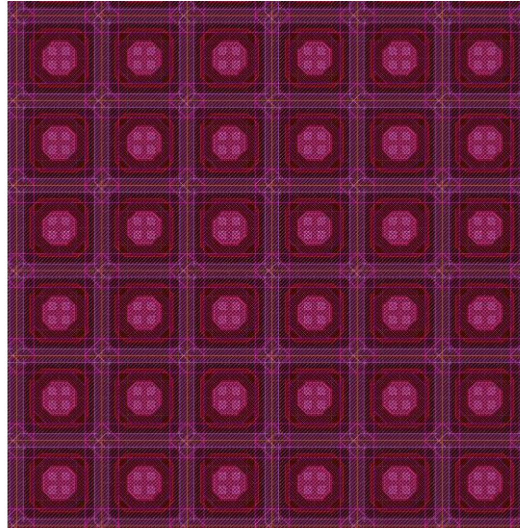
NHANCED SEMICONDUCTORS

The Detector

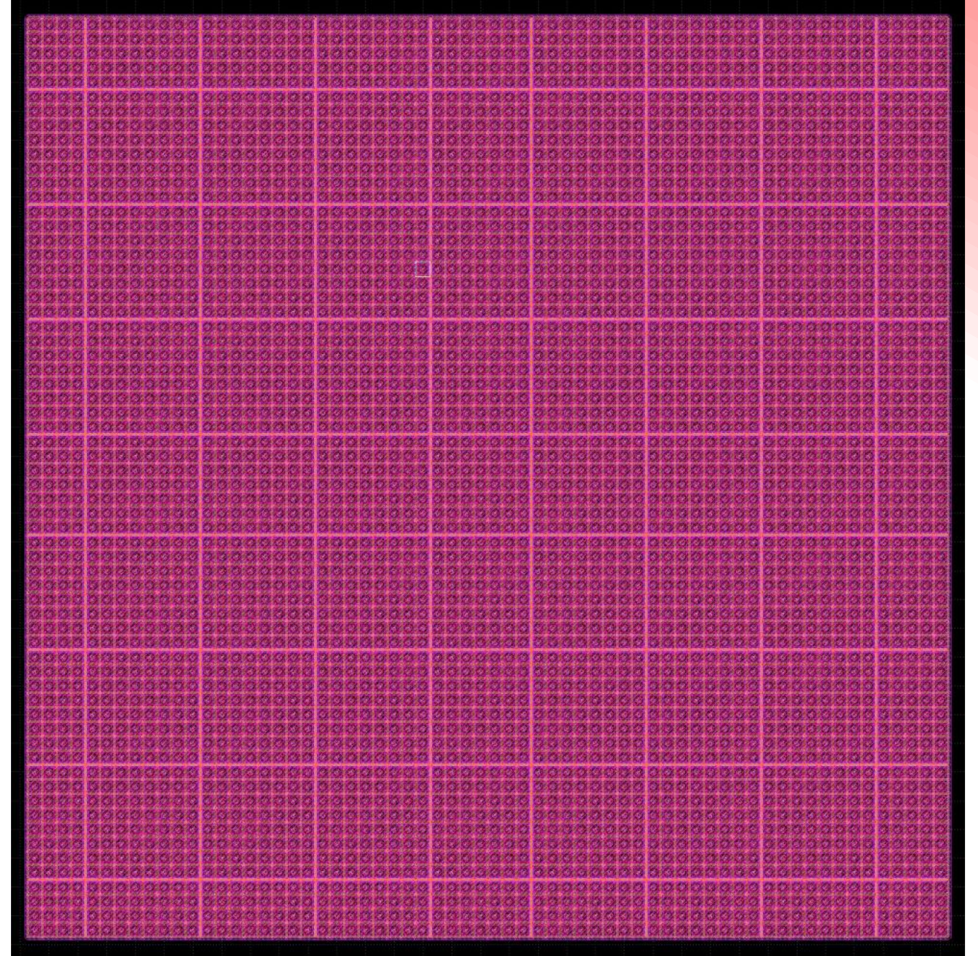
Detector Pixel (25x25um)



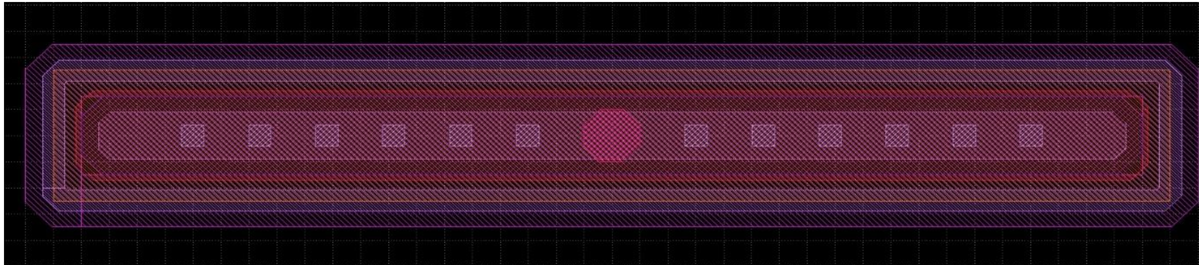
Detector Pixel Group



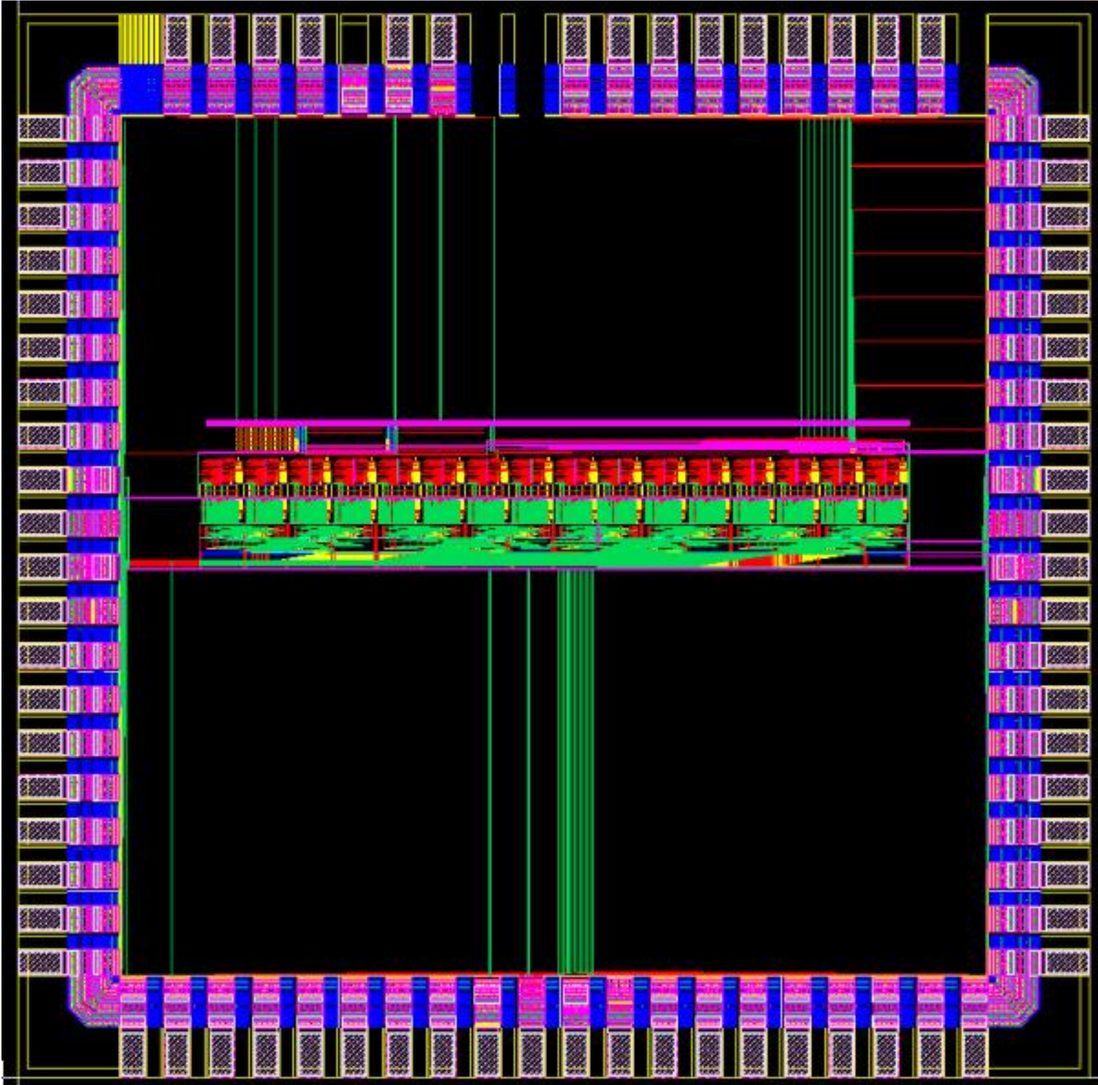
Detector Pixel Array



Detector Strip (25x200um)



Top Level ROIC Test Chip



NHANCED SEMICONDUCTORS

Challenges

- PI Change
- COVID delays
  - Internal
  - Supply chain
- Tool and PDK deficiencies
- Tool set change
- Build a hardened library

Direct and Indirect Breakthroughs

- Single Layer Directionality
- New ultra-thin temporary bonding
  - Good to >400C processing
  - Extremely planar
- Microwave annealing
- RHBD Tower 130nm Library Development

Conclusions

- Simulations complete
- Designs and layouts complete
- Verifications complete
- Foundry – some in process

- Significant new learning

WESTGATE MASTER PLAN

WESTGATE NORTHWEST PERSPECTIVE

WESTGATE ELEVATION