

DE-SC0020500

# Digital Data Acquisition with High Resolution and Linearity

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Principal Investigator

SBIR Exchange, August 16, 2023 5:00pm



- The company and its capabilities.
  - Customers.
- The ADC Nonlinearity problem.
- Nonlinearity example from Majorana Demonstrator.
- Demonstration of the Differential Nonlinearity (DNL) with our own DDC-10.
- Dedicated boards for measuring the ADC nonlinearity *in situ*.
- The nonlinearity measured with the dedicated board.
- The nonlinearity correction.
- Modifications to our regular product.
- Summary and conclusion.
- Future plans.
- Acknowledgements.

- The team: three physicists / engineers, a senior software engineer, a part time physicist, and a manager. We regularly work with a local Electrical Engineering consultant.
- We worked with several interns listed on the Acknowledgements page.

## Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, astrophysics, etc.

## Our capabilities: Development of electronic instruments for Nuclear Physics.

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, either hard silicon or soft cores.
- Algorithms for pulse processing.
- Algorithm implementation in FPGAs and in embedded processors.
- Processing data from nuclear detectors of any kind.
- Development of simple detector assemblies using scintillators, PMTs, or SiPMs.



## Success Story: LUX-Zeplin Data Acquisition

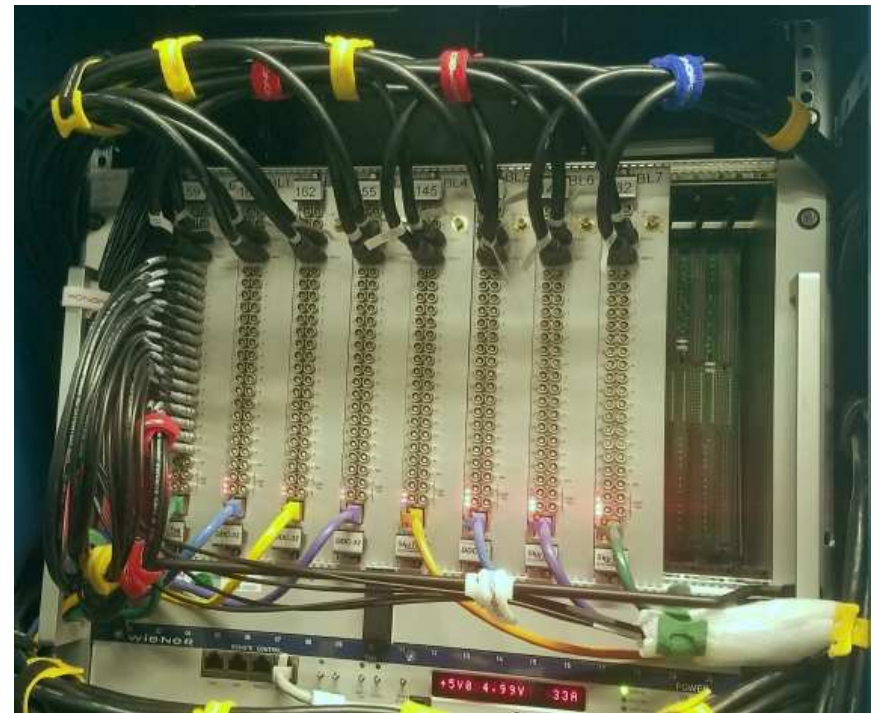
- LUX-Zeplin is the world's largest Dark Matter Search liquid xenon two-phase TPC (10 ton LXe).
- We delivered **1,632 channels** of the DAQ electronics to the LZ Collaboration.
- **No bad channels.**
- The DAQ was deployed in Sanford Underground Research Facility at -4850' in Summer 2019.
- No problems were found with the DAQ while collecting signals since November 2019.
  - Continuous operation since deployment without any failures.

26 **Logic Boards**, sixteen 3.2 Gbps links each



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51 **Digitizers**, 32 channels each



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Low Energy Community Meeting 2023 at Facility for Rare Ion Beams (FRIB) at Michigan State University in East Lansing, MI. The detectors of cosmic rays were assembled by our interns Edmond and Joshua prior to the trip. The *Cosmic Ray Display* has three pieces of clear plastic on top. Each time a cosmic ray is passing through the detectors, these pieces will light up. We attracted quite a bit of attention with our live demo.



Cosmic ray detectors

Cosmic ray display LEDs

## The Problem:

- Pipelined ADC architecture causes semi-periodic nonlinearities of the response, due to imperfect matching of the ADC stages.
- Nonlinearity is impacting resolution in high precision measurements
- Example was described in the Majorana Demonstrator paper.

N. Abgrall, et al, *ADC Nonlinearity Correction for the MAJORANA DEMONSTRATOR*

<https://arxiv.org/pdf/2003.04128.pdf>

Nonlinearities of the GRETINA digitizer (AD6645) reported by Majorana Demonstrator.

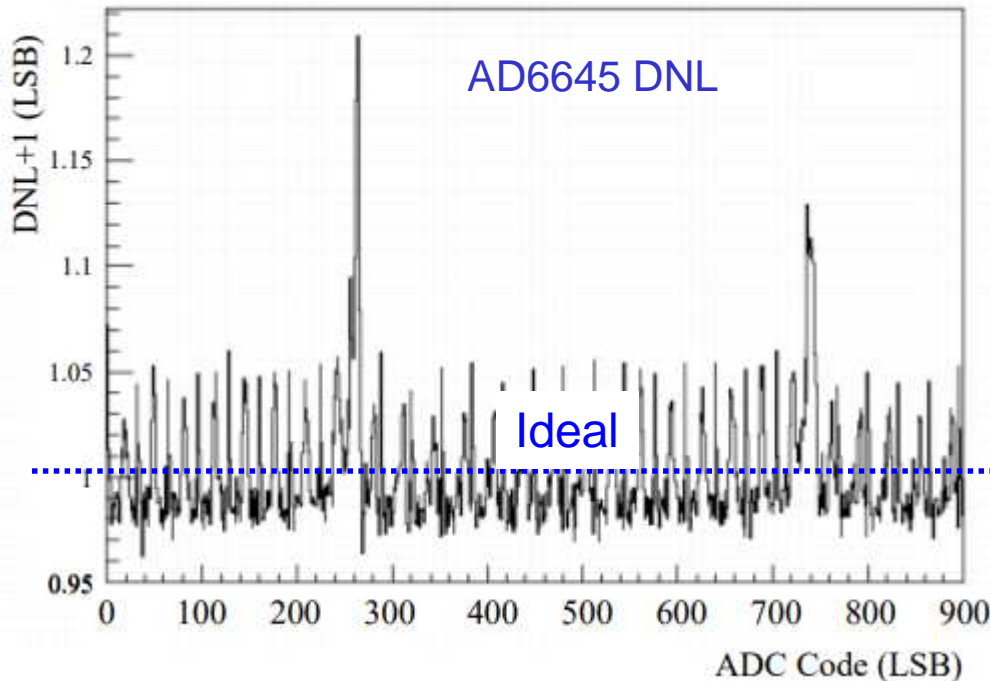
N. Abgrall, et al, ADC Nonlinearity Correction for the MAJORANA DEMONSTRATOR

<https://arxiv.org/pdf/2003.04128.pdf>

Ideal responses should be flat!

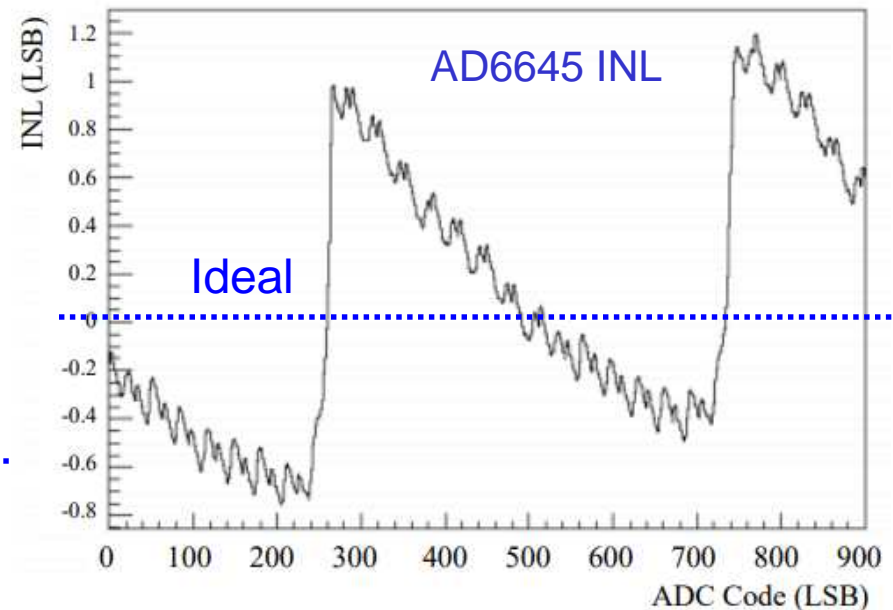
**Figure 3**

DNL measured with slow analog ramp.



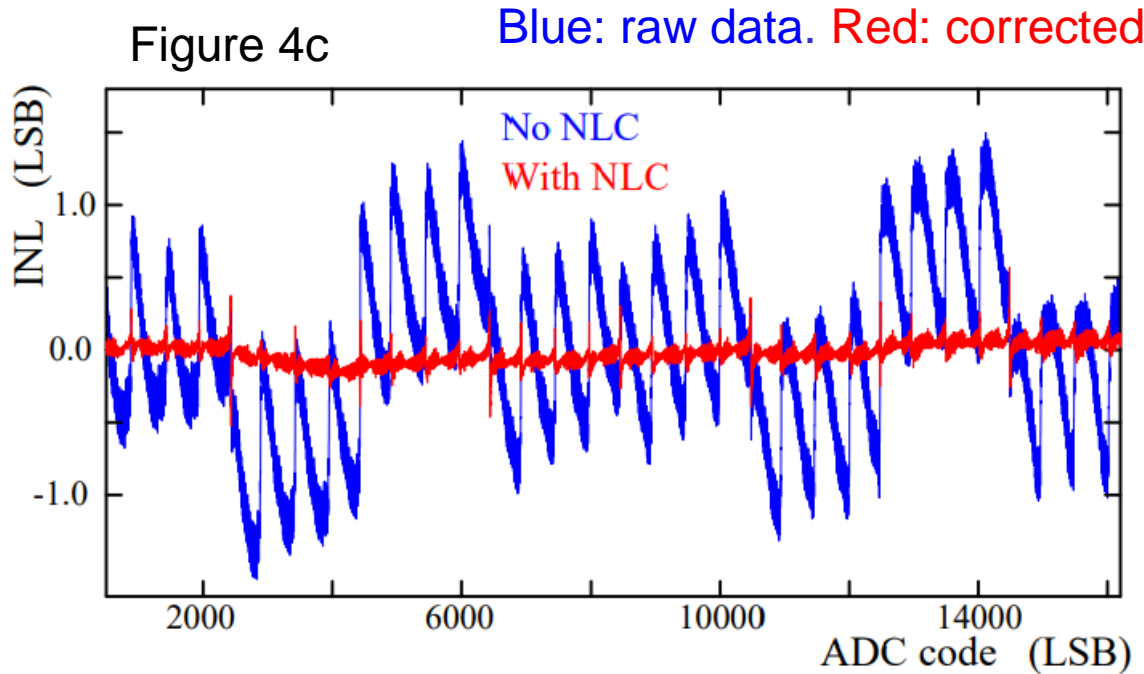
**Figure 4**

INL: integrate the measured DNL, subtract away overall slope.



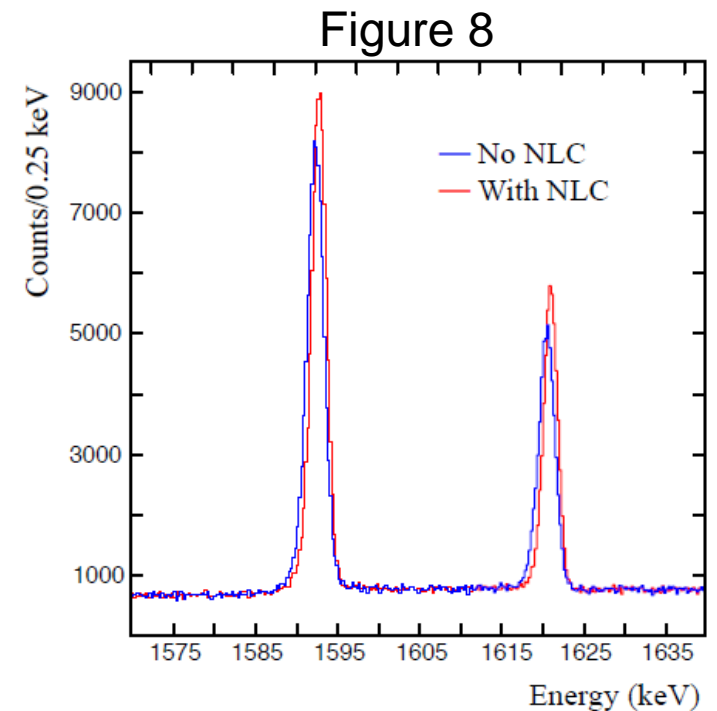


- Use the measured ADC value to index the correction table.
- The table provides deviations of the measured values from the perfect ADC response.
- Fig. 4: Corrected INL (red line) is almost perfect, except for small residual INL spikes near major ADC bit transitions.
- Fig. 8: Improvement of the 1592.5 keV and 1620.7 keV  $\gamma$ -lines by about 11%.
- Reference: N. Abgrall, et al, <https://arxiv.org/pdf/2003.04128.pdf>



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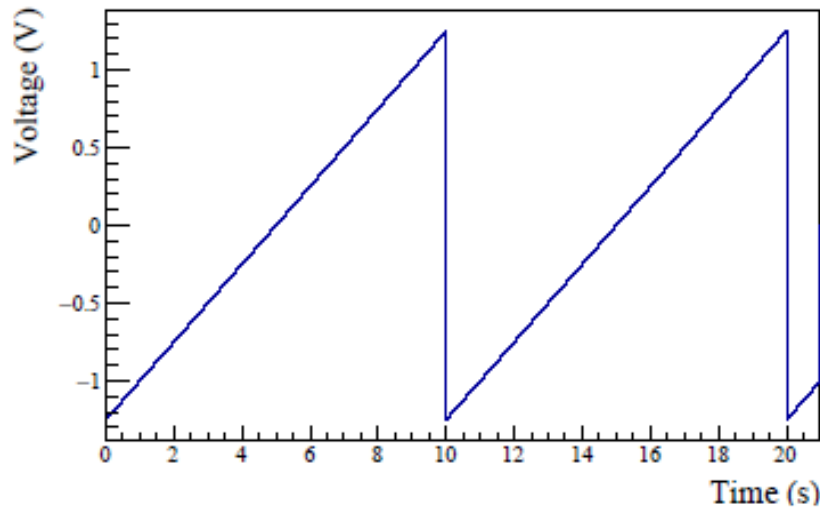
9

# Majorana Demonstrator DNL / INL Measurement

It was quite complicated...

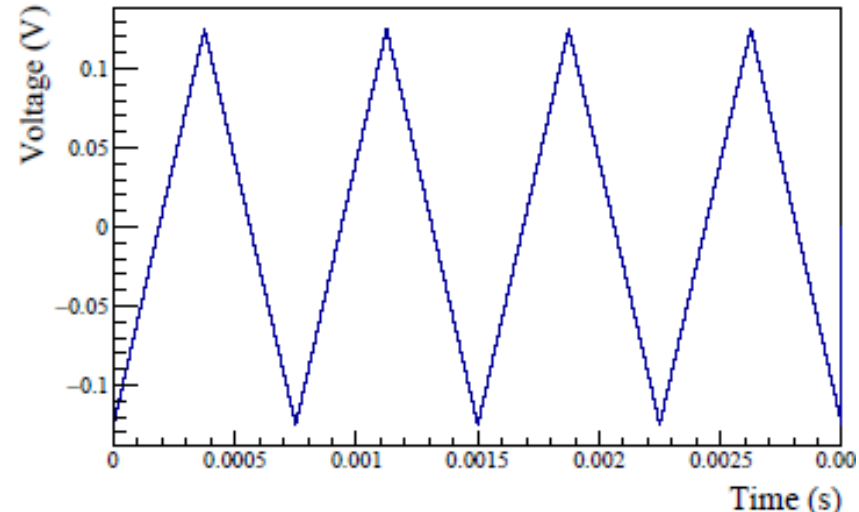
- The authors disconnected detector signals and connected two ramp generators to complementary inputs of the LBNL GRETINA digitizer. The nonlinearity was measured by swiping the voltages over the ADC range.
1. The method required disconnecting the signal cables and connecting the test cables.
  2. It cannot be done with detectors connected to the digitizer inputs *in situ*.
  3. The procedure required a lot of manual work and effort.
  4. The method **requires a differential input**. LBNL GRETINA digitizers provide such inputs, but **this is not common**.

Slow analog ramp applied to one ADC input.



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Fast analog ramp applied to the other ADC input.



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Nonlinear ADC response is easy to demonstrate.

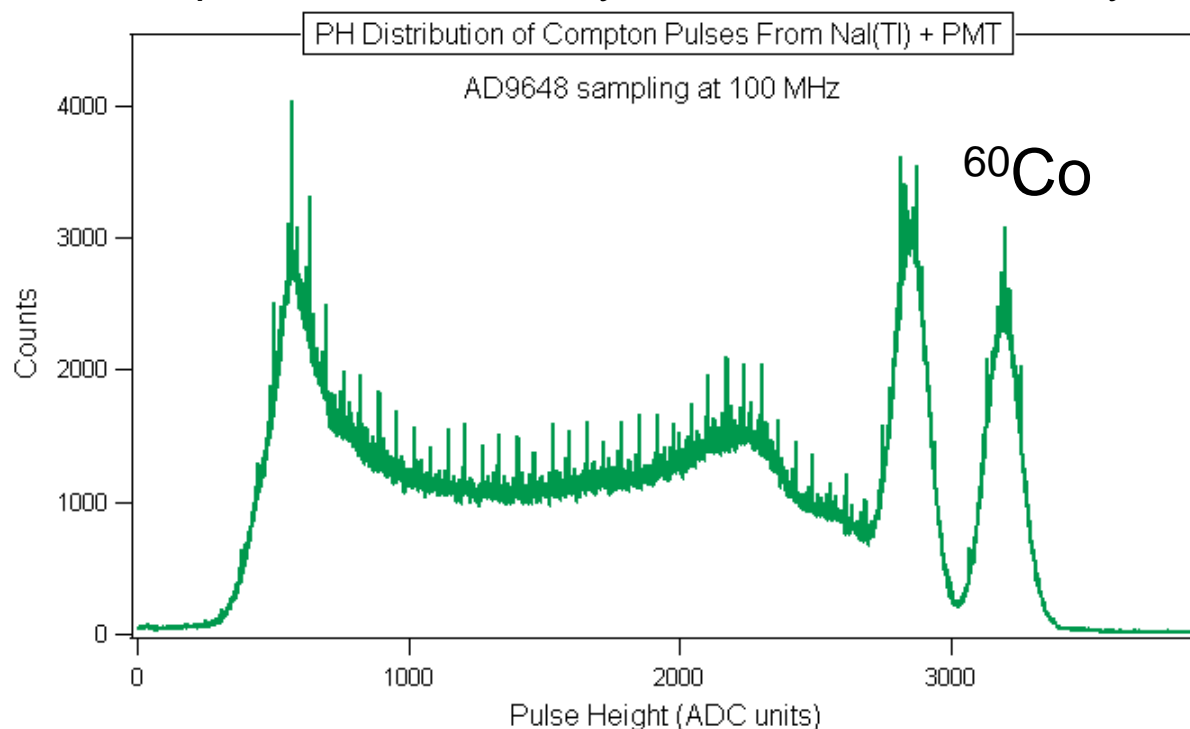
If you have an ADC, then you also have the nonlinearities.

# Nonlinear Response of the Pipelined ADC

Demonstrated with our standard DDC-10 built with AD9648

- DNL is qualitatively demonstrated with the NaI(Tl) detector and  $^{60}\text{Co}$  source.
- The spikes originate at the ADC stages which are not perfectly matched.
- The observed ADC bin width variation is in agreement with the AD9648 Data Sheet.
  - AD9648 is the name of the ADC chip which we used in DDC-10.

## Spikes are caused by Differential Nonlinearity



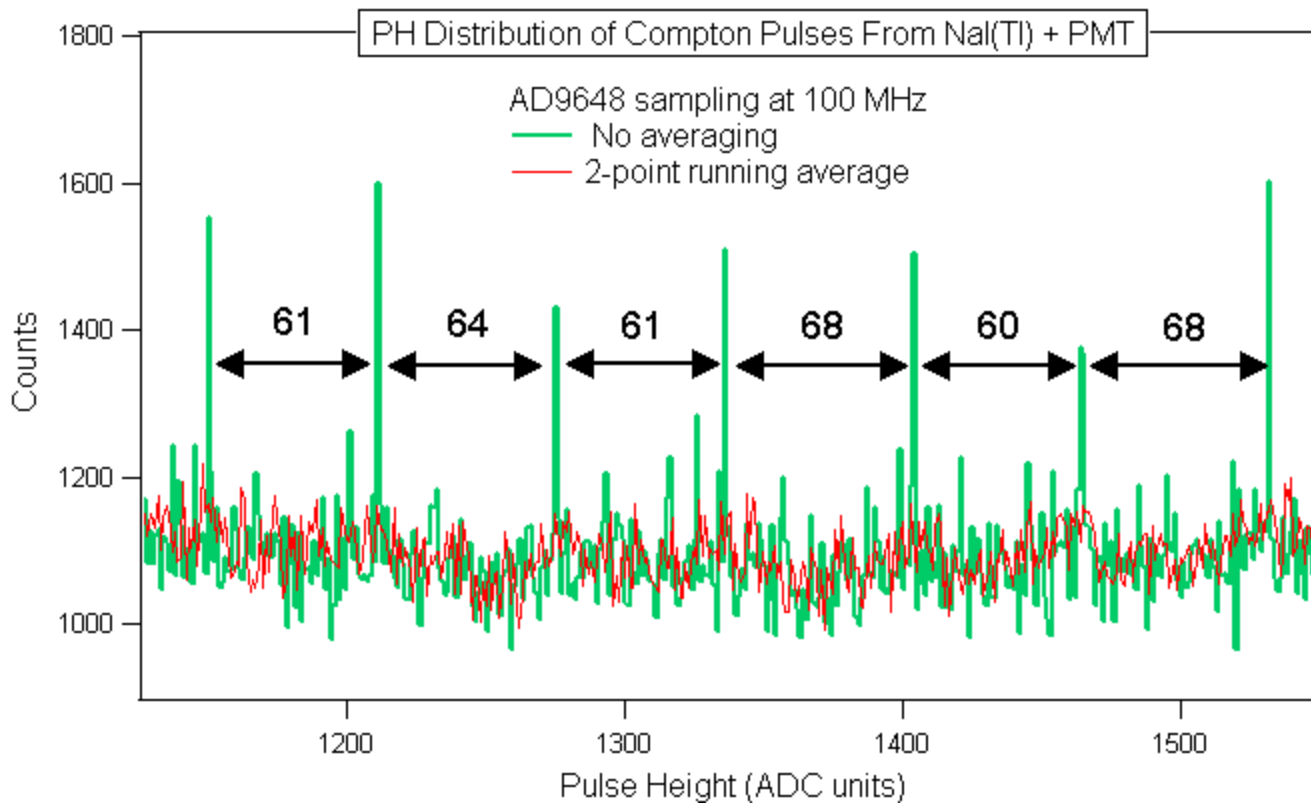
Spikes indicate the ADC bin width variation from 1.0 LSB @ the baseline, to 1.6 LSB @ the spikes.

Consistent with the AD9648 Data Sheet, Table 1, page 4: DNL = +/- 0.5 LSB.

**Important:**  
In order to see the nonlinearity, do NOT apply any averaging

The zoomed histogram is showing the semi-periodic Differential Nonlinearity (DNL).

## Spikes are caused by Differential Nonlinearity



Spikes indicate the ADC bin width variation from 1.0 LSB @ the baseline, to 1.6 LSB @ the spikes.

AD9648 Data Sheet, Table 1, page 4: DNL = +/- 0.5 LSB.

**Important:**  
In order to see the nonlinearity, do NOT apply averaging

Averaging will not remove the DNL impact on the HPGe resolution.

# We Built the Test Digitizer With 18-bit ADC & DAC forming on-board nonlinearity measurement circuit

Voltage generators

1: Fast ADC, 2 channels, 14 bits  
2: Slow ADC, 1 channel, 18 bits

+5V

Ethernet

SD card with Linux

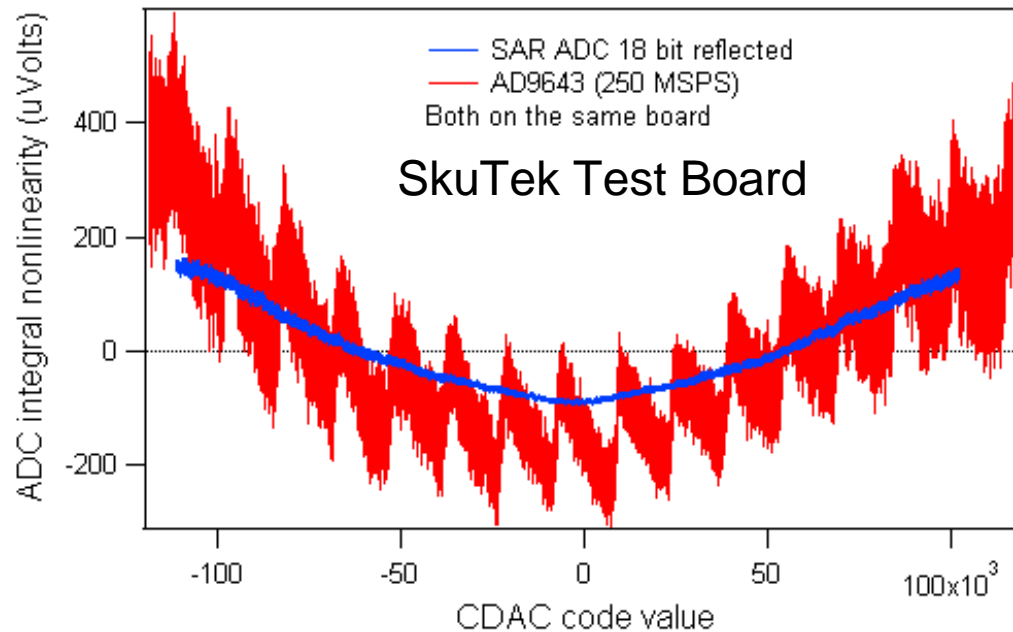
JTAG & UART over USB



JTAG

# In Situ Nonlinearity Measurement Performed with our 18-bit Test Digitizer

- For every 18-bit DAC voltage we recorded two ADC waveforms with 32k samples.
  - A waveform from the **fast pipelined 14-bit ADC**.
  - A waveform from the **slow SAR 18-bit ADC**.
- We calculated the averages of both waveforms and plotted against the DAC code.
- The **slow SAR ADC** was free of local nonlinearities (no sawtooth pattern).
- The **fast pipelined ADC** showed the sawtooth, as expected.
- The overall **horseshoe pattern** was caused by the **operational amplifier** at input.



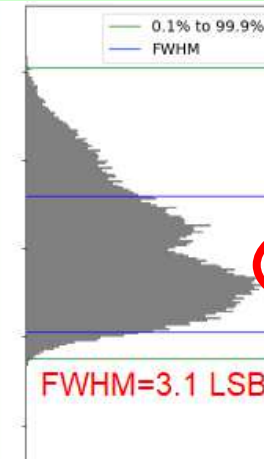
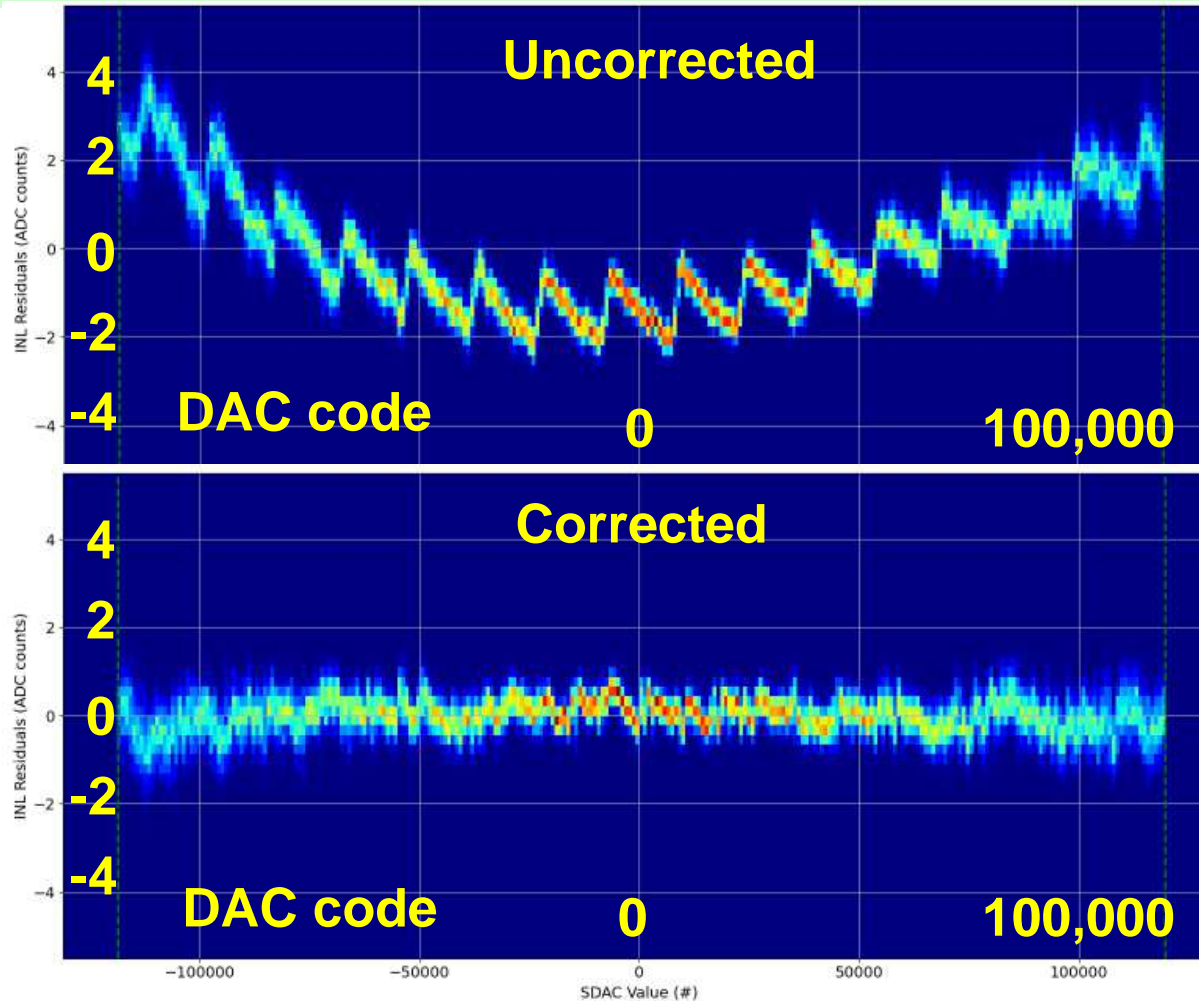
Blue: slow 18-bit ADC  
Red: pipelined 14-bit ADC

# Our Nonlinearity Measurement and Correction

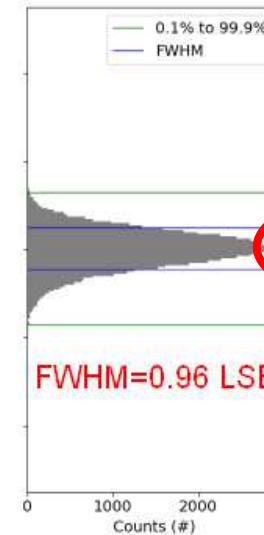
Using our 18-bit Test Digitizer

- We measured the INL, using the on-board 18-bit DAC to drive the **known voltage** to the input.
- The stimulus voltage was **verified** using the 18-bit ADC in parallel with the 14-bit main ADC.
- After applying the correction, the 14-bit ADC response is **at the limit** of the ADC Data Sheet.

**Integral Nonlinearity (LSB)**



**3.1 LSB**



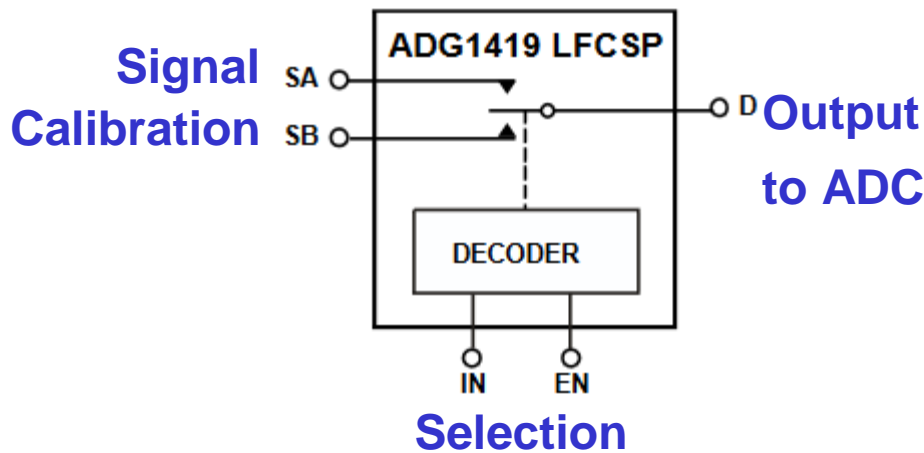
**0.96 LSB**



# Time to modify our 32-channel digitizer!

- Analog switch selects between the input signal and on board calibration

## Conceptual schematic



## ADG1419 signal bandwidth

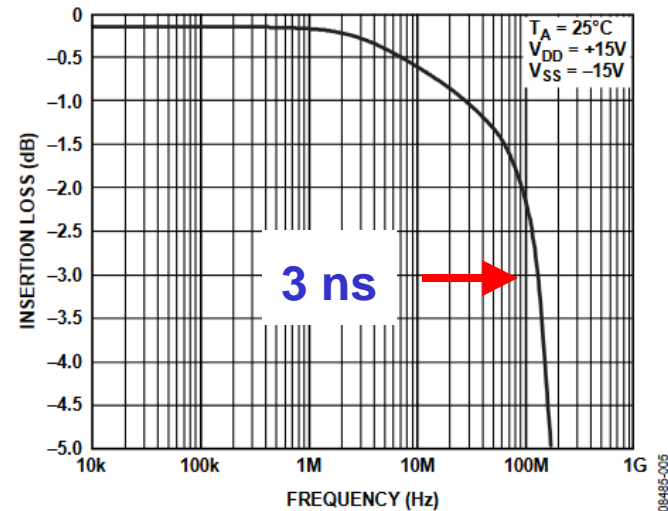
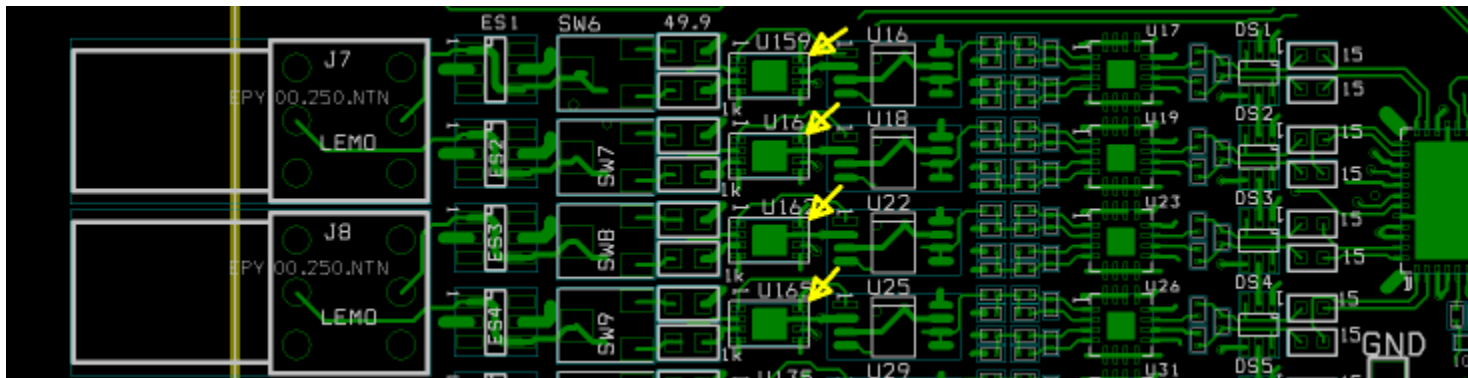


Figure 19. On Response vs. Frequency

## Modified board layout with analog switch in every channel



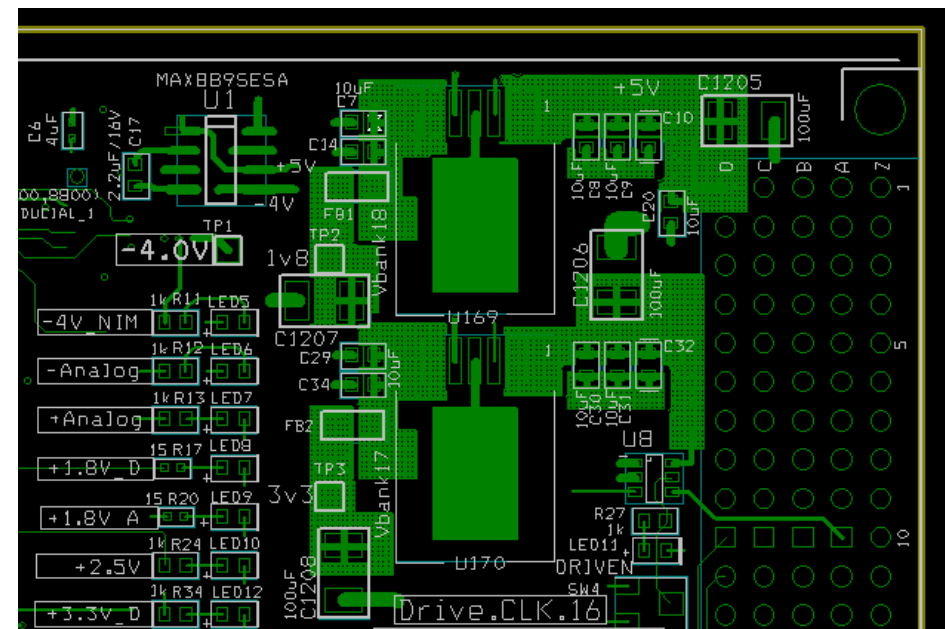
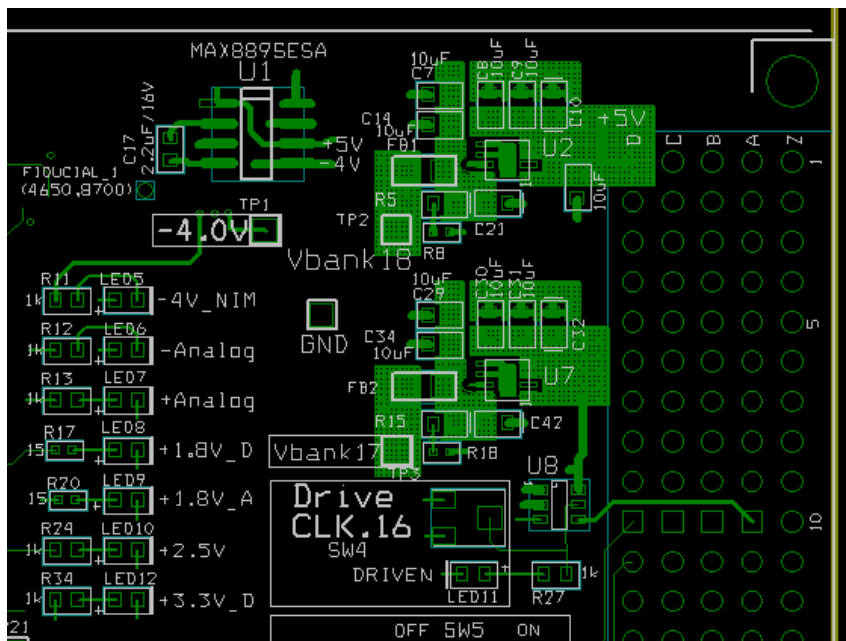
# Skutek Other modifications of the 32-channel digitizer

## Instrumentation

- Out of stock parts changed to in-stock ones. These parts were procured before redesigning the board.
- The area in the upper-right corner of the board is shown before and after redesign.
- NB: original design was perfectly valid and tested. *It is frustrating to do these changes.*

TPS82084SIL out of stock

LMZ10505TZ in stock



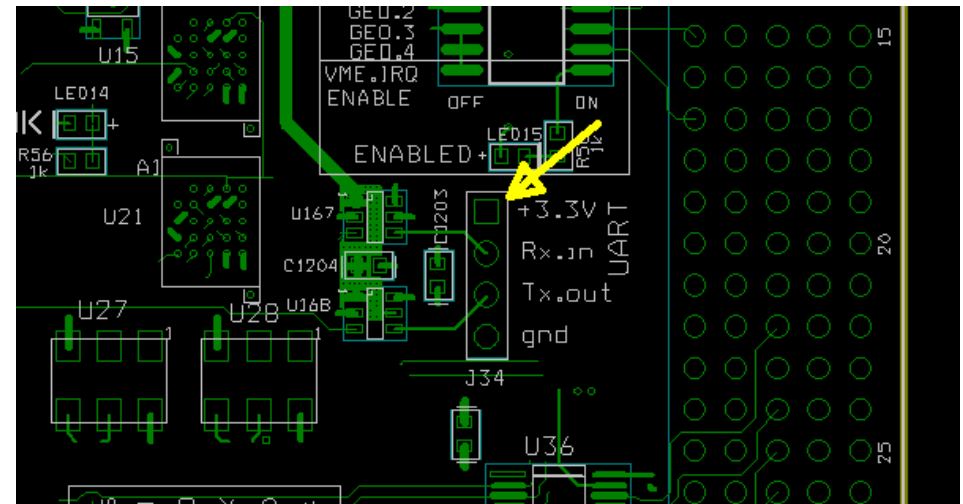
# **SkuTek** Other modifications of the 32-channel digitizer *Instrumentation*

- Two small additions will allow to embed a small RISC soft core in the FPGA fabric.
- The core can run a real time operating system named Astrobe.
- Calibration tasks can be fully automated using this core without the on-board Linux.

## Micro SD card socket



## Serial port pin connector



- We developed two **Linearity Test Boards** with the 14-bit pipelined ADC, 18-bit stimulus DAC, and ancillary feedback ADC for verification of the stimulus test voltage.
- 250 MHz ADC (we showed the photo), and a 100 MHz ADC (not shown, looks similar).
- The boards let us measure the DNL and the INL **without disconnecting** the inputs.
- We measured the ADC response functions and derived the INL corrections.
- We applied the corrections both **offline** to recorded waveforms, and **online** in real time.
- We developed the **firmware** for applying real time corrections.
- **Phase II electronics.**
- The Phase II **production was delayed** due to supply chain disruptions.
- We were forced to redesign parts of the 32-channel board to use the in-stock parts.
- Before the redesign, we procured the parts.
- The modified 32-channel board is ready for production.

- **Continue** development of hardware, firmware, and software.
- **Simplify** our designs to decrease the exposure to electronic part shortages.
- **Assemble** the modified 32-channel digitizers.
- **Apply the modifications** to future revisions of other devices.
- **Contribute** high linearity devices to Nuclear Physics experiments.
- **Support the DOE mission** through contributing to NP projects.
- **Survive** the part supply crisis till electronic parts are available again.
  - It seems to be happening, but the recovery is slow.

Joanna Klima, Gregory Kick, David Miller, James Vitkus, Jeffrey Maggio

Consultant: Eryk Druszkiewicz

Interns:

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