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2023 SBIR/STTR Exchange PI Meeting
Nuclear Physics

Picoseconds Detector Readout System with 25GE Links

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Telluric Labs LLC

This material is based upon work supported by the DoE, Awards DE-SC0017156
Patents Pending US 15509352, PCT/US2023/063085

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Background

Telluric Labs LLC was first registered in New Jersey in 2016 by its two founders Michael Ivanciu, and Radu Radulescu.

The core field of expertise is next generation photonics based readout networks integrating picosecond timing.

Develops fundamental cross-domain technologies in collaboration with research institution and industry experts.

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Picoseconds Detector Readout System Description (IP Access Gateway System)

- Integrates Frontend, Backend, and computing subsystems into a software defined, in band time synchronized, highly scalable DAQ (from 25Gbps to Pbps) through COTS HW, and IP based protocols;
- Provides ubiquitous timing synchronization with a precision range of 10pS or better and immediate event reconstruction.

Functional blocks:

- Continuously timestamping TDC engines, configurable for either accuracy or density (Ex: 16 channels at 500fS v. 256 channels at 7.5pS precision).
- Any combination of configurations coexist on the same FPGA device.
- The network interface – multiples of 10/25/100 GE optical links;
- Packet Switch.

Features

- ETDC determines the timing of both the rising and the falling edge of a pulse associated with an event;
- Minimum pulse width is 500pS;
- Sustained, continuous minimal pulse period = 1nS (2x 0.5nS);
- Maximum sustained rate is more than 2G timestamps per second corresponding to 1GHz signals (as limited by the IO bandwidth);
- IPAG uses the General Timing Synchronization (GTS) protocol and algorithms to synchronize numerically the timestamps;
- The numerical synchronization does not change local clocks, which eliminates transient errors and instability;
- Performs Ethernet packet switching, potentially using all the SERDES/GTY ports of the FPGA (with a theoretical BW of 120 x25G = 3Tbps)
- Can provides ADC equivalent functionality when combined with a front end pulse width modulation (PWM) circuit;
- SW defined operation;
- Seamless interface with third party detectors providing synchronization pulses.

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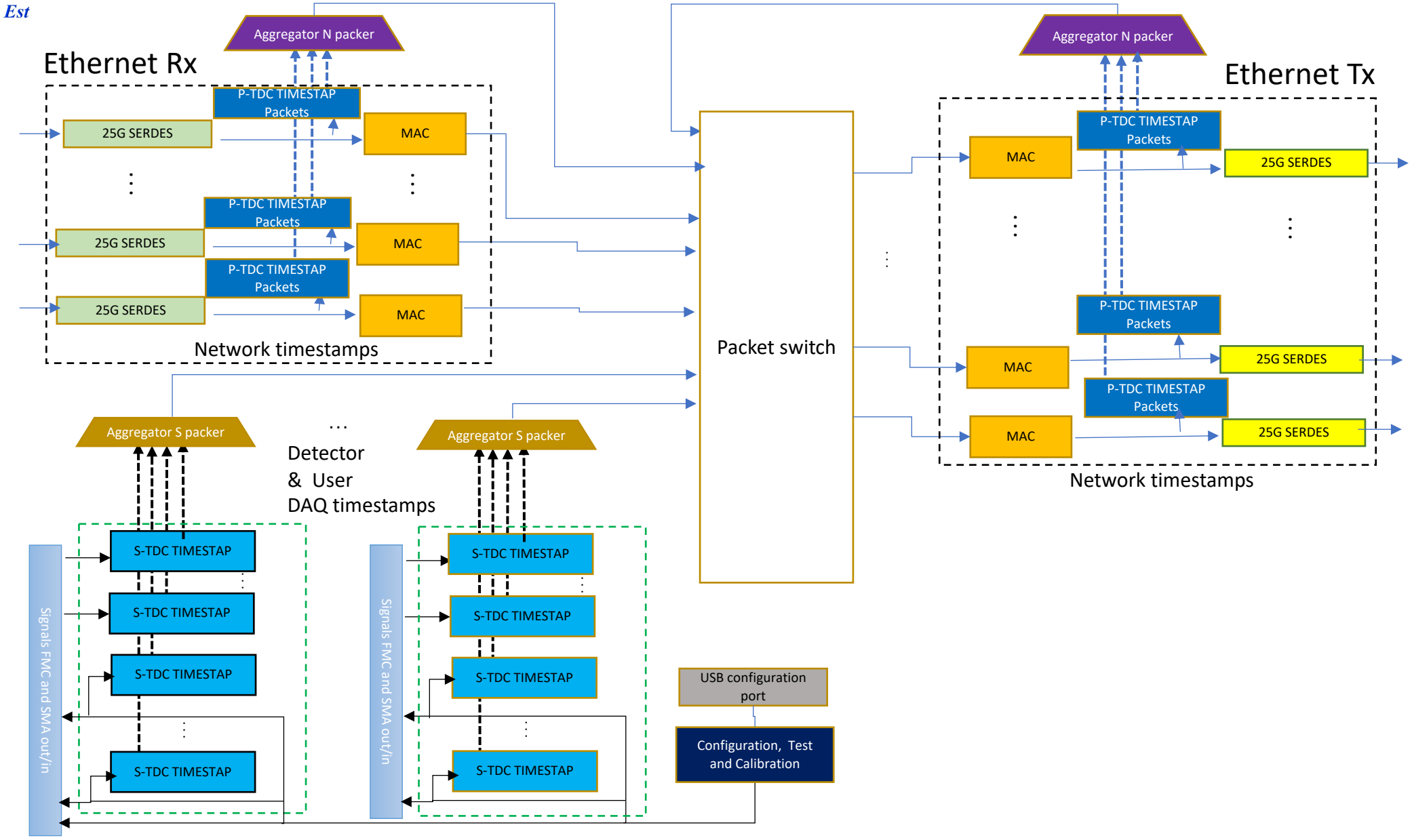
FPGA BLOCK DIAGRAM



Synchronized readout GTS network - tree topology example

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Timing Detector readout network using low cost 25GE FPGA boards with 4, 8, 16, or more ports

Root timing

8 x 25GE IPAG

Stand alone or PCIe inserted IPAG boards

CF1

CF1.1

CF1.1.1

CF1.2.3

CF2

CF2.1

CF2.3

CF3

CF3.1

Network TS

Hits TS

4 x 25GE IPAG

16 x 25GE

Leaf timing

Test loop

COTS Switch

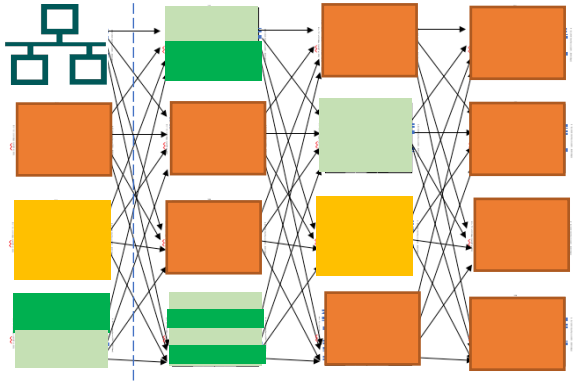
USER DIGITIZER

USER DIGITIZER

Other DAQ

End to End Retiming = CF1(CF1.1(CF1.1.1)) ~ CF1+CF1.1+CF1.1.1

Layered GTS distributed switch topology covering a heterogenous campus network



Example: Interlayer cross section BW for VCU118 boards = 4x4x25Gbps= 400Gbps. Total 1.2 Tbps.

How GTS operates:

- Each 25GE port generates a (Timestamp, packet ID) pair for every packet. These pairs are aggregated into GTS metapackets and sent to the proxy computing node, typically at the outbound end of the link.
- Timestamps generated by the same packet at the two ends of a link (S_I with R_O and S_O with R_I where S=send, R= Receive, I=inbound, O=outbound) are matched based on identical sequences of IDs. The difference between matched timestamps of the same packet represents a Packet Delay (PD). Two PD files are created, PDR and PDS, indicating the Received or Sent direction relative to the Inbound (or Master) end of the link.
- Polynomial functions (FitPDR/S) are fit over the PDR/PDS points of each data Interval (Bn, Bn+1], where Bn represents local values of absolute boundaries determined by Root.
- A weighted average is applied to adjacent FitPDR/S functions.
- The CF.link.m (FitPDR, FitPDS) is calculated for each link.m in the data path.
- An End to End Correction Function is determined for a path as:

$CFe2e = CF_{link1}(CF_{link2}(\ldots(CF_{linkN})\ldots)) \sim = CF_{link1+}CF_{link2}+\ldots+CF_{linkN.}$ This is further used for event reconstruction, TSabsolute = CFe2e(TSlocal).

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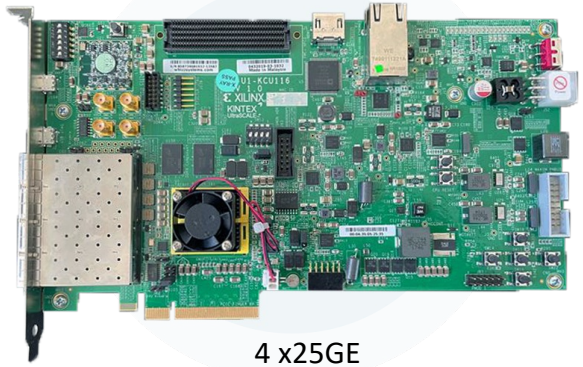
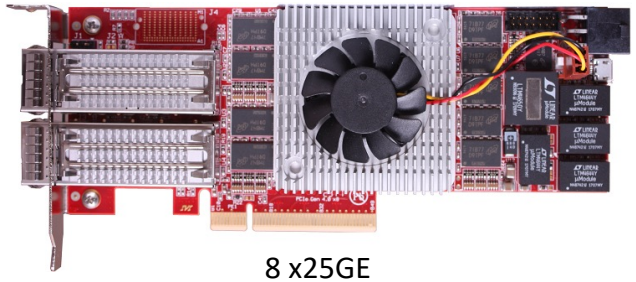
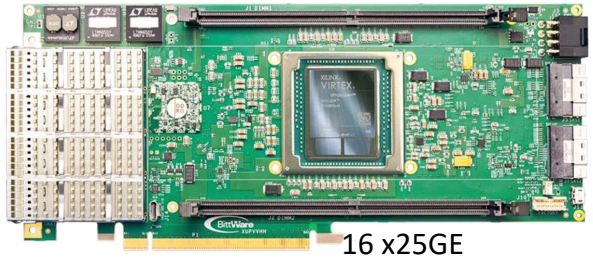
Sample of 25GE COTS FPGA boards and optical transceivers



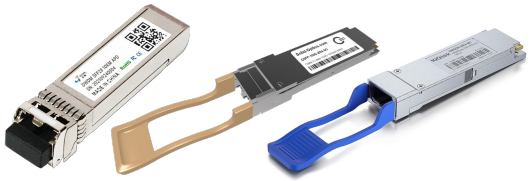
4 x25GE



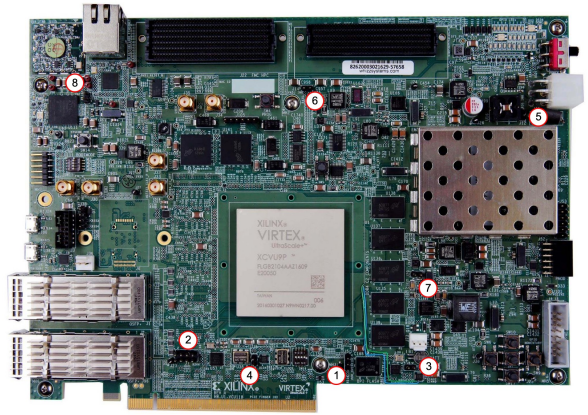
8 x25GE



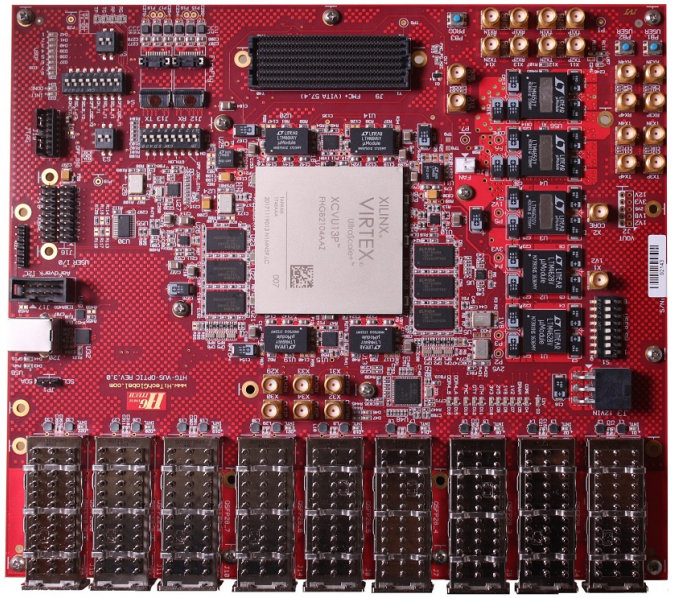
16 x25GE



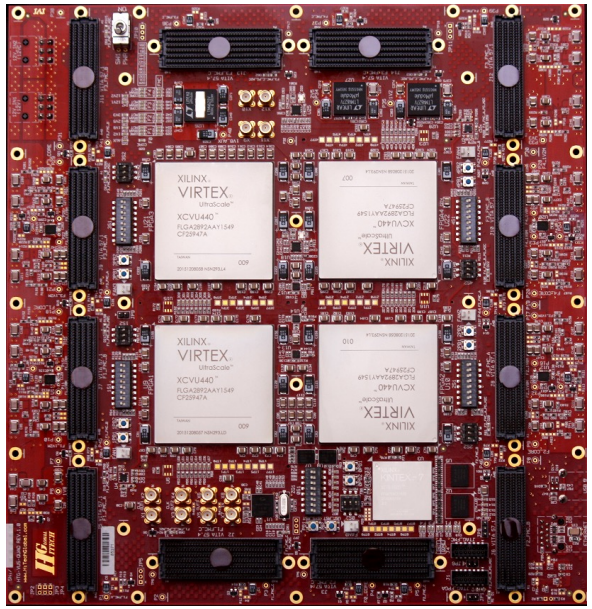
Pluggable SFP+ and QSP form factor COTS optical transceivers



8 x25GE



36 x25GE



48x25GE

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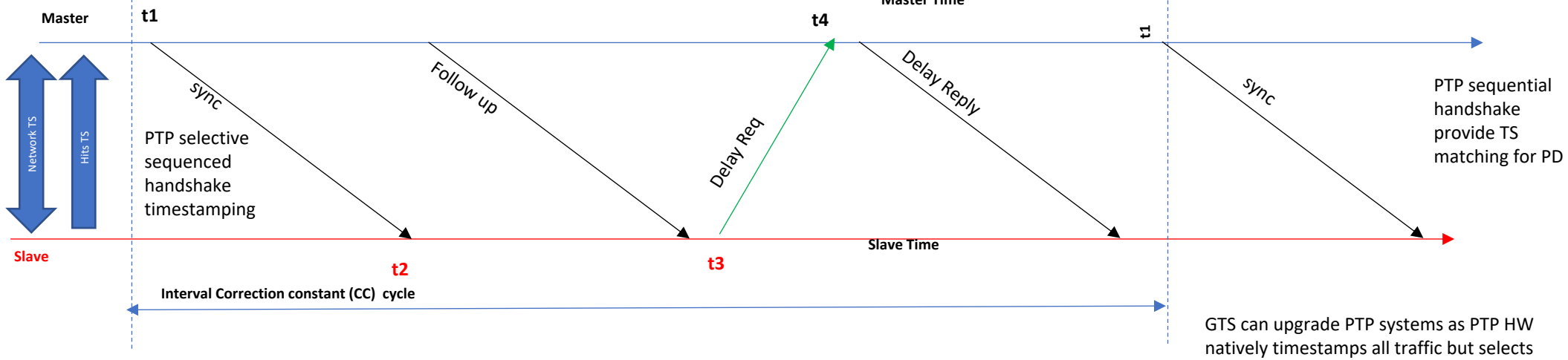
General Timing Synchronization Protocol v. PTP

Timing synchronization equations are based on the travel time of packets through bidirectional communication channels. Established protocols like Precision Timing Protocol (PTP) and White Rabbit use a 4-step Request and Answer packet handshake to transfer remotely captured timestamps.

GTS Metapacket structure

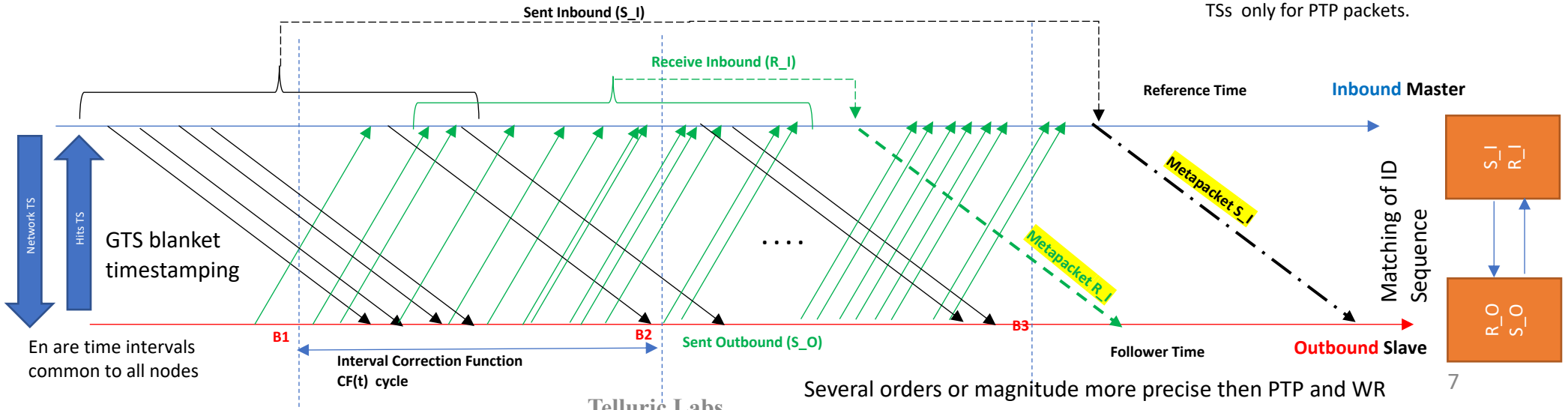
PTP TS packet structure



GTS is significantly more efficient and precise than PTP. This is achieved through the utilization of:

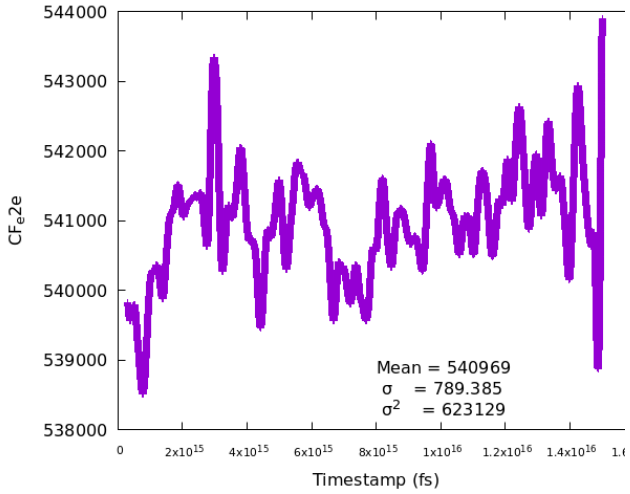
1. A higher number of Network Timestamps (>10^6/s) of user traffic.
2. TS with ps precision, uses Time-to-Digital Converters (TDC).
3. Fixed oscillators.
4. Independent time Synchronization Cycles (~0.3s)
5. Correction Function (CF(t)) expressing dynamic timing relation between nodes
6. Contemporaneous packet timestamps used for CF(t) and detector timestamps to be synchronized are in the same time interval.

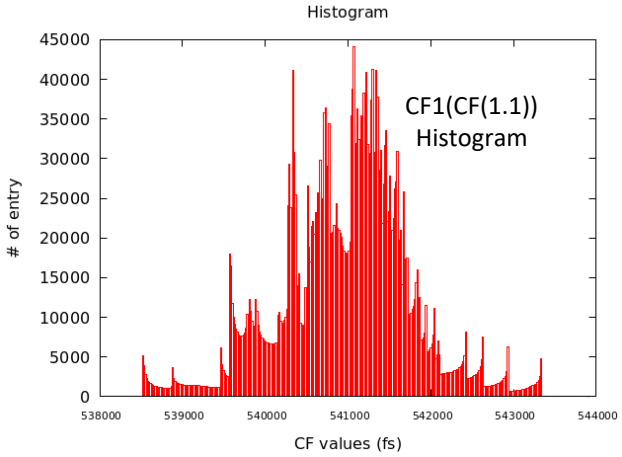
GTS can upgrade PTP systems as PTP HW natively timestamps all traffic but selects TSs only for PTP packets.

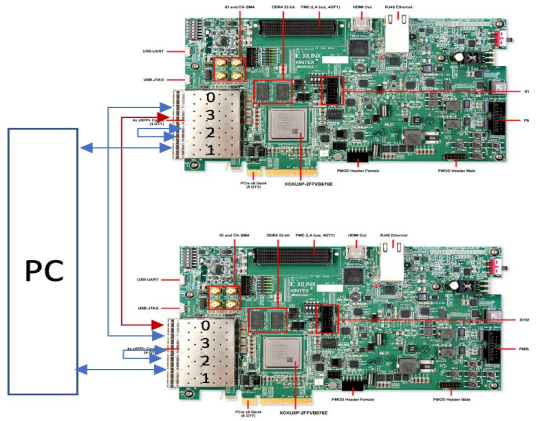


Several orders or magnitude more precise then PTP and WR
Can seamlessly upgrade PTP systems

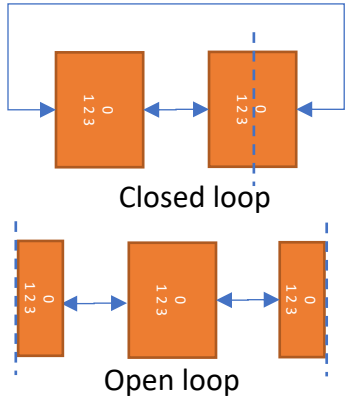
2x25GE links test (packets timestamping by ETDC FPGA)



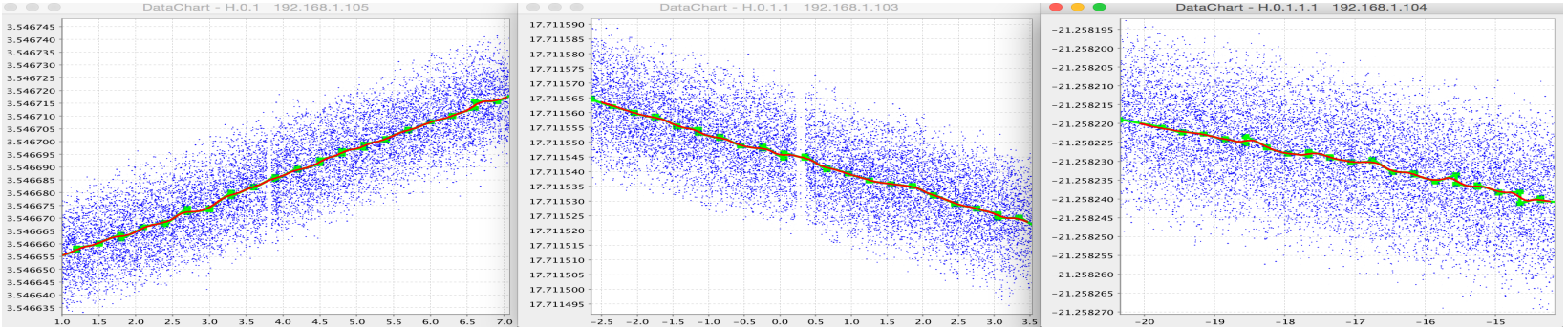


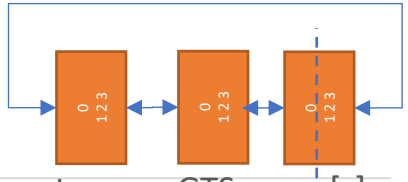


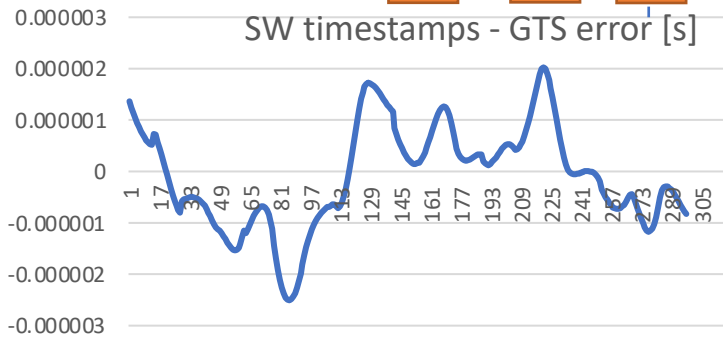
0. 8 ps STDEV across two links



3x1Gbps links test (packet timestamping by UBUNTU SW)



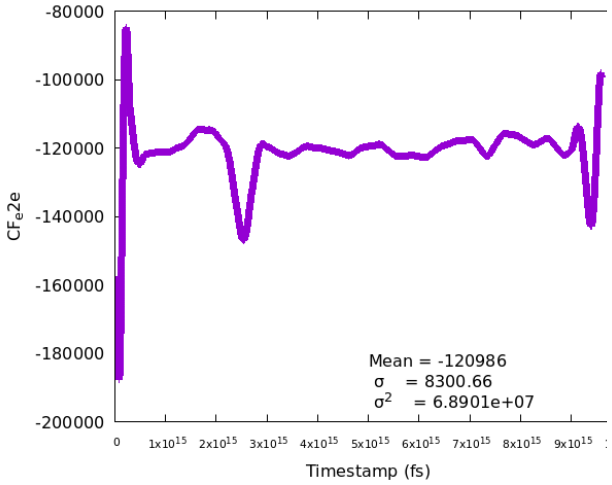


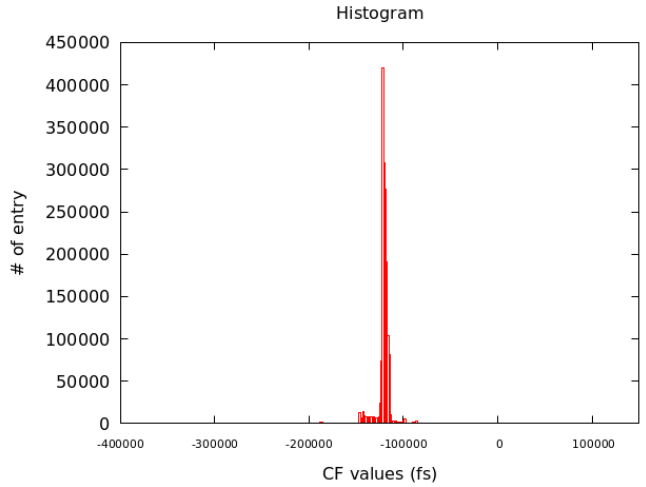


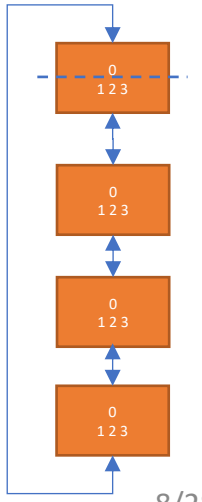
SW based timestamping (~50uS precision) provides proportional, microseconds precision for a three links network.

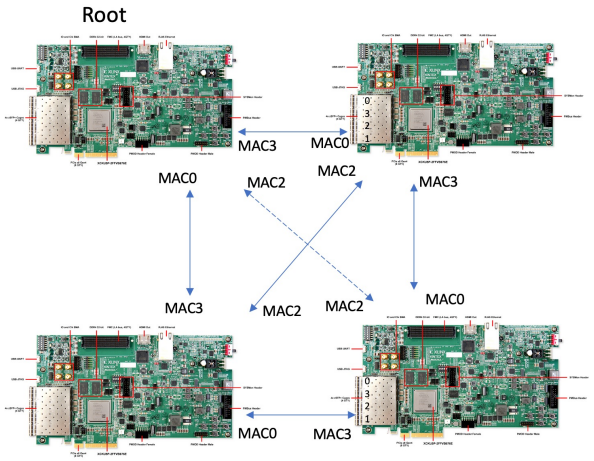
More tested topologies

4x25GE links test (ETDC timestamping)

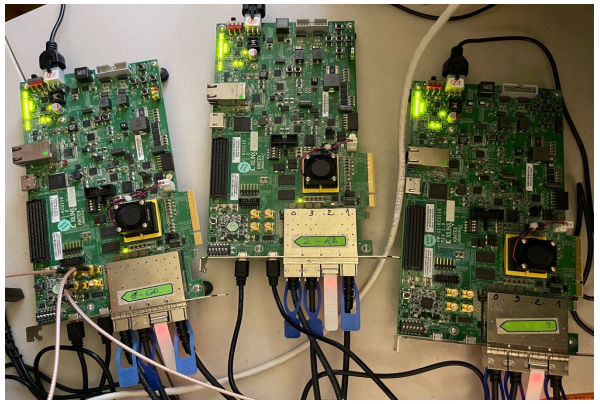


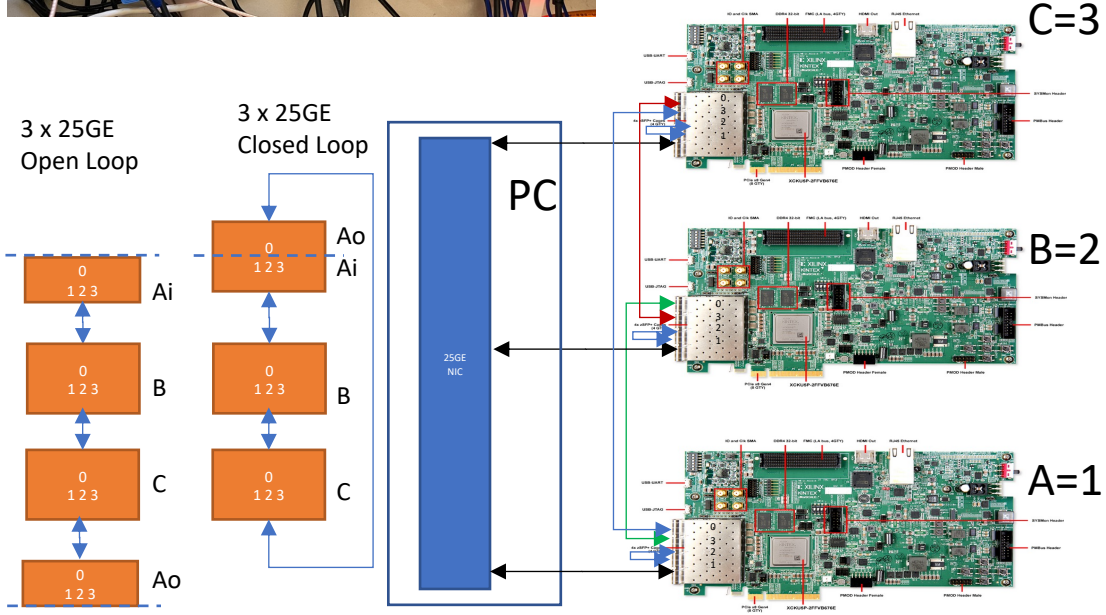






3x25GE links test (ETDC timestamping)





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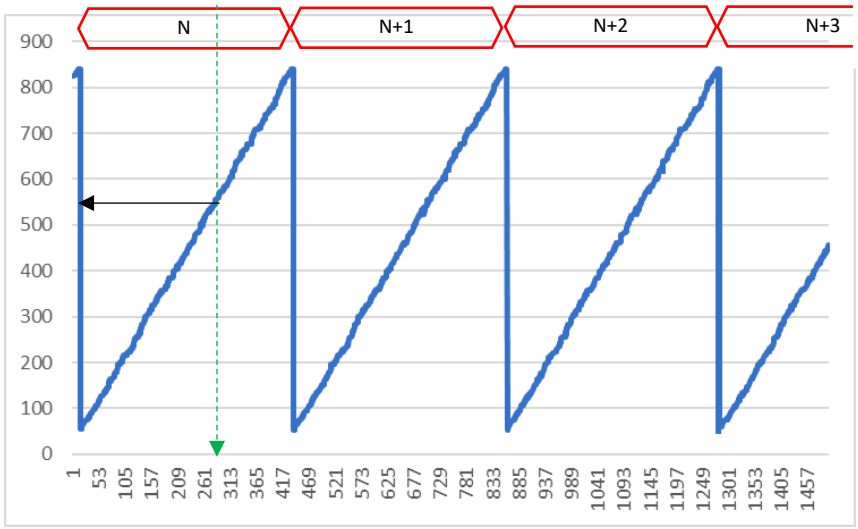
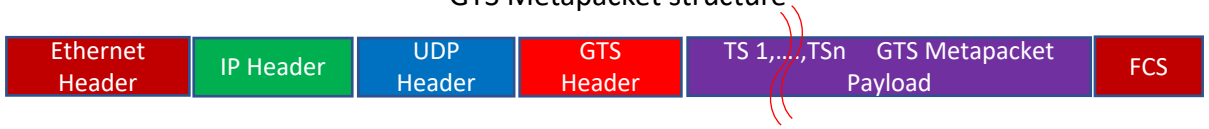
Ergodic TDC



Continuous conversion of time (horizontal axis) to the tap number (vertical axis) further converted into picoseconds by the internal Lookup table. The clock counter increments on the rising edge of the TDC latching clock

1. 2Gsamples/s
2. 500pS min sample to sample
3. Continuous acquisition
4. 7.5 to 0.5 ps precision (for practical limitations)
5. 64b to 32b per timestamp
6. 25GE optical network interfaces (1 to 120 ports)
7. Only valid timestamps are sent through metapackets
8. Metapacket payload has hundreds of TS
9. Both ends of the link can send metdapacket to a proxy for computing of CF(t)
10. Network timestamps are paired with packet ID (FCS(n))
11. FPGA implementation allows reconfigurable performance v. number of channels
12. Look Up Table (LUT) converts the tap# into actual calibrated delay to that tap

GTS Metapacket structure



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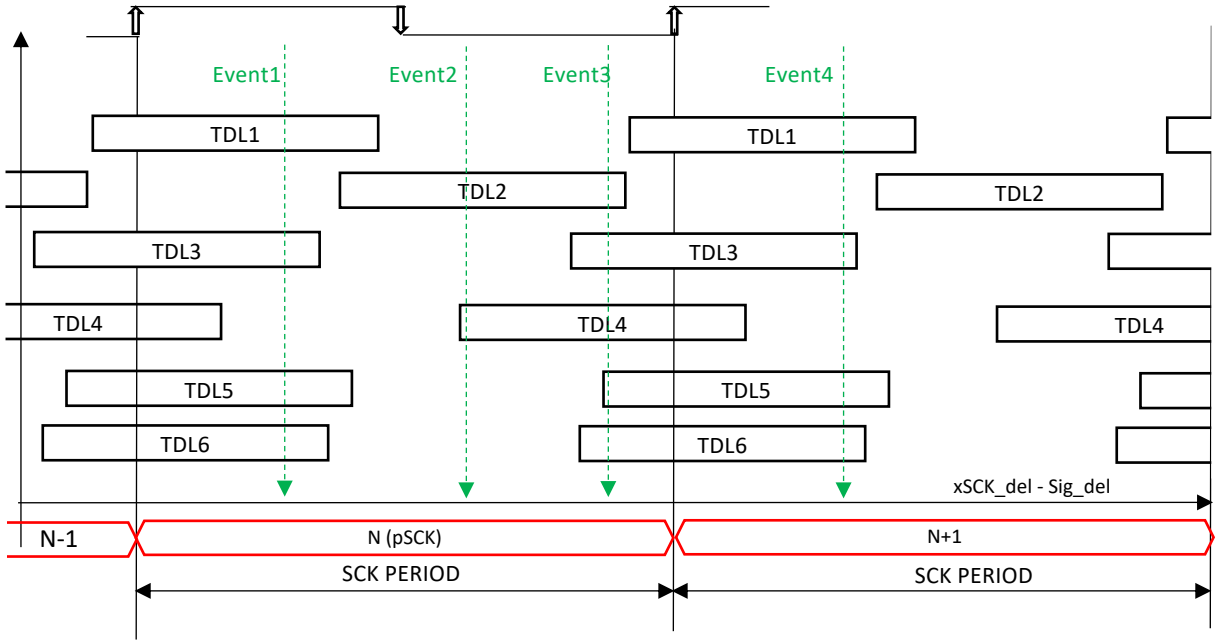
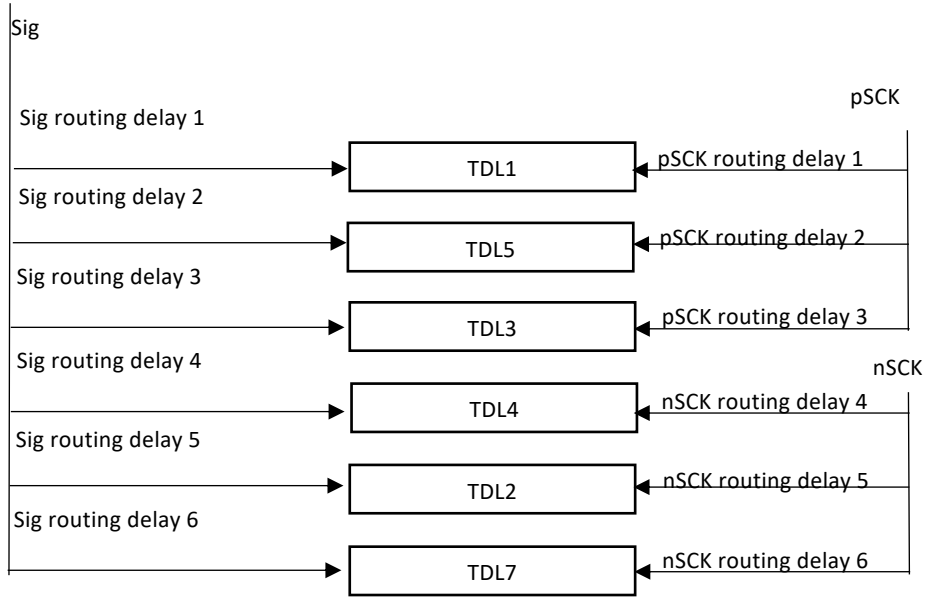
Ergodic TDC FPGA timestamping diagram



Events occurring at different time relative to SCK phase are captured by different number of TDLs, Ex: Event 1 is captured by 4 TDLs, while Event 2 by 2 TDLs. Two (or more) pSCK, nSCK phases, latch the TDL to cover the dead time intervals. ETDC FPGA identifies the TDLs which captured transitions, aligns the TDLs TS with xSCK-Sig delay offsets (TDL 2,4,6 are latched by nSCK) and performs an average.

Physical Tapped Delay Line routing diagram



The TDLs covering less then a SCK period are connected in parallel, but FPGA clock routing delay of the input signal and SCK, and the different phases of the latching SCK scatter their capture by a random offset (left diagram)

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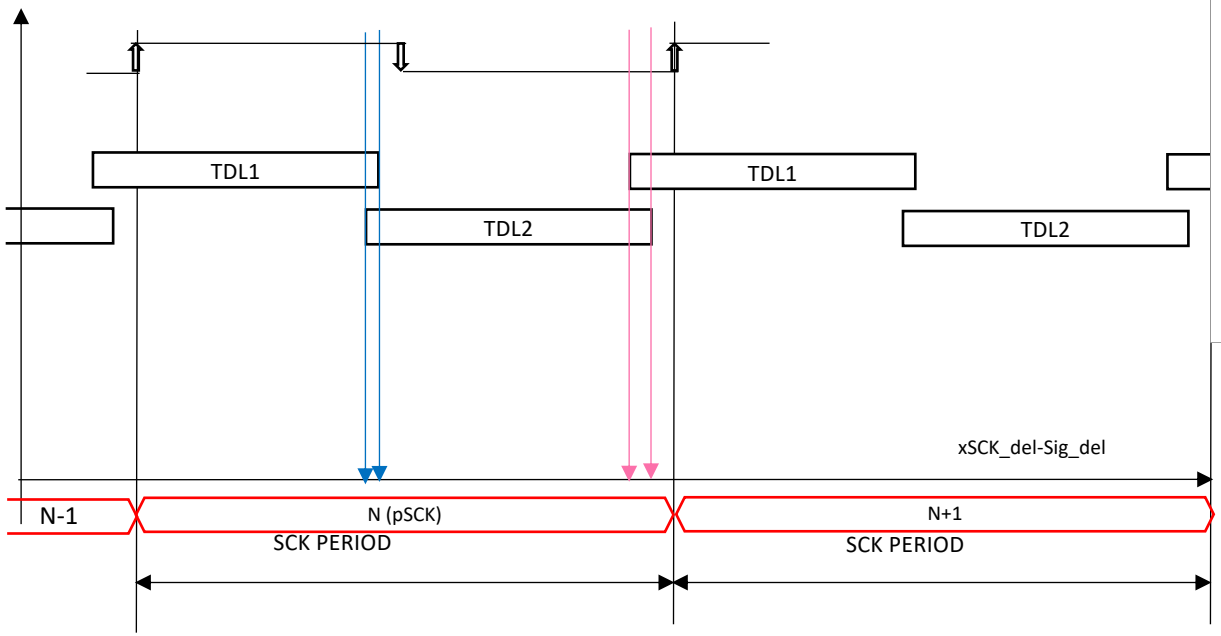
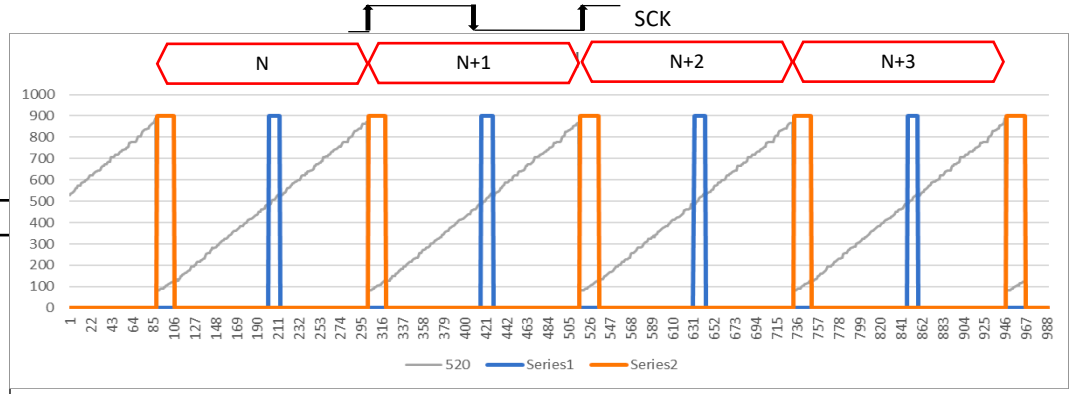
Mending TDL readings for Ergodic TDC's continuous operation





Implemented algorithm detects overlapping TDL sections and performs disambiguation or averaging

Continuous acquisition
No need for start/stop
No dead time
Fully numerical process

Calibration
There are several calibration processes:
1. Initial board HW calibration - factory
2. Traveling wave calibration - offline
3. Statistical calibration - run-time

Traveling Wave Calibration
Timestamped signal is the sampling clock with slight offset (ex 100ppM). Every SCK the transition is captured at a slightly different offset on TDL

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CONCLUSION

FPGA integrates Ergodic TDCs with a Network Packet Switch and latest optical links

- ETDC captures event transitions through groups of parallel TDLs latched by multiple phases of a local clock.
- ETDC has configurable precision for best use of FPGA resources for each experiment (8ps to 0.5ps)
- ETDCs uses the same local clock timestamp for both the Detector and the Network packet events.
- PacketETDC pairs timestamps with seceral FCS bits
- Integration of a packet switch on the FPGA
  - provides any network topology (mesh, tree, daisy chain)
  - eliminates cost, power, traffic delay, maintenance of third-party switches
  - Reduces experiment setup time
  - Provides the massive bandwidth for the network backbone of the entire facility

GTS Protocol Elements

- Uses numerical synchronization: TS generated from fixed, predictable oscillators, numerically corrected by CF(t)
- Determines a Correction Function CF(t) function of outbound local time, dynamically compensating HW drift
- Network GTY Serdes have deterministic latency which can correct asymmetric delay between directions
- ETDC timestamps are more then 40 times higher precision then PTP timestamps.
- A GTS Metapacket transports hundreds of TSs for 25 to 50 folds increase in bandwidth efficiency. PTP's handshake takes 4 packets to transport 2 timestamps while GTS performs blanket timestamping and aggregates 160 to 355 TSs per packet.
- The typical tree topology GTS network takes no bandwidth from upstream Physics data flow as the Metapackets flow downstream for processing.
- Synchronization is quasi instant using network data gathered during independent cycles typically 30ms to 300ms.

Looking for opportunity to deploy the time synchronous readout adapted to various requirements of research and production facilities

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Collaborations

FRIB

MICHIGAN STATE UNIVERSITY

MIT Lincoln Laboratory

ANALOG PHOTONICS

AIM photonics

NJIT

Brookhaven National Laboratory

Stony Brook University

Massachusetts Institute of Technology

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Thank you !

Looking forward to build together the Internet of Time (IoTi)

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SUPPLEMENT

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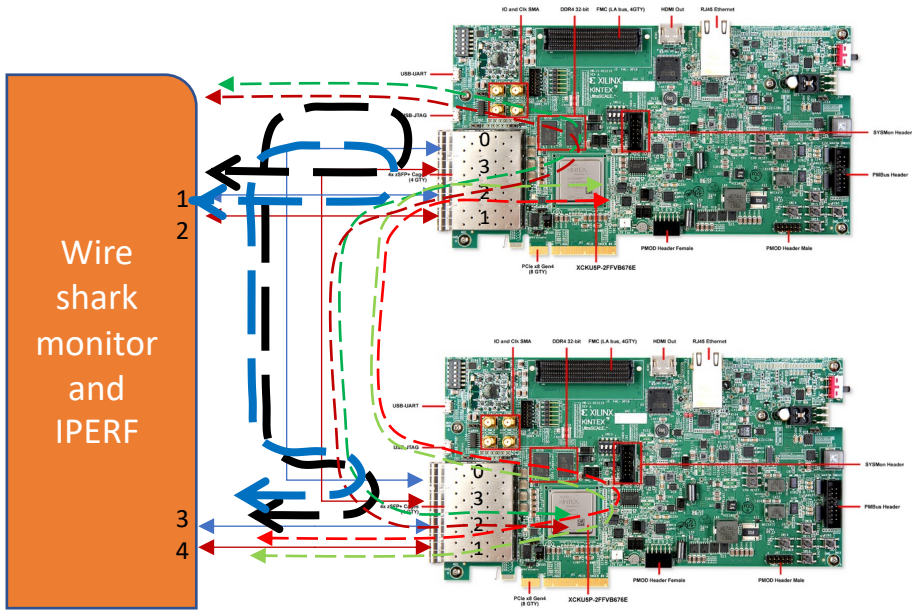
CAPCITY LOAD TESTS



Muxing test of PC IPERF generated traffic and metapackets for hits signals and network timestamps for synchronization

Load tests : Performed on 4 25GE NIC card on a Linux Workstation
Traffic was generated and received on all 4 ports of the NIC.
Metapackets for bursts of hits and for data packets were generated at each board and inserted in the NIC traffic before being sent to the other board and then to the NIC
Packet counters can be read at any port of the FPGA. There were no dectable lost packets

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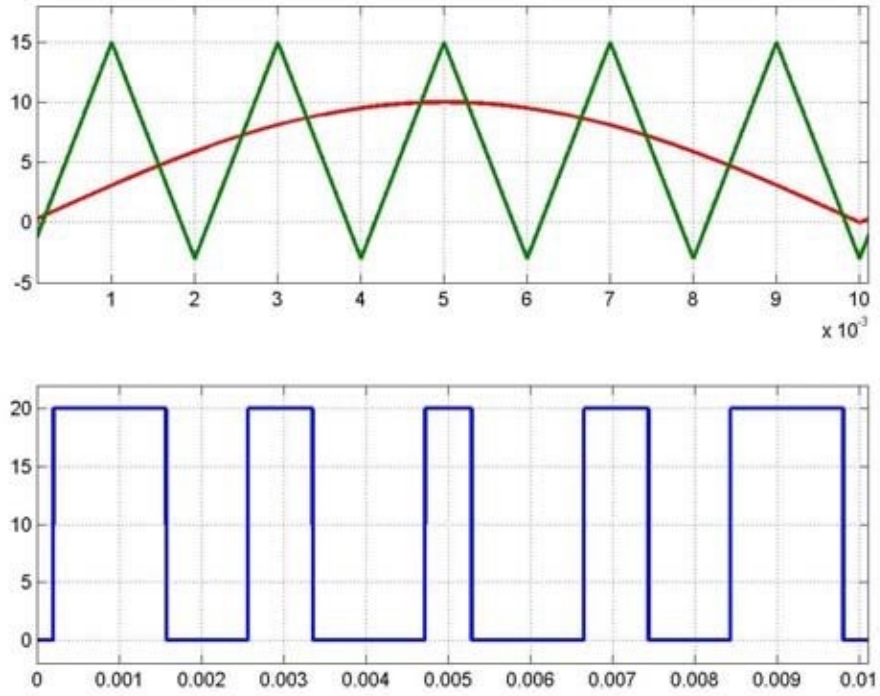
FUTURE ENHANCEMENT
ADC FUNCTION OF THE ETDC

A simple, radhard PWM frontend circuit ads ADC capability (12b/100Mbps) for

- high density channels,
- high linearity (implicitly calibrated through internal LUT)
- low power
- implicit event reconstruction
- lowest end to end system cost
- all other IPAG – facility wide network functionality



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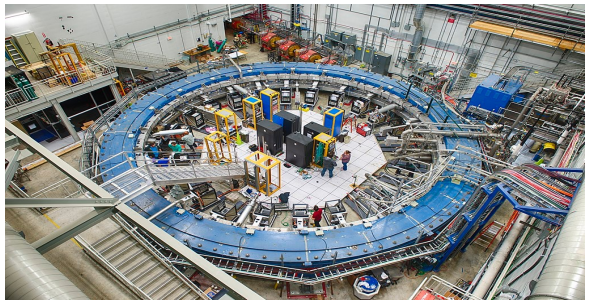
COMMERCIAL POTENTIAL

Micro Cellular Networks: 5G require sub nanosecond timing and higher bandwidth per fiber

- GPS no longer reliable (band conflict)
- GPS not available indoors
- ETDC and GTS provide the answer for in band timing synchronization
- The 5G 6G synchronization – at least 10% of the CAPEX of wireless business. Total yearly revenues, $5.5T



Global Positioning

- Replacement for GPS with precise propagation delay determination to the known radio node or station.

Medical Imaging

- Time to digital converter (TDC) with higher channel count and precision (MRI)

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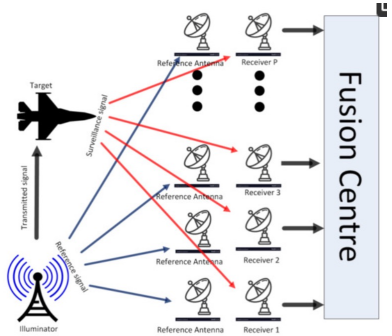
COMMERCIAL POTENTIAL (cont.)

Financial Transactions (Consolidated Audit Trail, SEC regulation)

- Outperforms IEEE 1588 which degrades with increased traffic and is vulnerable to cyberattack.
- GTS is stealth and stable with increased traffic

Military

- Radars
- Position, Navigation, and Timing (PNT)



Data centers

- Internet of Things (IoT)
- Unique picosecond timing essential for increase capacity without investment

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COMMERCIAL POTENTIAL (cont.)

Renewable Energy Sources

- Accurate time synchronization is essential for efficient transfer of energy to the power grid

General Instrumentation Require Precision Time Sources

- ETDC has one order of magnitude higher sampling rate and precision.
- GTS replace legacy IEEE 1588 at 5 order of magnitude better precision.