

Low Cost Data Acquisition Synchronization for Nuclear Physics Applications

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- Outline
 - The company and its capabilities.
 - Customers.
 - Success Story: LUX-Zeplin DAQ deployment.
 - Description of the Phase I project: Proof of principle.
 - Description of the Phase II project: The goal.
 - Phase II progress and achievements.
 - Future plans.

- The team: three physicists, a senior software engineer, a part time physicist, and a manager. We regularly work with a local EE consultant.
- We worked with several interns listed on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, Dark Matter search...

Our capabilities: Development of electronic instruments for Nuclear Physics.

- Electronic design (conception, schematic, board layout).
 - Typically we outsource the assembly, unless the board is really simple.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors: Embedded Linux or micro controllers.
- Algorithms for pulse processing.
- Algorithm implementation in the FPGA (VHDL, Verilog) and in embedded processors (Pascal, Python, C).
- Processing data from nuclear detectors of any kind.
- Development of simple detector assemblies using scintillators, PMTs, or SiPMs.



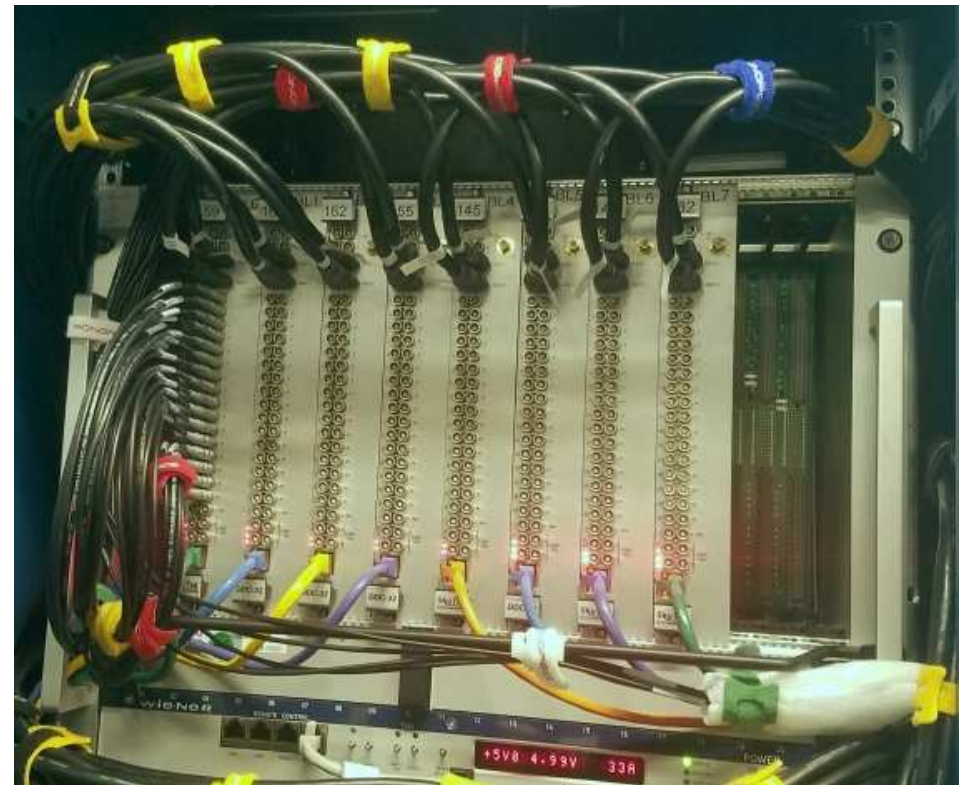
Success Story: LUX-Zeplin Data Acquisition

- LUX-Zeplin is the world's largest Dark Matter Search liquid xenon two-phase TPC (10 ton LXe).
- We delivered **1,632 channels** of the DAQ electronics to the LZ Collaboration.
- **No bad channels.**
- The DAQ was deployed in Sanford Underground Research Facility at -4850' in Summer 2019.
- No problems were found with the DAQ while collecting signals since November 2019.
 - Continuous operation since deployment without any failures.

26 **Logic Boards**, sixteen 3.2 Gbps links each



51 **Digitizers**, 32 channels each



The Overview of the SBIR Project

GRETINA and Digital Gammasphere (DGS) both use LBNL 10-channel digitizers.

- The hardware was still in good shape.
- The legacy **VME interface was limiting the data throughput**.
- Spartan-3 **FPGAs were almost full** with the present firmware (more than 90%). It makes the new firmware developments quite difficult.

How this problem or situation was addressed.

- **New** digitizers with a **new FPGA**, on-board **Linux**, and fast streaming readout (1 Gbps and **10 Gbps per digitizer**). VME was eliminated.
- The digitizers would be **backward compatible** with the GRETINA & DGS and **forward compatible** with GRETA.

In Phase I we delivered a proof of principle using our 40-channel prototype digitizer.

- We performed measurements with **Gammasphere**, using our 40-channel prototype **in parallel** with the present LBNL DAQ electronics. We established that our prototype **performed on par** with the established LBNL units.

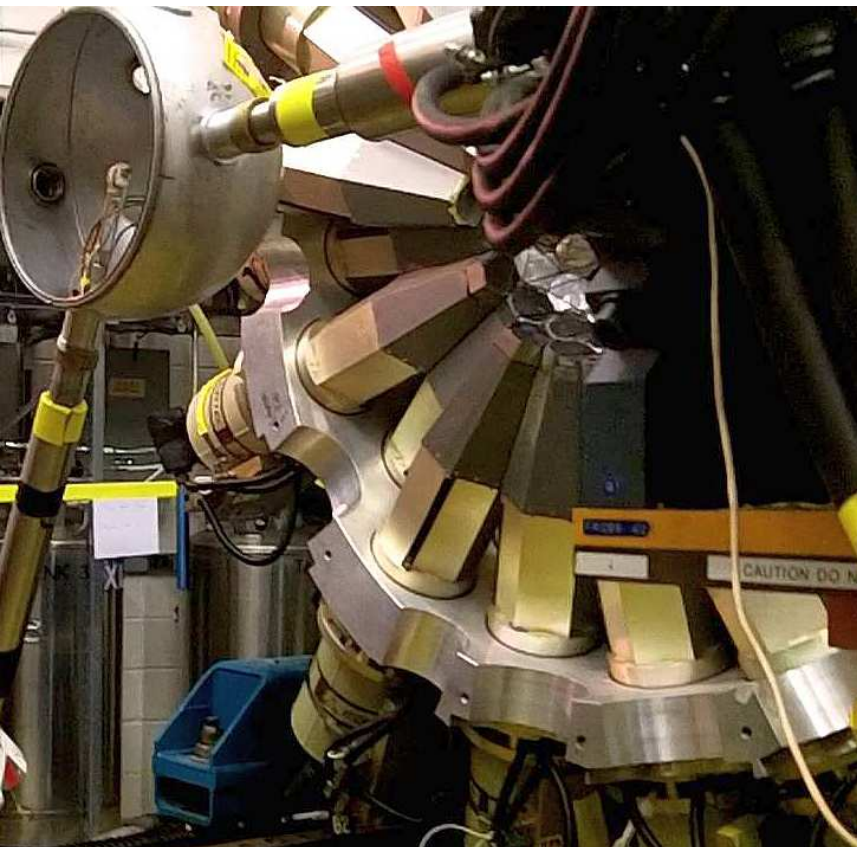
Test With Digital Gammisphere (DGS)

Gammisphere consists of 108 Compton-suppressed high-purity germanium (HPGe) detectors surrounded by the BGO anti-Compton shields.

DGS is equipped with the LBNL [digital electronics](#) originally developed for GREY. Each LBNL digitizer provides 10 channels, 14 bits @ 100 MSPS.

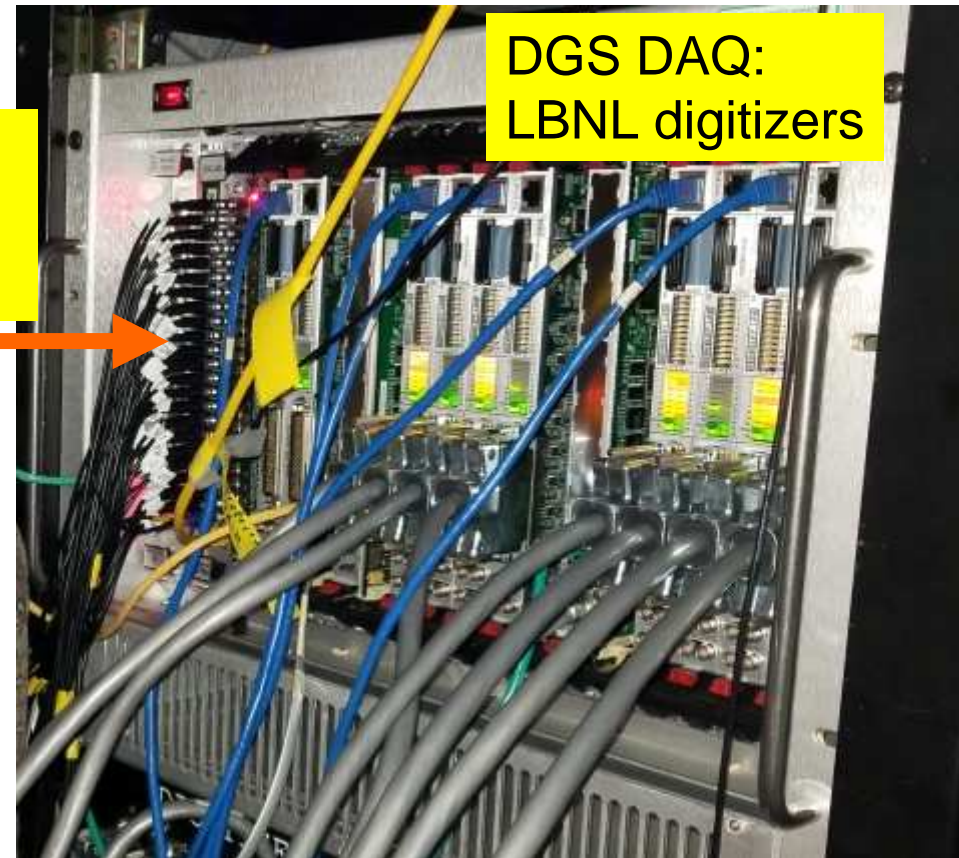
We used [Skutek 40-channel prototype](#) to measure the same signals in parallel.

Gammisphere Detector Array



Skutek
40-channel
prototype

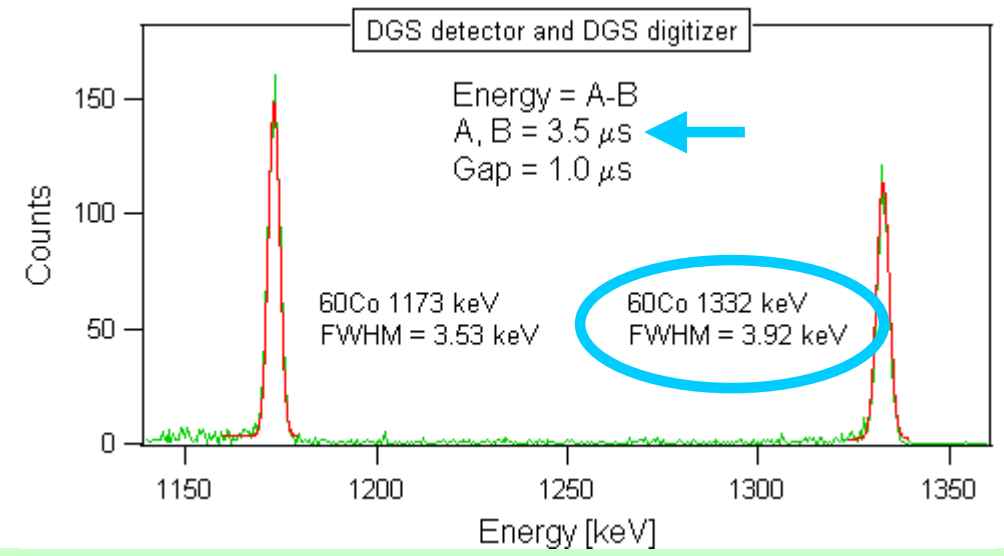
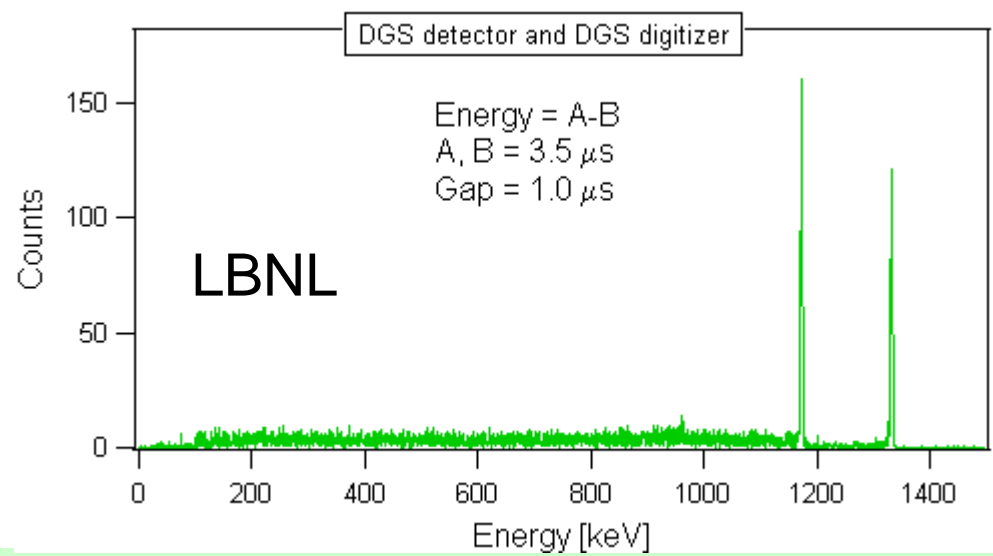
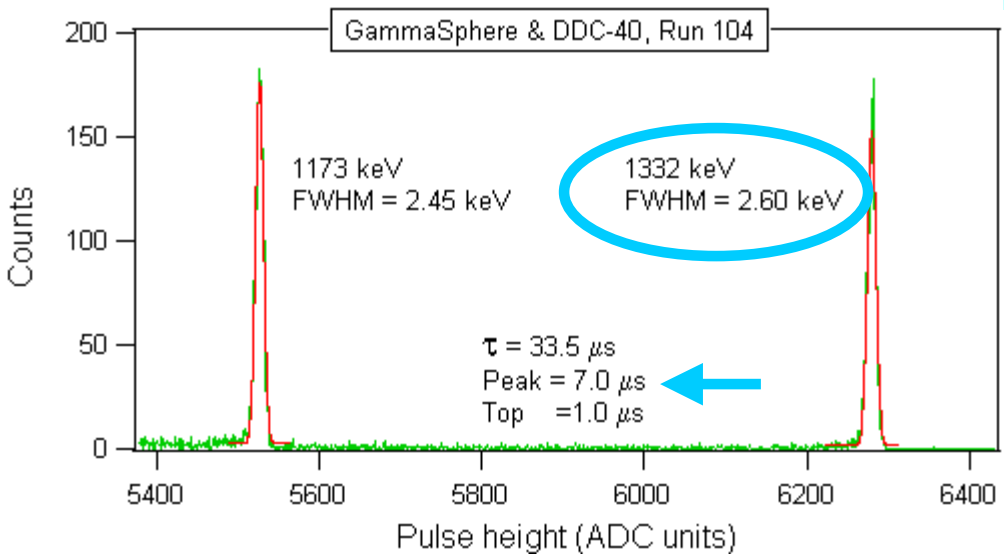
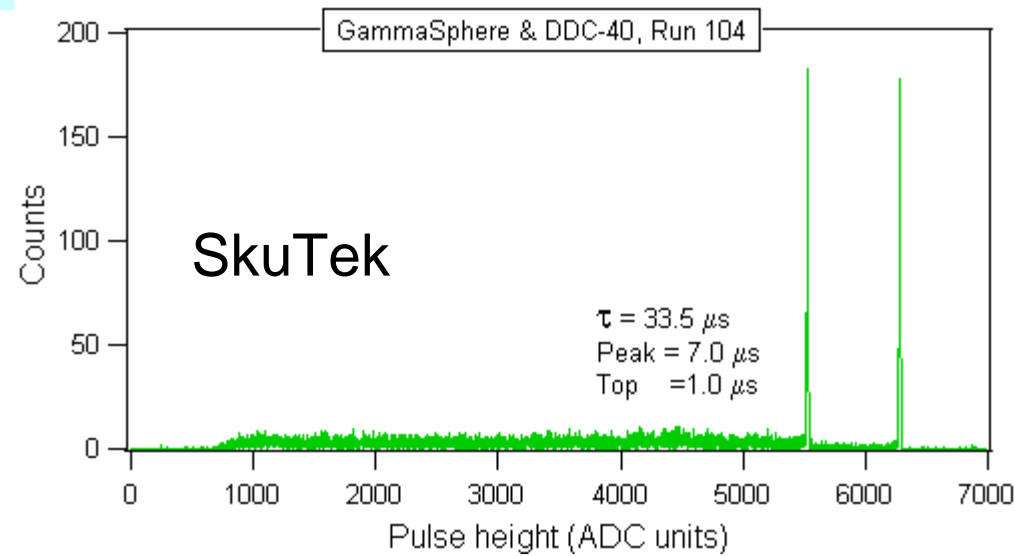
LBNL & Skutek Electronics



DGS DAQ:
LBNL digitizers

Phase I Was a Great Success

- Comparing the energy resolution with Co-60 and Gammasphere --> **PASS!**
- The resolution achieved with both devices was the same with equal running sums. We achieved a SQRT(2) better resolution when we applied 2 * longer running sums.



Phase II Project

The challenge:

- How can we **interface** and **integrate** SkuTek digitizers with the established GRETINA or DGS environments, which are providing **clock**, **trigger**, and **time stamp synchronization** among many digitizers and logic modules?

How this situation was addressed:

- We added the GTCL - compatible optical link on the Rear Transition Module (RTM).
- We adopted the GRETA Trigger Command Link (GTCL), **compatible** with **DGS TTCL**.
- We replaced VME with **gigabit Ethernet** (1G copper and **10G optical**).
- We used on-board **Linux** for setup and control over Ethernet.
- **We collaborated** with the ANL Physics Division on GTCL and DSP firmware development.

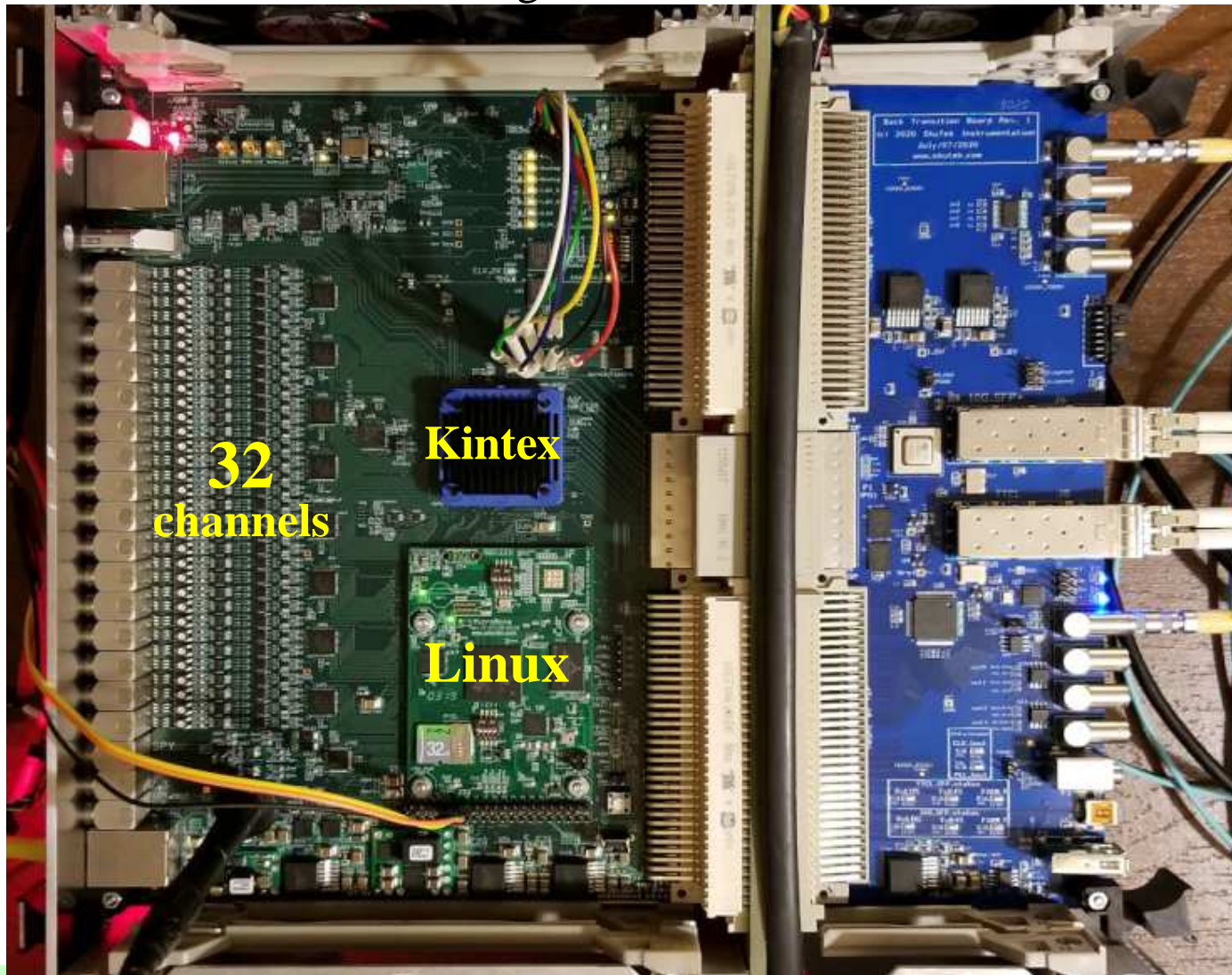
32-Channel Digitizer With the Rear Transition Module

4 Gbps over the GTCL optical link, and **10 Gbps** over the optical Ethernet link.

Both links will be present in every digitizer. Readout will **not** be shared among digitizers.

NEW 32-Channel Digitizer

NEW Rear Transition Module (RTM)



1 GbE (FPGA)

Digital HDMI

32 Analog
inputs

2 Analog
outputs

1 GbE (Linux)

4 * NIM in

10 G Ethernet
Optical GTCL
**Compatible with
GRETA**

4 * NIM out

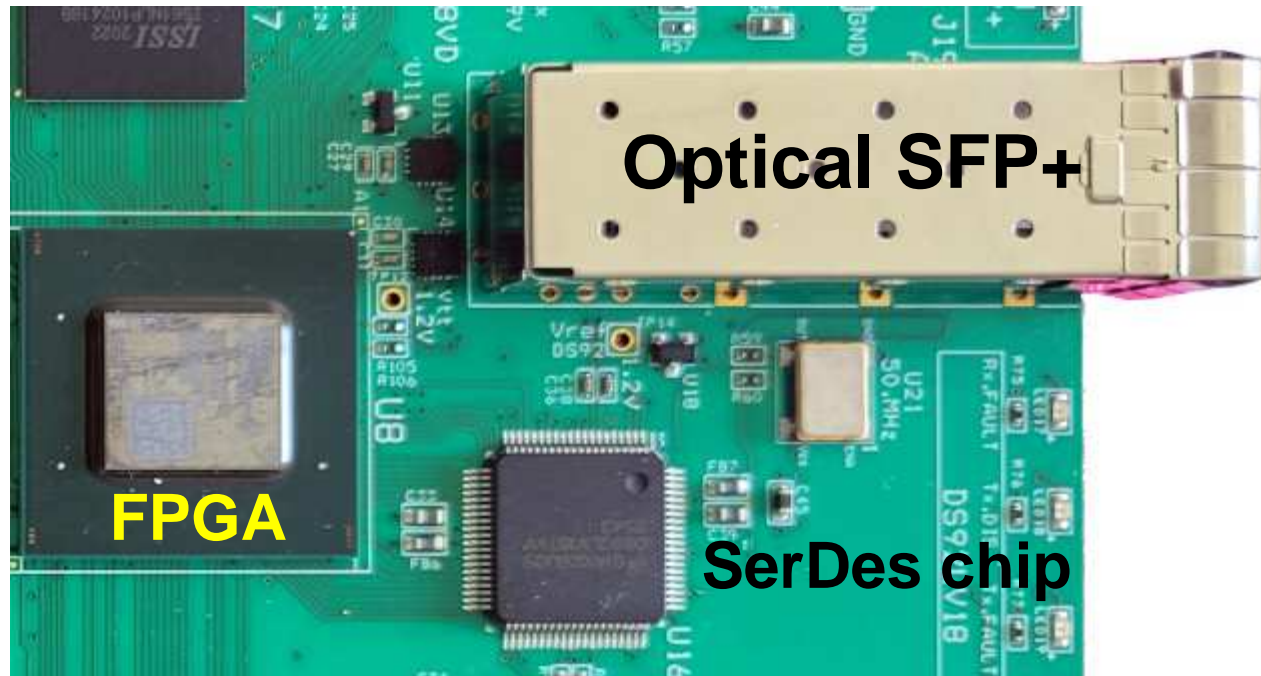
Serial UART
(Linux)

How to connect dozens of digitizers into a coherently triggered DAQ system?

The answer: DGS / GRETA Trigger Command Link (GTCL)

GTCL was designed by John Anderson, Argonne National Laboratory

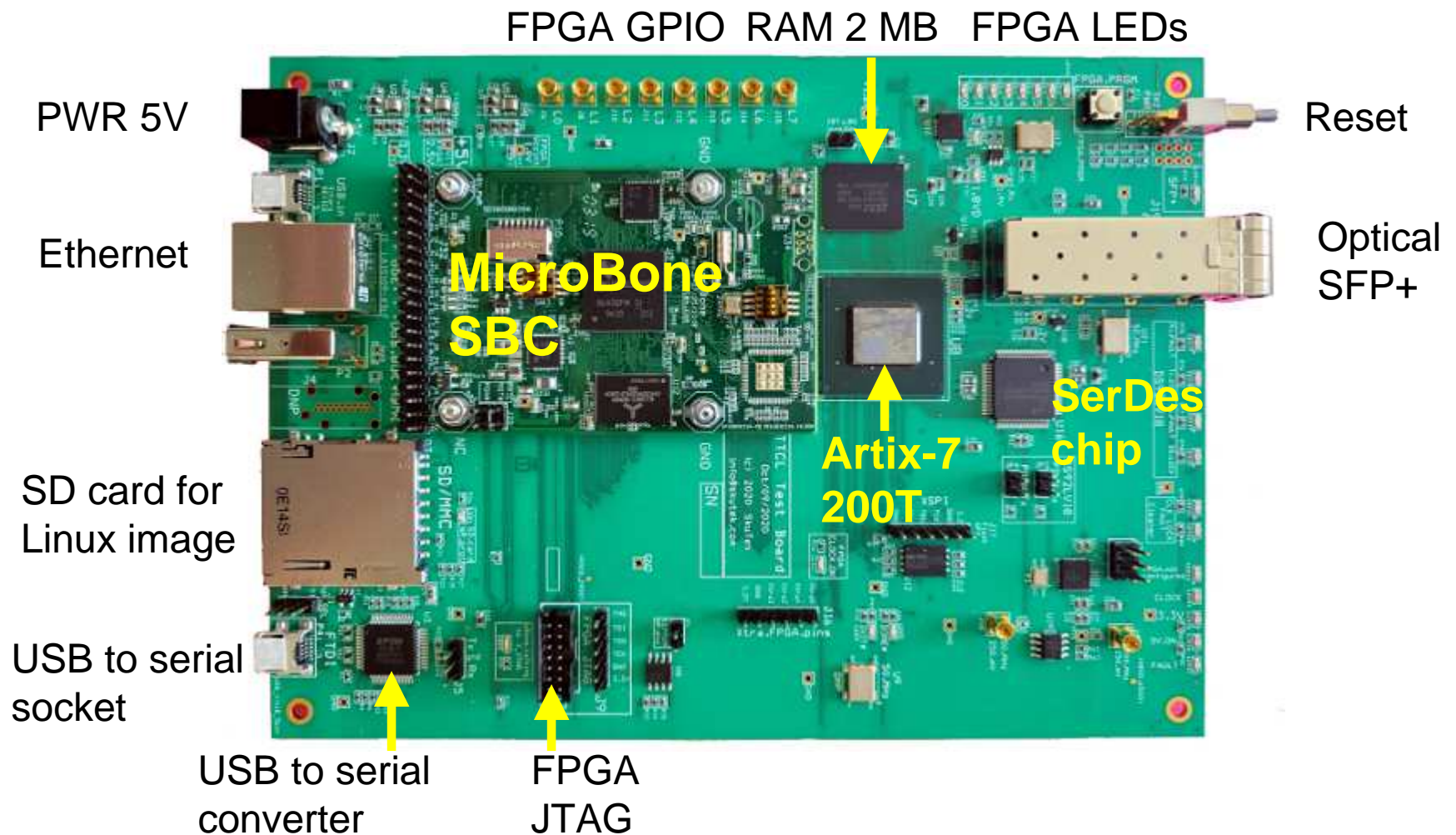
GTCL Tester board layout by WS, SkuTek Instrumentation



GTCL Implementation @ SkuTek

We created the GTCL Development Board to **avoid traveling** to ATLAS during COVID.

- MicroBone Single Board Computer (SBC) is setting up and controlling the GTCL link.
- We developed GTCL communication with the digitizer using this board.



GTCL shares the hardware with the GRETINA / DGS *Time and Trigger Control Link* (TTCL). GTCL / TTCL provides **clock, timestamp, trigger, and control** to the digitizer modules. **Hundreds of digitizers** can be served with a **fixed-latency** tree of GTCL fan-outs.

In addition to distributing the trigger, GTCL is also distributing the clock, much like White Rabbit.

1. The **reference 50 MHz clock** will reach the ADCs with about **~100 ps** jitter, depending on the clock distribution tree. Tens of ps possible after careful board design optimization.
2. All the **timestamps** in the entire system can be reset, using a single GTCL command.
3. The **trigger condition** is distributed among all digitizers in all auxiliary detectors.
4. GTCL can also distribute Run Control messages embedded in its frames (start, stop, etc.).
5. GTCL **does not require run-time programming**. All the GTCL specifics are implemented either in the SerDes hardware, or in the VHDL which is driving the SerDes data pins.
6. TTCL (the GTCL predecessor) **was proven sufficient** in dozens of experiments at ATLAS.
7. GTCL **does not rely on any third parties**, consortiums, or external bodies.
8. GTCL hardware is **simple** and **frugal** (as shown in the previous slide).

DSP Firmware **was ported** from the LBNL 10-channel digitizer **to SkuTek 32-channel digitizer** under SBIR subcontract with ANL.

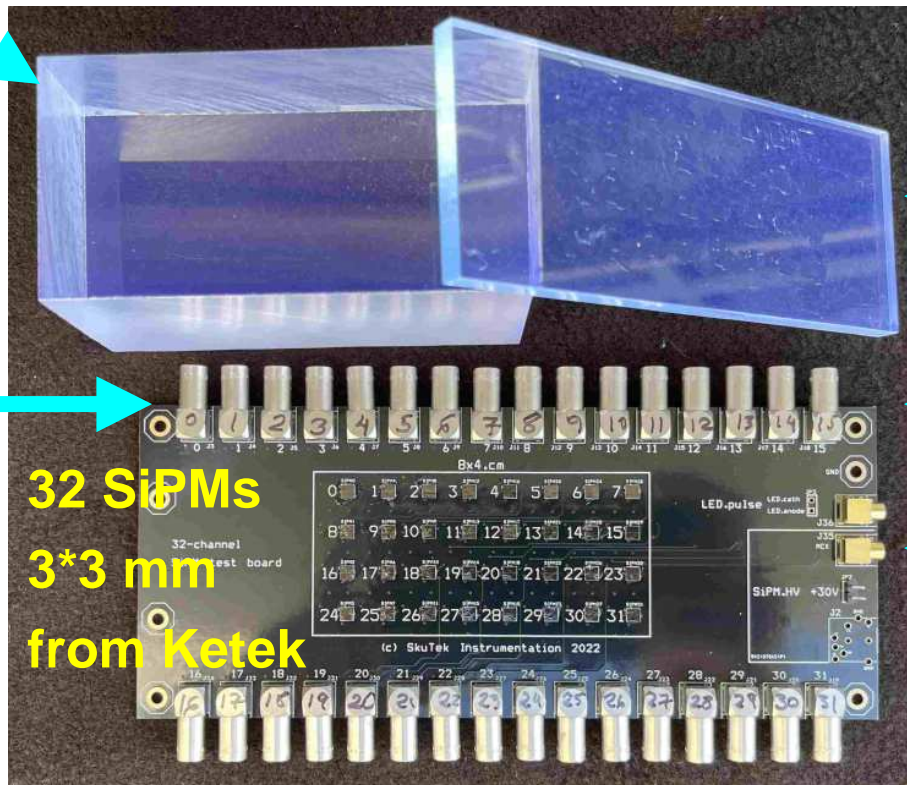
1. ANL DSP pipeline firmware was expanded from 10 channels to 32 channels and integrated into the SkuTek firmware.
 - The ANL firmware was used with LBNL digitizers at ATLAS (DGS, DFMA, X-Array, HELIOS, MUSIC). Our digitizers **will be ready** for all of these!
2. Registers were implemented to control all parameters of each channel individually.
3. Reception of clock and commands **from** the GTCL / TTCL trigger system was demonstrated.
4. Streaming of digitizer data **to** the GTCL / TTCL trigger system was completed.
5. Discriminators and energy measurement were demonstrated with NaI(Tl) and a test stand.
 - **Status:** The development has been completed. We visited ATLAS and tested the digitizer + RTM with real detector signals in the ATLAS environment.

We Built Our Own 32-Channel Signal Source

- We did not have access to a 32-channel detector in Rochester.
- ATLAS has detectors. But we could not travel...
- We built **our own 32-channel detector** for testing coincidences.

Bicron BC412, 5 cm * 10 cm * 2.25" from E-bay for \$45 a piece.
Cut to size by Tom Hall (iradinc on E-bay).

32-channel
SiPM board.
Developed by
Skutek.



32 SiPMs
3*3 mm
from Ketek

6 mm piece
of BC412

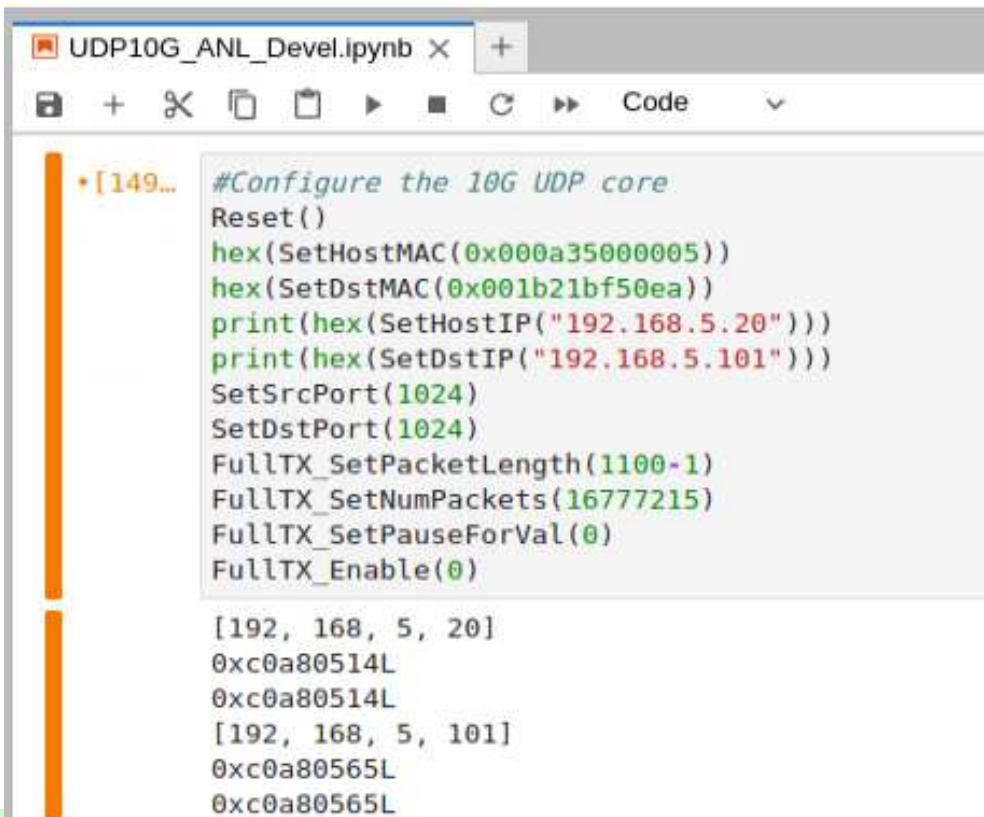
32 individual
LEMO outputs

SiPM bias
+27 V

Digitizer Control Software

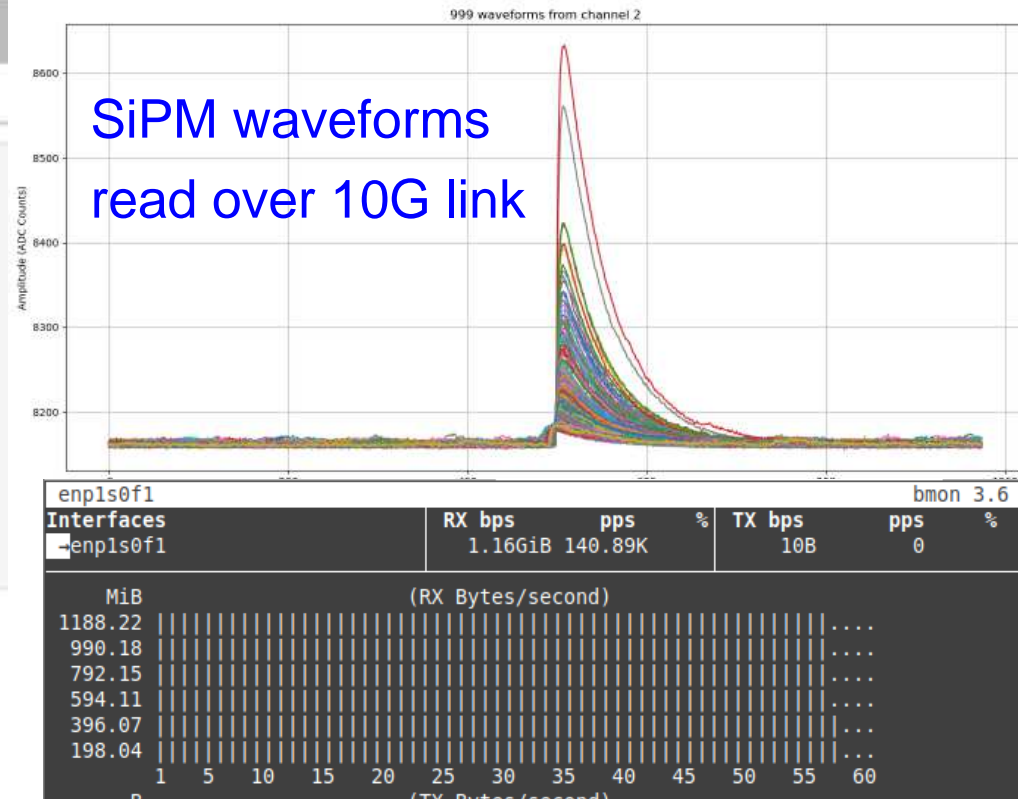
Software is primarily developed by SkuTek.

- **MicroBone** SBC is setting up and controlling the FPGA registers.
- **Jupyter** is the primary software controlling our products.
 - Jupyter is “remote Python” executed on the board over Internet under Linux.
 - In addition, we also used a lower level Remote Python Call (RPLYC).
- The on-board Linux can also run **EPICS**. See the next slide.
- **Status**: We keep adding new functions to both the software and the firmware.



```
UDP10G_ANL_Devel.ipynb X +
+ [149... #Configure the 10G UDP core
Reset()
hex(SetHostMAC(0x000a35000005))
hex(SetDstMAC(0x001b21bf50ea))
print(hex(SetHostIP("192.168.5.20")))
print(hex(SetDstIP("192.168.5.101")))
SetSrcPort(1024)
SetDstPort(1024)
FullTX_SetPacketLength(1100-1)
FullTX_SetNumPackets(16777215)
FullTX_SetPauseForVal(0)
FullTX_Enable(0)

[192, 168, 5, 20]
0xc0a80514L
0xc0a80514L
[192, 168, 5, 101]
0xc0a80565L
0xc0a80565L
```

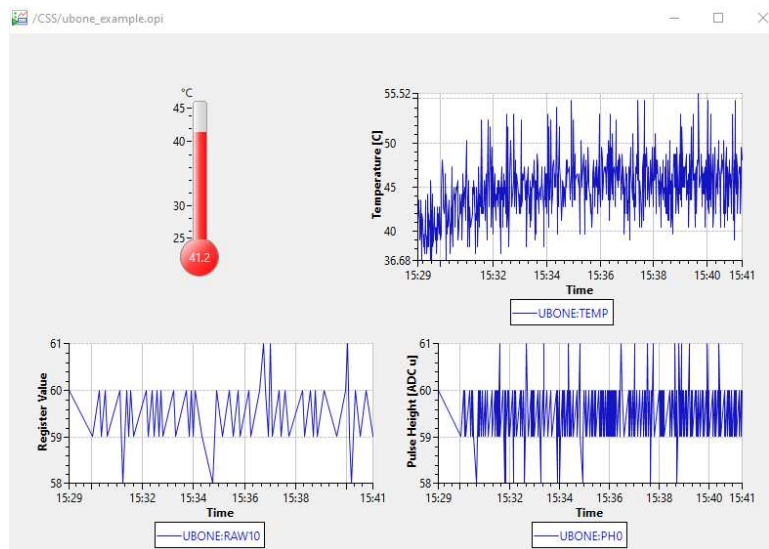


Experimental Physics and Industrial Control System (EPICS) [1] is used to control the DSP

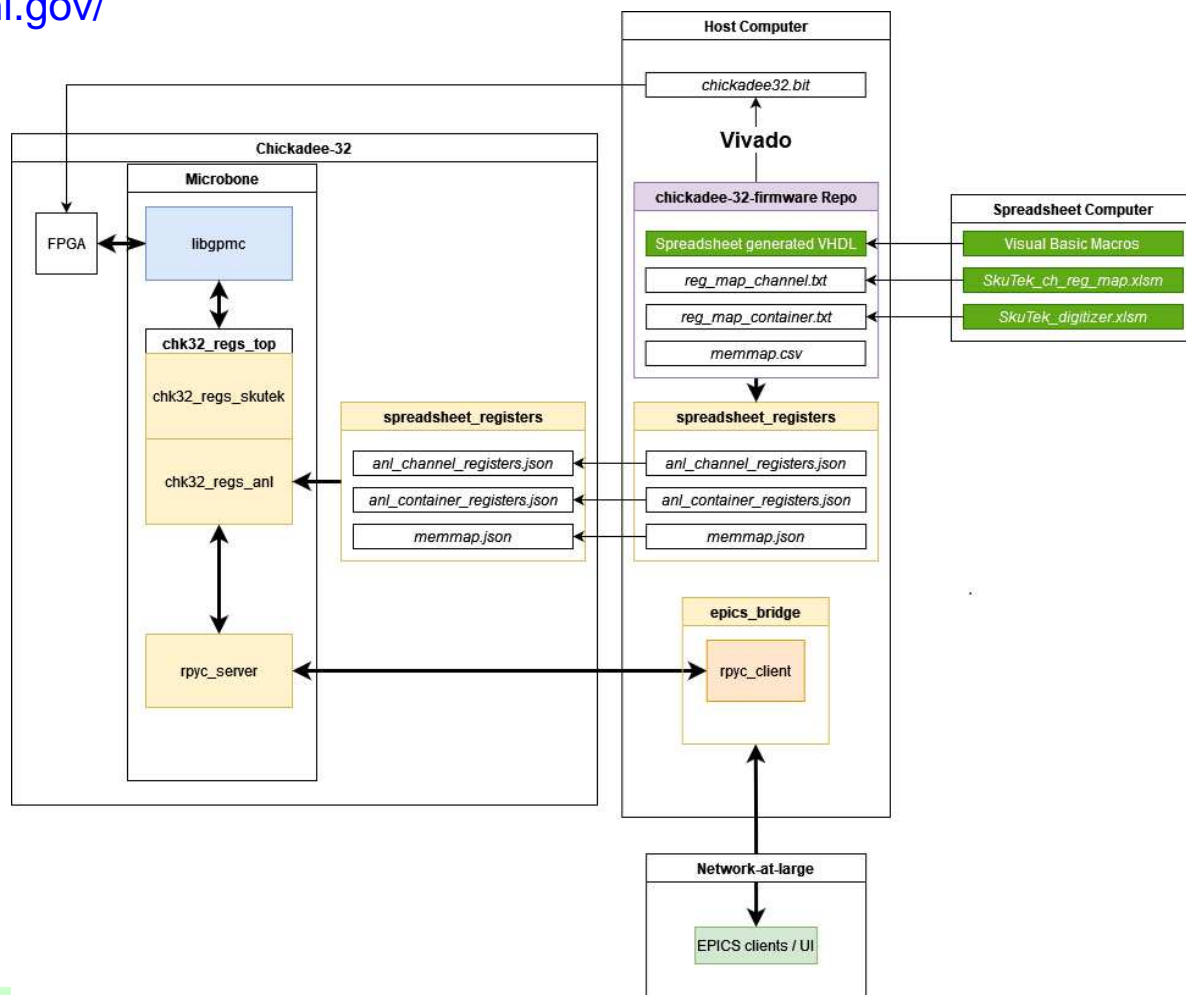
We expanded the EPICS database to include all internal parameters used in the firmware for individual channels consistent with existing Digital Gammasphere and GRETINA implementation

This also can be utilized as a direct Python API to talk to individual digitizers

[1] EPICS is documented at <https://epics.anl.gov/>



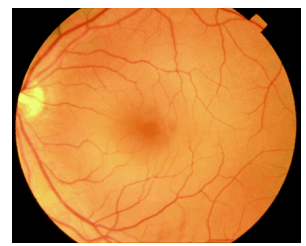
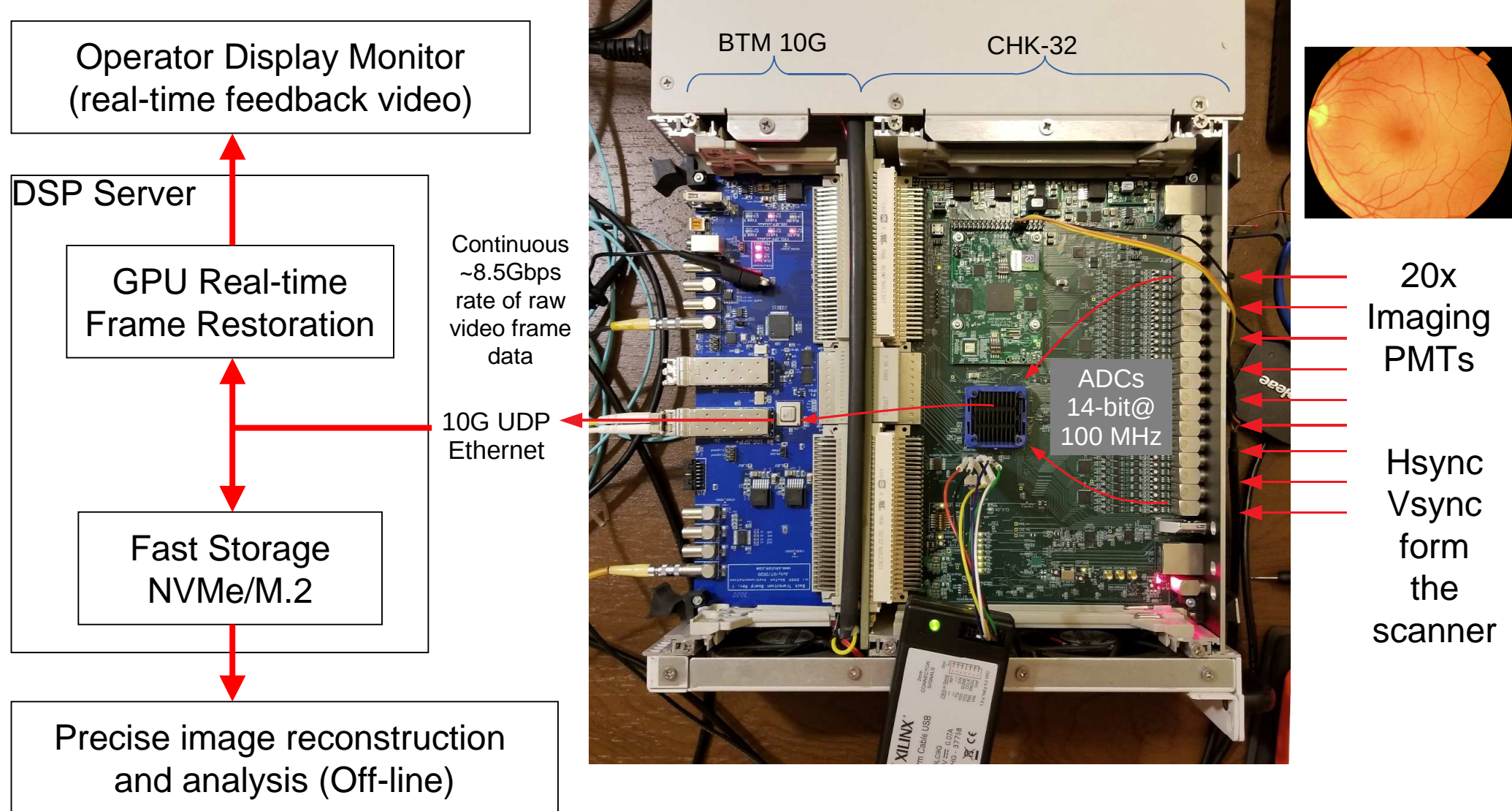
UI widgets can be deployed to track the relevant parameters in real-time



- Both 1G and 10 G streaming were completed.
- The data packets are streamed with **UDP Protocol** directly from the FPGA fabric.
- 1G / 10G data streams are using GRETA / DGS header format.
- Our data streams will be **seamlessly received** and merged with other GRETA / DGS data.
- 10 G streaming is used with Phase II *Data Management for High Speed, Distributed Data Acquisition* (DE-SC0021502) awarded to SkuTek, described by Jeff Maggio in his talk.
- **Status:**
 - 1G streaming was **extensively used** by the LUX-Zeplin experiment.
 - 1G GRETA / DGS formatting is **finished**.
 - Both 1G and 10G development was **completed**.
 - 10G streaming is now used in DE-SC0021502.
 - 10G streaming is also used for biomedical research project @ UofR.

Application Outside Nuclear Physics

CHK-32 will be used for Adaptive Optics Fluorescence Image Scanning Ophthalmoscopy at University of Rochester. Credits: Yongyi Cai, David Williams, Juliette McGregor, Eryk Druszkiewicz



Summary

- **Phase I:** We tested our 40-channel prototype digitizer with HPGe GammSphere detectors.
 - Pulse height resolution was **equivalent** to LBNL digitizers.
 - The **success** led to the Phase II collaboration with the ANL.
- The goals of **Phase II:**
 - **Integration** of the digitizers into the ATLAS DAQ, using the GRETA Timing and Command Link (GTCL), **back compatible with previous TTCL**.
 - **Fast readout** using 1G or 10G Ethernet links directly from the digitizers.
 - Setup and **monitoring** using the on-board **Linux**, separate from the fast readout.
 - **Achieve operation** of our prototypes in the ATLAS environment (after the pandemic).
- **Achievements:**
 - **Redesigned** the digitizer to provide 1G Ethernet in front, and P0 connector for the back.
 - **Developed** the Rear Transition Module with the GTCL and 10G optical links.
 - **Achieved** the GTCL design throughput @ 4 Gbps, using the optical SFP+ module.
 - **Developed** the GTCL Test Board to continue work despite travel restrictions.
 - **Developed** Jupyter control software.
 - **Developed** an EPICS example running on Microbone. (EPICS is used at ATLAS).
 - **Ported and tested** the ANL DSP and GTCL firmware to Skutek digitizer.

Joanna Klima, Jeffrey Maggio, David Miller, James Vitkus

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John Anderson, Michael Oberling,
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Consultant: Eryk Druszkiewicz

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