DOE-Nuclear Physics SBIR/STTR Exchange Meeting August 2015

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Nuclear Physics Instrumentation: Position Sensitive Charge Particle and Gamma Ray Tracking Devices (SBIR Topic: DOE 2013 – 42b)

Digital Silicon Photomultiplier Array Readout Integrated Circuits

VOXTELOPTO

Outline

- Brief Introduction to Voxtel
- Overview of Problem/Opportunity
- Readout Circuit Technical Discussion
  - SPAD device design and operation
  - Active quenching circuits
  - DSPAD prototype characterization results
  - Sensor specifications
- Summary and Questions

About Voxtel Companies

- Founded 1999
- 50 employees summer 2015 (30% PhD, 80% Advanced Degree)

Voxtel Opto (Beaverton, Oregon)

- Avalanche Photodiode (APD) and PIN Detectors and Arrays
- Eyesafe Pulsed Laser Transmitters
- Rangefinders, 3D Imaging, LADAR, and Electro-Optic Systems
- Readout Integrated Circuits (ROICs)
- Active & Act./Passive Focal Plane Array (FPA)

Voxtel Nano (Eugene, Oregon)

- Nanotechnology Technologies Group
- Nanocrystal VIS-SWIR-Thermal IP Imaging Products
- Analytical Facilities (HRTEM, SIMS, XRD, UPS/XPS)

Vadient Optics (Corvallis, Oregon)

- Spun out in 2013
- Inkjet Printed Solid Freeform Fabrication of GRIN Optics

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VADIENTOPTICS

SBIR Program Summary

Statement of Problem

The need for ever more sensitive, compact, rugged, and inexpensive optical sensors is particularly acute in the fields of homeland security, biological sciences, nuclear medicine, astronomy, and nuclear/high-energy physics.

- Applications like fluorescence and luminescence photometry, absorption spectroscopy, scintillation readout, charged particle detection, and Cherenkov imaging require extremely sensitive optical sensors to operate in space-limited and adverse environments.
- Existing detector technologies include: photomultiplier tubes (PMTs), microchannel plate photomultiplier tubes (MCPMTs), silicon photomultipliers (SiPM), **and single photon avalanche detectors (SPAD)**

Program Objectives

- Complete specification, design, and layout of the large format Digital SPAD sensor.
- Fabricate DSPAD readout, capable of being utilized as readout integrated circuit (ROIC) or monolithic sensor.
- Electrically and optically characterize the sensor.

Program Contacts

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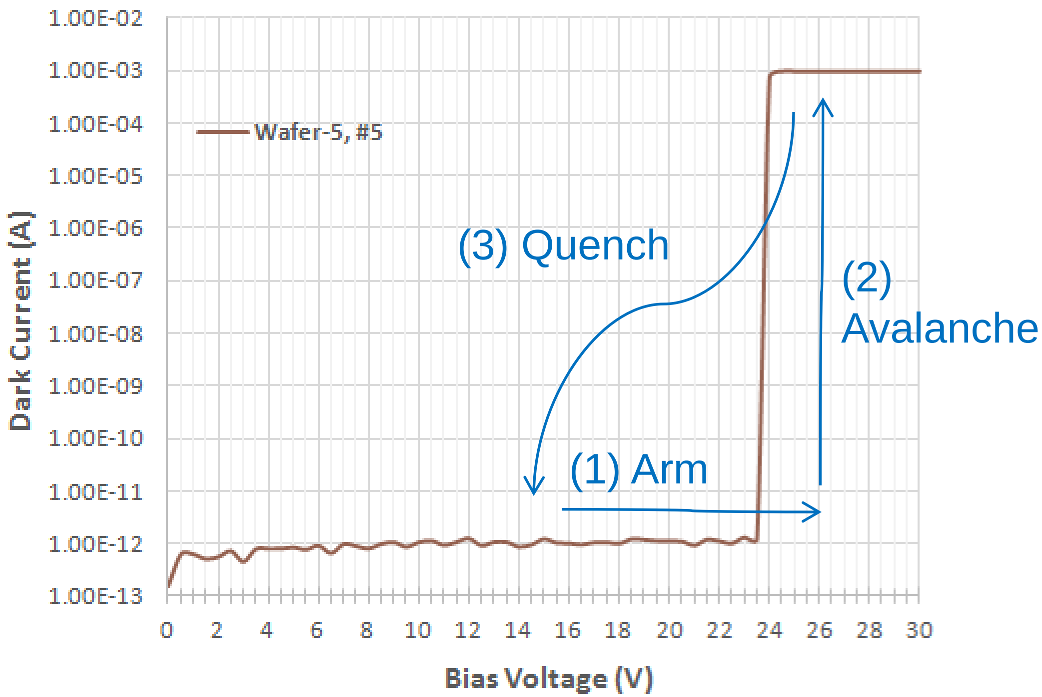
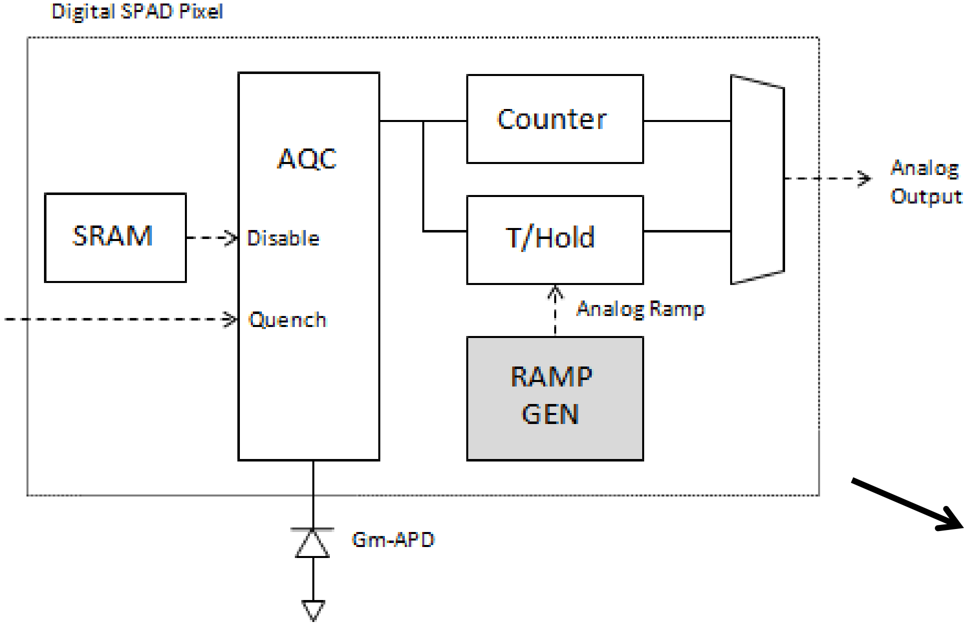
Geiger Mode SPAD Operation

1. Reverse bias is applied to photodiode beyond breakdown potential of device, arming the detector.
2. A photo- or thermally-generated carrier is collected in the junction, resulting in avalanche current in device.
3. Avalanche current is sensed and photodiode reverse bias is reduced (quench) to protect device.

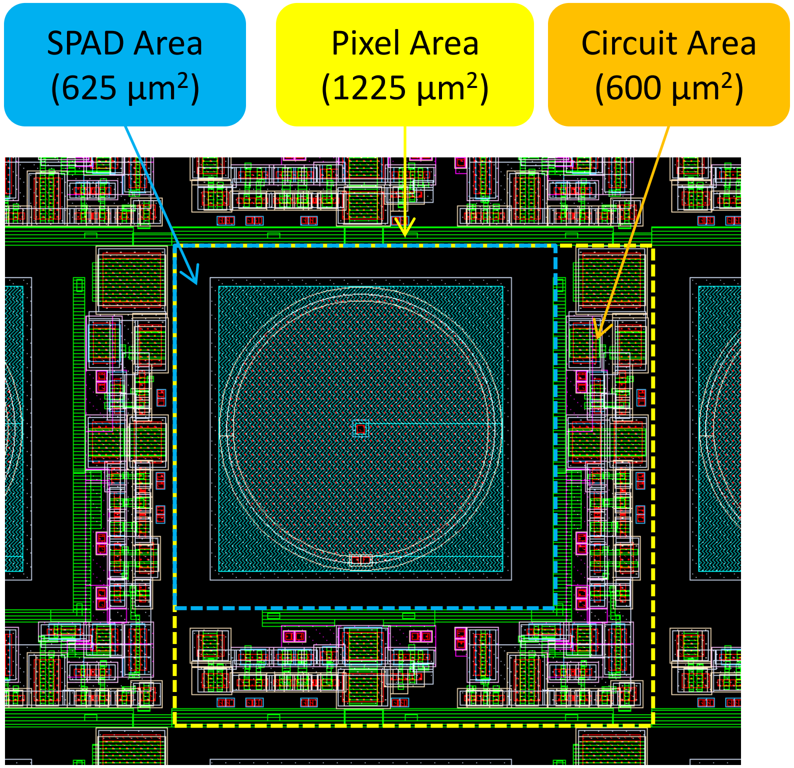


DSPAD Pixel Architecture



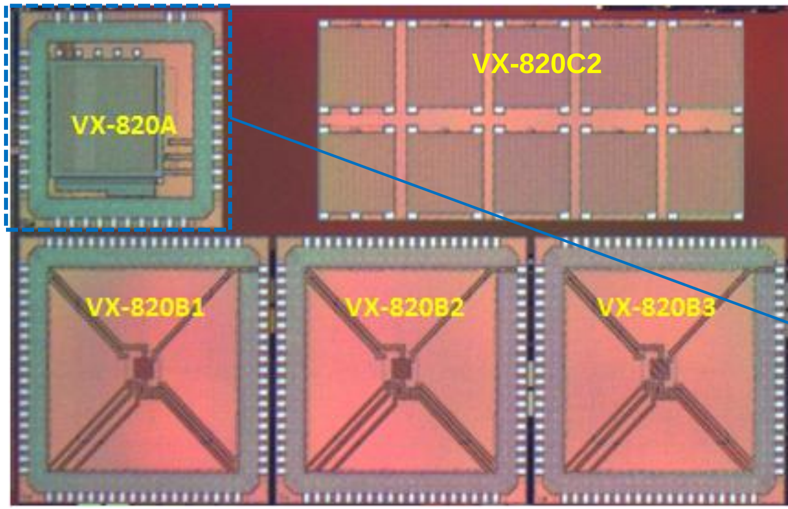
- AQC modulates bias and controls quench time of the Gm-APD.
- In-pixel SRAM to disable individual pixels, improving dark count rate and device yield.
- Pixel output is either number of photons or time-of-flight (analog ramp).
- Local ramp generator may be utilized for improved timing resolution.

SPAD device development supported under DOE contract # DE-SC0006157 (Wafer-scale Geiger-mode Silicon Photomultiplier Arrays Fabricated Using Domestic CMOS Fab)



Prototype Pixel Layout (20% fill factor)

Prototype DSPAD and SiPM Sensors



Picture of VX-820A, VX-820B(1,2,3), and VX-820C prototype sensor designs.

VX-820A: 40 x 40 SPAD Array

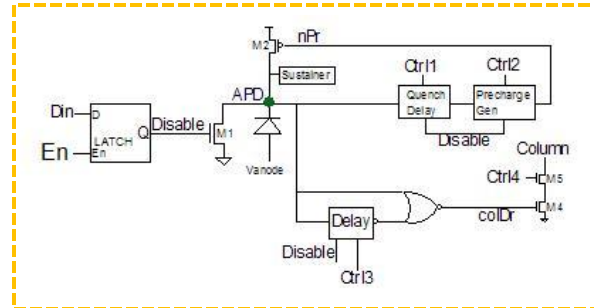
On-chip multiplexer

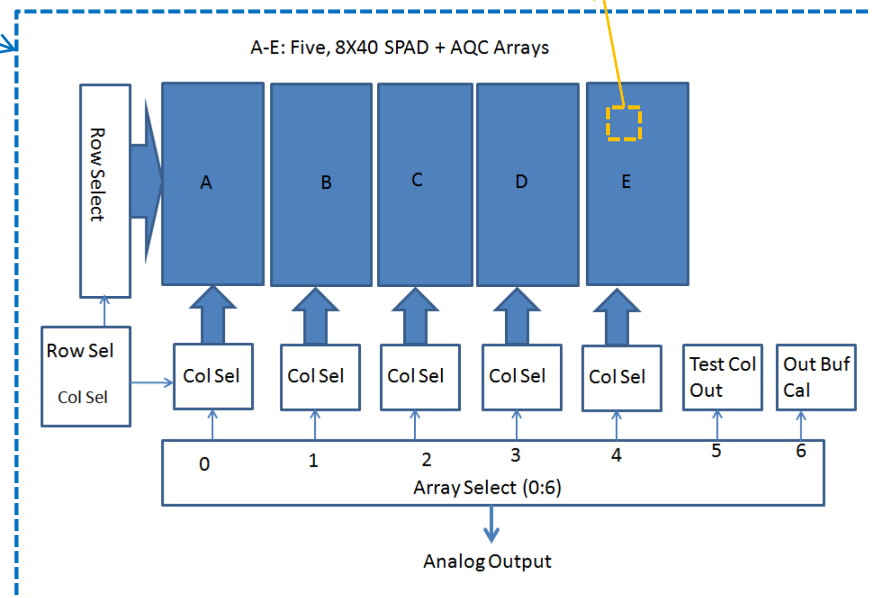
VX-820B (1,2,3): 8 x 8 SPAD Arrays

Fan-out for integration with 64 channel TDC

VX-820C2: 1mm² SiPM Devices

VX-820A pixel block diagram

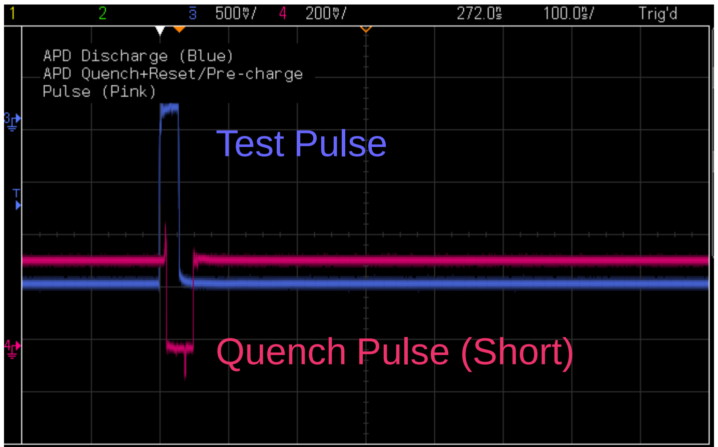


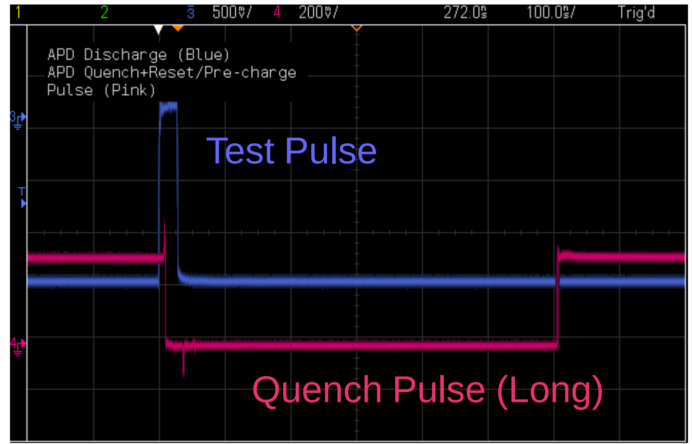


Block diagram of VX-820A sensor including 5 different SPAD arrays (A-E) and the select multiplexer that is utilized to characterize individual pixels within the array.

AQC and Multiplexer Operation

Laboratory demonstration of AQC APD quench and re-arm operation. Quench time is adjustable from 12 – 1200 ns.

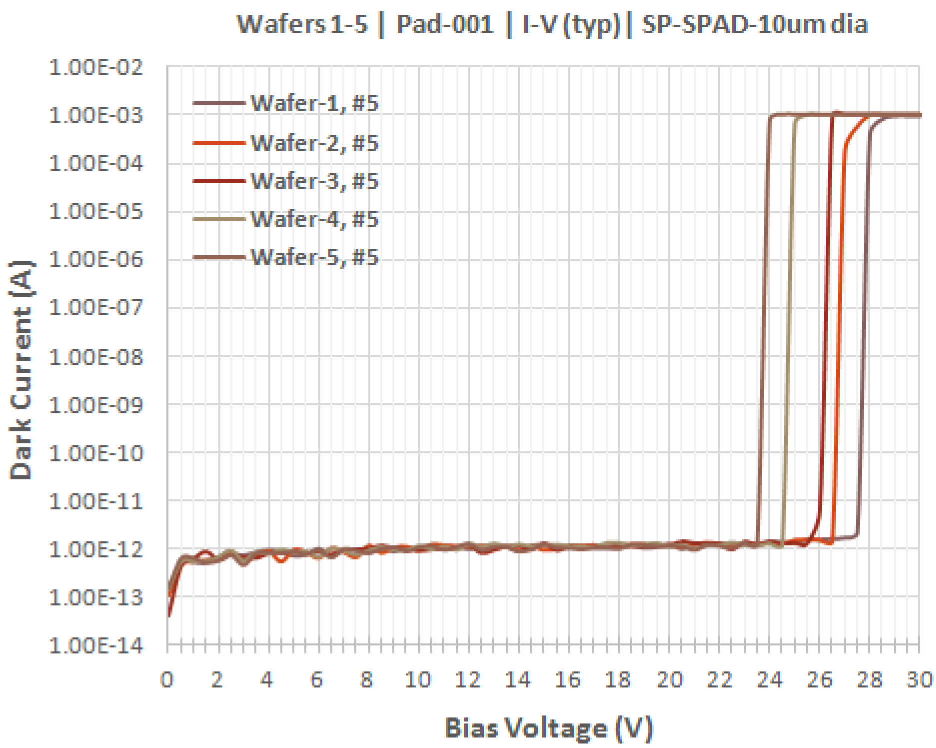




Summary of key AQC timing parameters verified by measurement

	Simulated Nom		Meas. Nom	Measured Max		Measured Min	
Description	Nom Curr (µA)	Sim val.	PD/Amp	Min Curr (µA)	PD/Amp	Max Curr (µA)	PD/Amp
Pixel quench duration (qcap)	-20		149ns	-320	12ns	-1	1190ns
Quench Pulse duration on APD Anode	-20		540ns	-320	37.5ns	-1	4250ns
Pixel precharge/reset duration (nPr)	500	2.2ns	3.9ns	1	1000ns	660	3.4ns
Pixel Col pulse duration (PD)	-10		95ns	-1	460ns	-90	12ns
Column pulse amplitude (test AQC)	100		(-)15mV	10	(-)3mV	450	(-)60mV
Column pulse amplitude (SPADA)			(-)15mV			690	(-)96mV

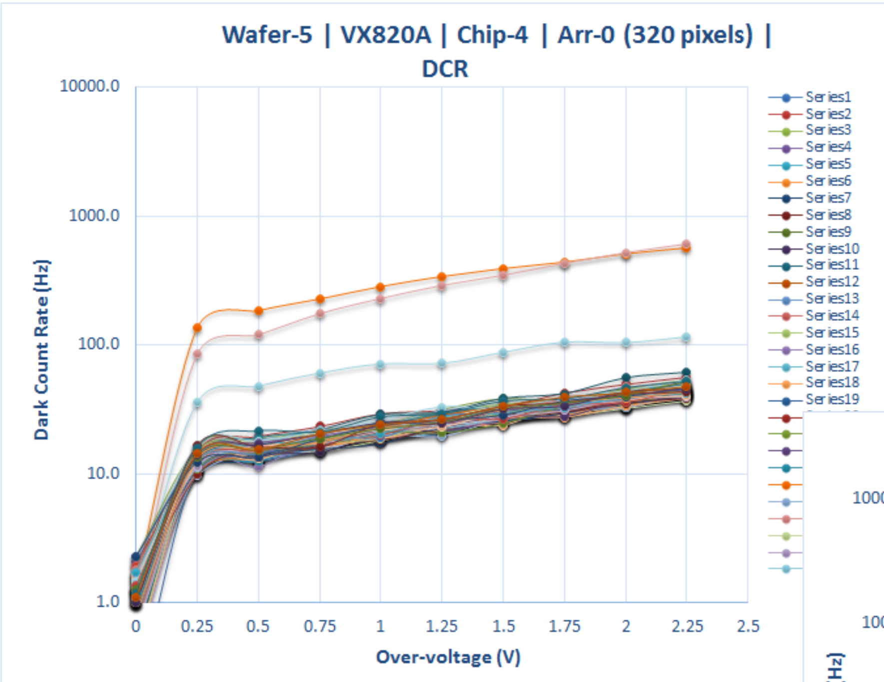
Breakdown Voltage



Wafer #	Measured V_{BR} (V)
1	27.5
2	26.5
3	25.5
4	24.5
5	23.5

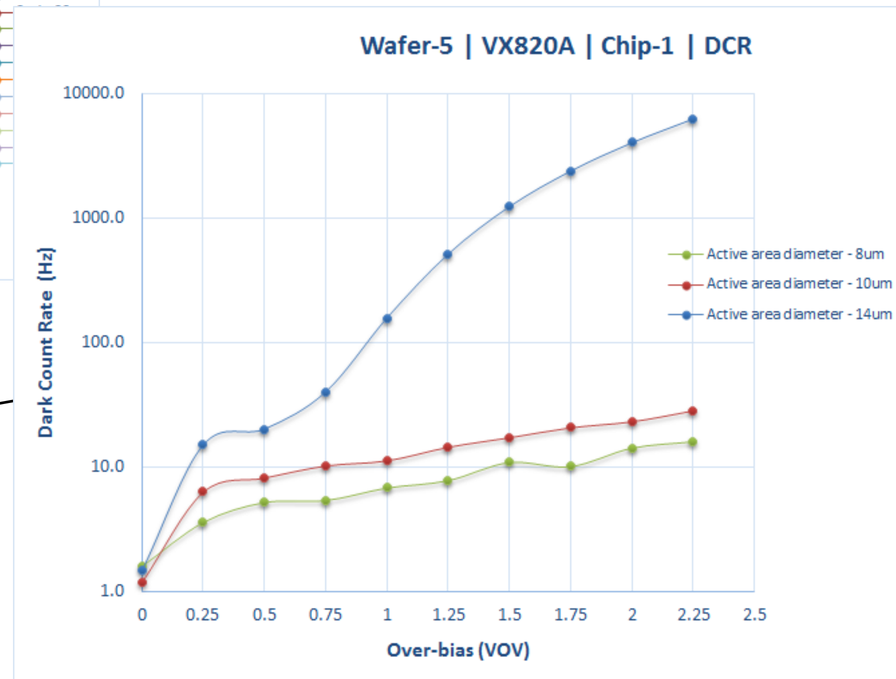
Target breakdown voltage was 13-25 V for wafers 1-5. Difference resulted from misplacement of annealing step in initial device process model. Upon changing the process simulation model to match the fabrication process flow, the measured breakdown voltages match the simulation results.

Dark Count Rate (DCR)

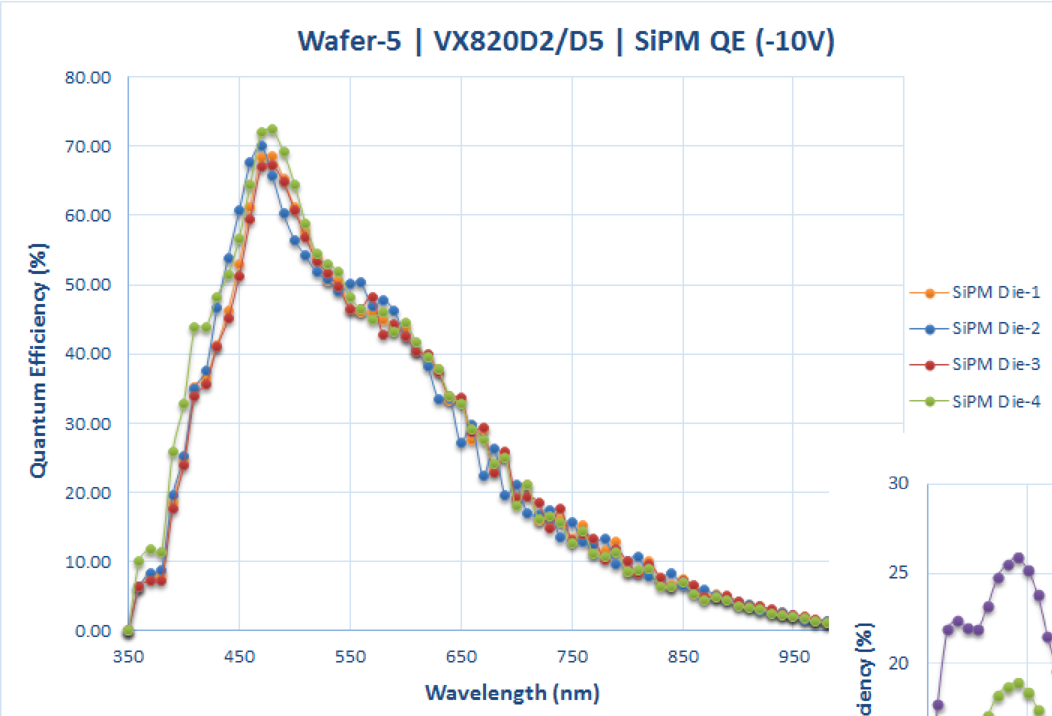


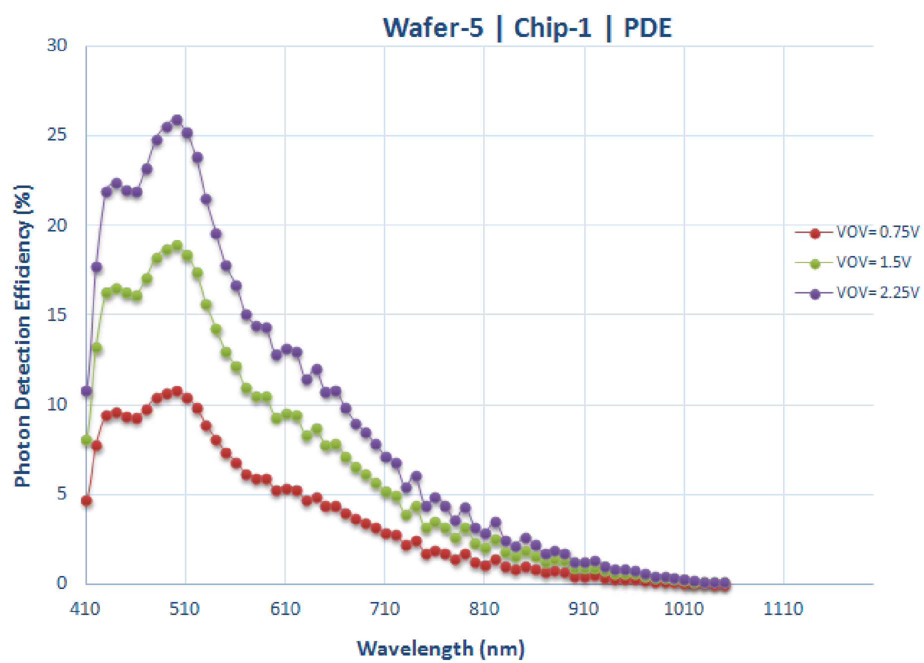
- Average DCR is 25-40 Hz at 2.25V over-bias (~9.2% V_{OB}).
- Roughly 2% screamer pixels.
- DCR scales roughly with active area.
- Negligible crosstalk and after pulsing effects.

The 14-µm diameter active area device has a reduced anode to guard ring spacing resulting in an early increase in DCR.



Quantum/Photon Detection Efficiency



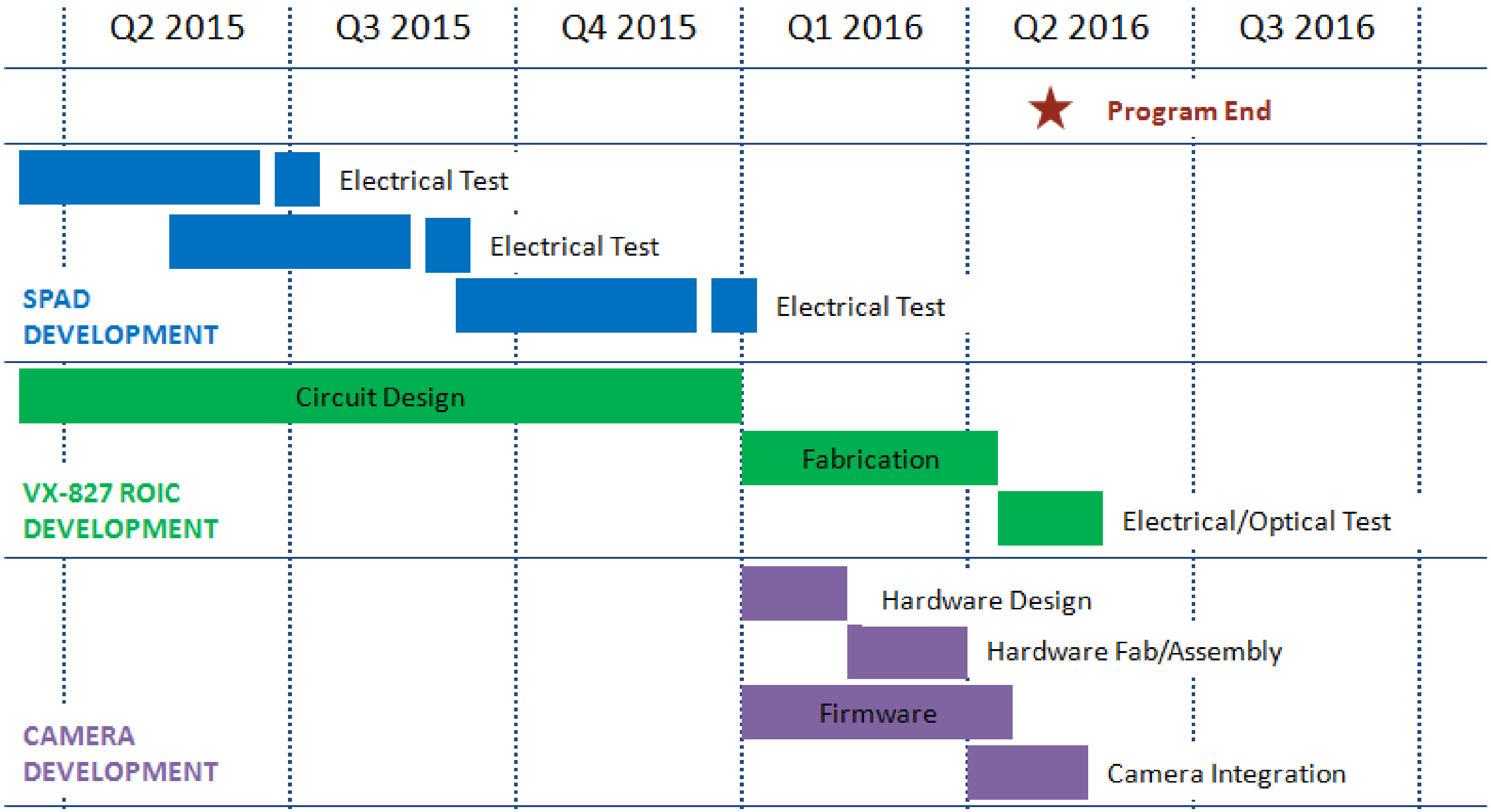


- PDE is measured on single element SPAD (VX-820A sensor).
- Measurements at wavelengths below 450 nm are questionable (noise floor of ref. detector).

DSPAD Array Specification Summary

Specification	Goal	Notes
Pixel pitch, resolution	30 µm, 256 x 256	Baseline
Frame rate	500 Hz	Assumes 1 ms integration time, snapshot, integrate-then-read
Sensitivity	Single photon	Gm-APD device
Dark count rate	< 150 counts/pixel/sec	Based on measured VX-820 data, scaled to active area
Photon detection efficiency	> 25% peak	At 500 nm, PDE >10% from 400 – 650 nm
AQC quench time	10 – 50 ns	Active, adjustable through DSI
Counter dynamic range	12-bits	Integration mode
ToF minimum gate time	250 ns	37.5 m depth, can be longer
SPAD jitter	~100 ps	Current estimate, measurement in progress
Timing resolution	120 ps	In TOF mode, jitter + time-to-digital conversion (61 ps)
Timing dynamic range	12-bits	In TOF mode
Output channels	1 (6-bits parallel)	Digital output, 12-bit ADC, DDR
Output data rate	20 MSPS	LVDS
Pixel disable	Yes	For DCR reduction
Operating temperature	300	Nominal
SPAD device	Silicon, p-on-n	Monolithic
SPAD area	20 x 20 µm	18-um diameter avalanche region - 30% fill factor

DSPAD Development Program Schedule



Lot turns at foundry are currently taking 4-5 months. Schedule is already tight so we are most likely going to need 6 month no-cost extension on the program.

Program Summary

- Technical risk related to monolithic SPAD design has been greatly reduced through VX-820 prototype arrays that were fabricated/characterized early in the program.
- Initial prototype lot had larger than expected SPAD breakdown voltage (>20 V), thus limiting available over-bias in sensor. Modeling error has been identified and was corrected in current fabrication lot – expected September 2015. Continued optimization of SPAD devices.
- DSPAD AQC circuits and readout were characterized to be fully functional with monolithic SPAD devices.
- Prototype DSPAD arrays have demonstrated DCR of <40 Hz at 10% over-bias at room temperatures, with a peak PDE of 26% (at 500 nm).
- Large format DSPAD array (256 x 256) is currently under development with fabrication scheduled for early 2016.

LOOKING FORWARD…

N-type wafers for improved PDE? Back-side illumination?

Questions

Thanks for your time.

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