Digital Silicon Photomultiplier Array Readout Integrated Circuits

ADAM LEE - VOXTEL INC.

Nuclear Physics Instrumentation: Position Sensitive Charge Particle and Gamma Ray Tracking Devices SBIR Topic: DOE 2013 – 42b

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About Voxtel

- Founded 1999
- 50 employees summer 2016 (30% PhD, 80% Advanced Degree)

Voxtel Opto (Beaverton, Oregon)

- Avalanche Photodiode (APD) and PIN Detectors and Arrays
- Eyesafe Pulsed Laser Transmitters
- Rangefinders, 3D Imaging, LADAR, and Electro-Optic Systems
- Readout Integrated Circuits (ROICs)
- Active & Act./Passive Focal Plane Array (FPA)

Voxtel Nano (Eugene, Oregon)

- Nanotechnology Technologies Group
- Nanocrystal VIS-SWIR-Thermal IP Imaging Products
- Analytical Facilities (HRTEM, SIMS, XRD, UPS/XPS)

Vadient Optics (Corvallis, Oregon)

- Inkjet Printed Solid Freeform Fabrication of GRIN Optics

SBIR Program Summary

Statement of Problem

The need for ever more sensitive, compact, rugged, and inexpensive optical sensors is particularly acute in the fields of homeland security, biological sciences, nuclear medicine, astronomy, and nuclear/high-energy physics.

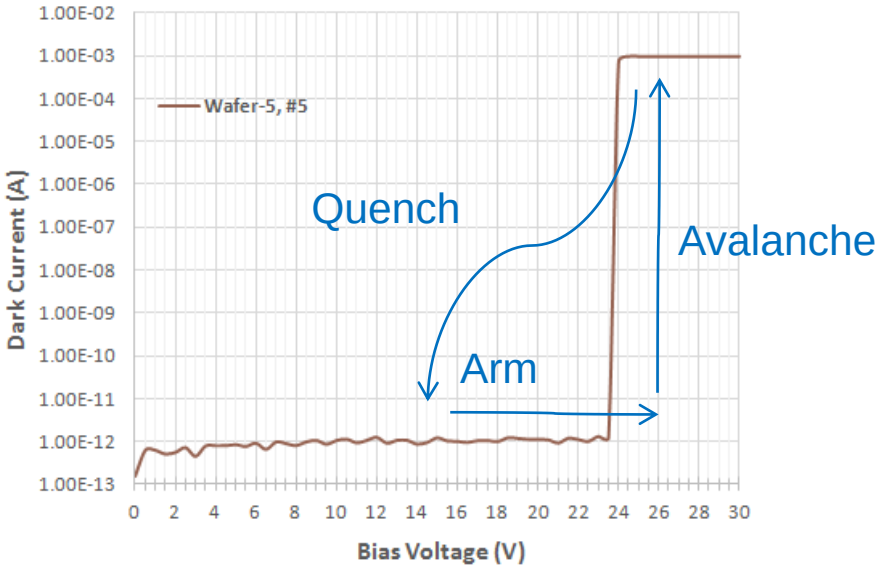
- Applications like fluorescence and luminescence photometry, absorption spectroscopy, scintillation readout, charged particle detection, and Cherenkov imaging require extremely sensitive optical sensors to operate in space-limited and adverse environments.
- Existing detector technologies include: photomultiplier tubes (PMTs), microchannel plate photomultiplier tubes (MCPMTs), silicon photomultipliers (SiPM), **and single photon avalanche detector (SPAD) arrays**

Program Objectives

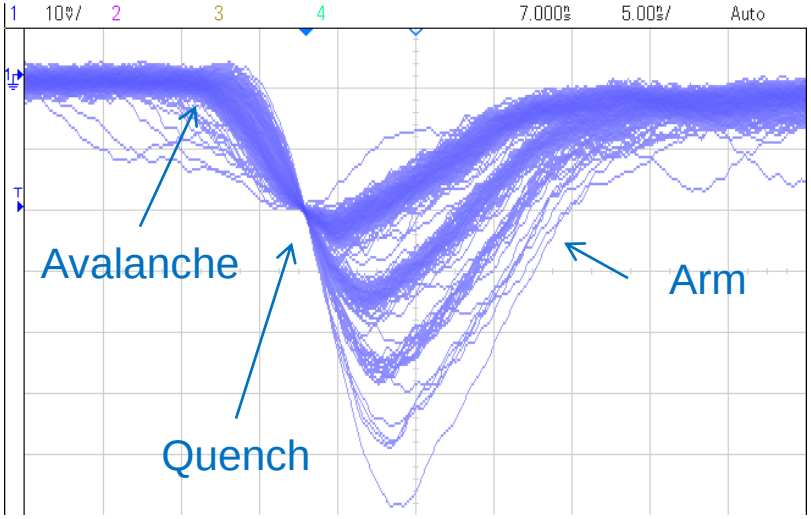
- Complete specification, design, and layout of the large format Digital SPAD sensor.
- Fabricate DSPAD readout, capable of being utilized as readout integrated circuit (ROIC) or monolithic sensor.
- Electrically and optically characterize the sensor.

Geiger Mode (Gm) SPAD Operation

SPAD Operation on I/V Curve

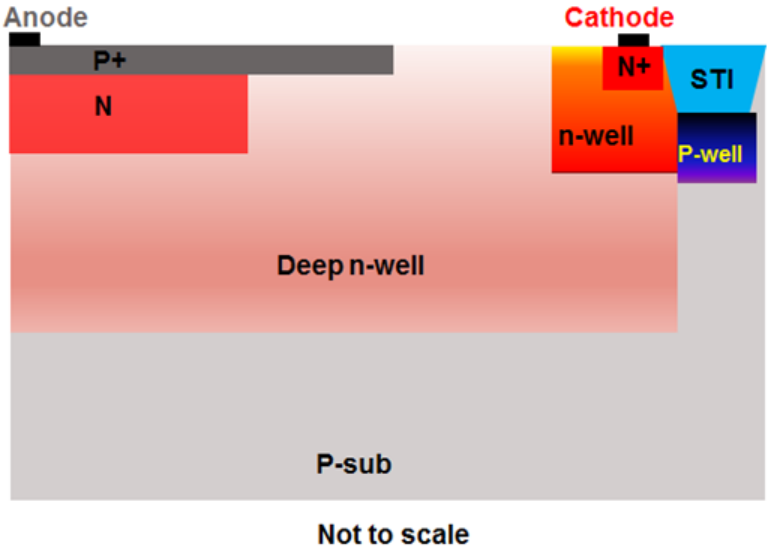


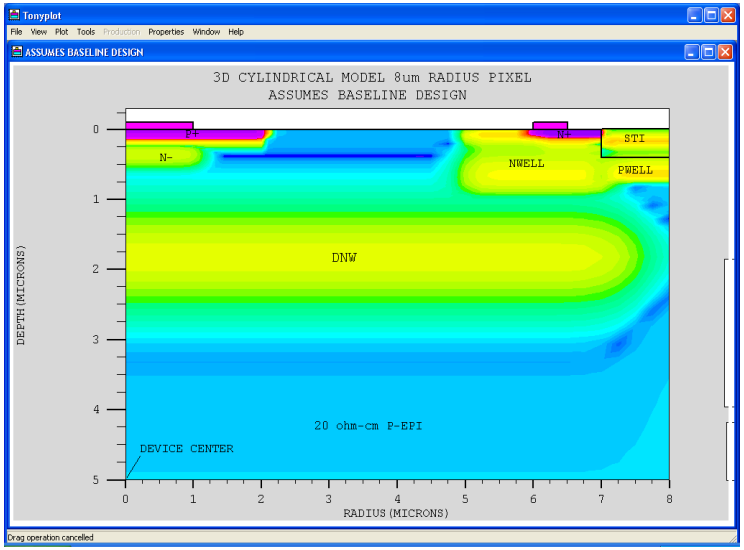
1. Reverse bias is applied to photodiode beyond breakdown potential of device, arming the detector (Arm).
2. A photo- or thermally-generated carrier is collected in the junction, resulting in avalanche current in device (Avalanche).
3. Avalanche current is sensed and photodiode reverse bias is reduced to protect device (Quench).



SPAD Transient Response Example

Baseline Monolithic SPAD Design





Baseline SPAD Cartoon

Simulated SPAD Doping Profiles

- Design optimized for fabrication on standard CMOS process with breakdown voltage <20 V, allowing use of standard CMOS devices for active quenching circuits (AQC).
- Virtual guard ring created using retrograde deep n-well.

SPAD device development supported under DOE contract # DE-SC0006157 (Wafer-scale Geiger-mode Silicon Photomultiplier Arrays Fabricated Using Domestic CMOS Fab)

SiPM Devices vs. DSPAD Arrays

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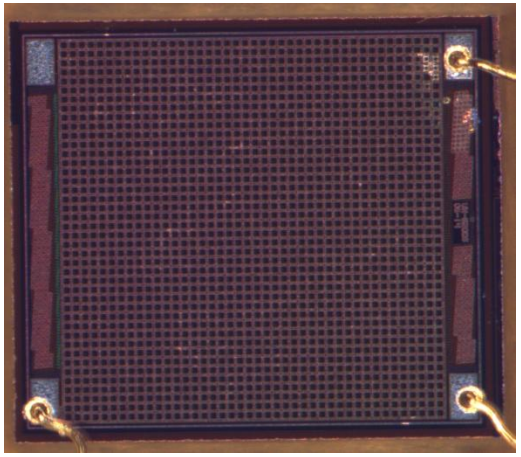
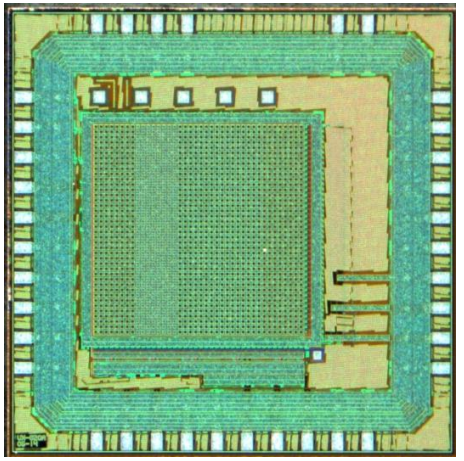
Silicon Photomultipliers (SiPM)



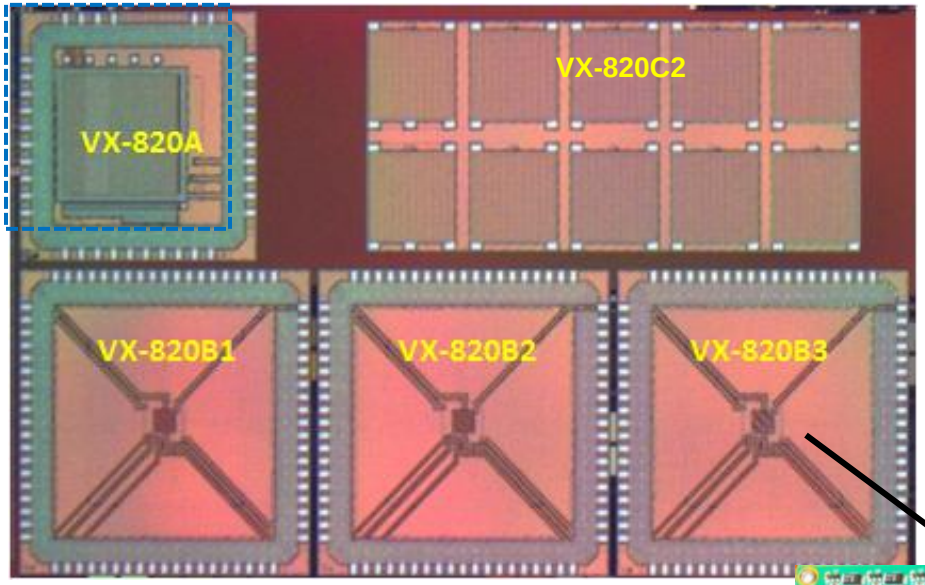
- Based on SPAD element that is passively quenched.
- All of the pixels in the array are connected together – no spatial information.
- Simple electrical integration (2-4 pins).
- Typical active areas of 1x1, 3x3, and 5x5 mm.

Digital SPAD Arrays (DSPAD)



- Based on SPAD element that is either passively or actively quenched.
- Pixels are individually addressed and readout in raster scan method – high spatial resolution within array.
- “Smart” pixel designs implemented to enable integrating and timing operations .
- Larger pin counts result in more complex integration.

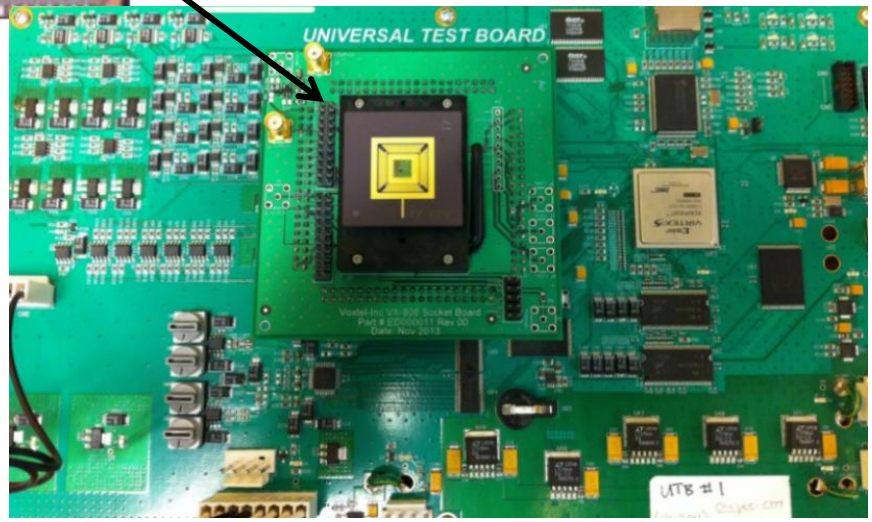
Prototype Sensor Evaluation



Prototype devices (both SiPM and DSPAD sensors) were evaluated and used in optimization of SPAD element and pixel/readout circuits.

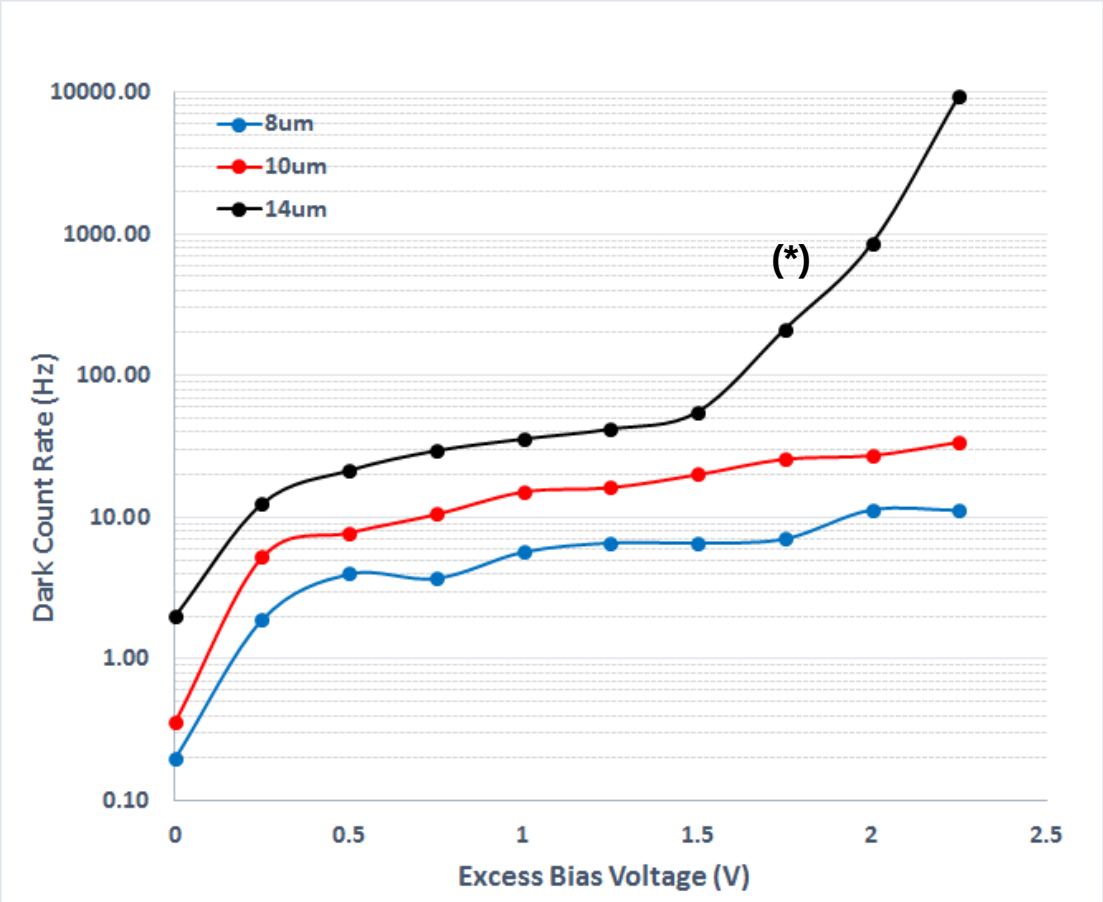
Picture of test system used in prototype SiPM/DSPAD device evaluation.

This prototype evaluation system has also been delivered to collaborators at DOE Jefferson Lab for radiation testing.



Dark Count Rate (DCR)

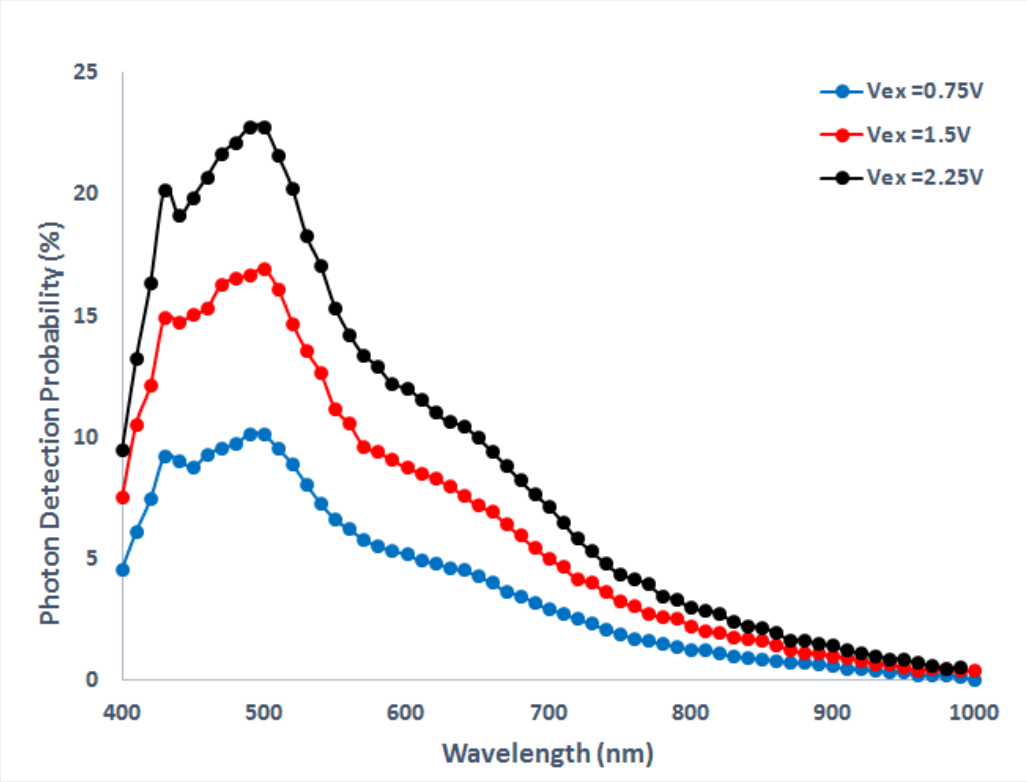
- Average DCR is 10 Hz at 2.25 V overbias (~9.2% over breakdown) for target 8-µm diameter SPAD diode.
- Negligible crosstalk and after pulsing effects (<0.01%) have been measured.
- Roughly 2% screamer pixels in array.
- DCR scales roughly with active area.

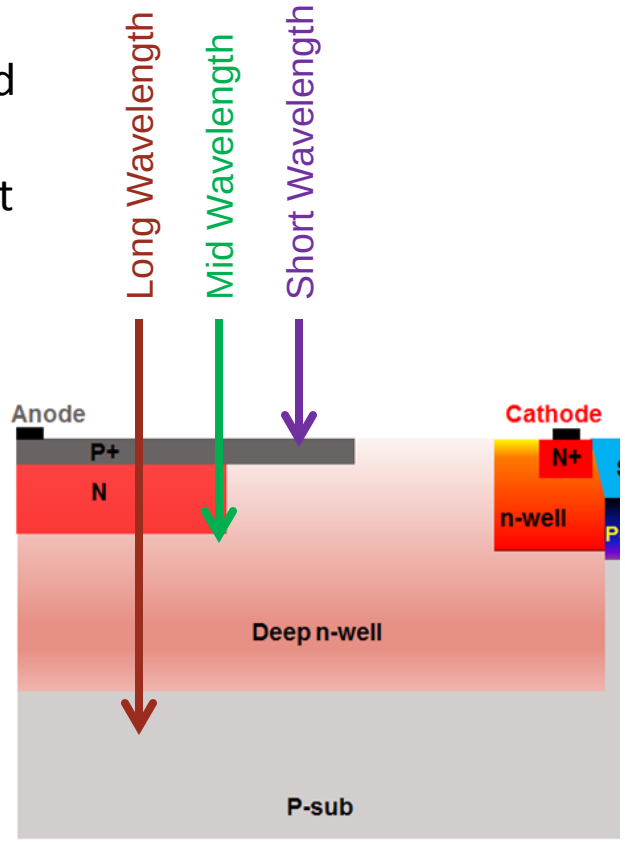


(*) The 14-µm diameter active area device has a reduced anode to guard ring spacing resulting in an increase in DCR at lower excess bias levels.

Photon Detection Probability (PDP)

- PDP measured on single element SPAD device.
- Overbias limited to 2.25 V due to higher than expected SPAD breakdown and limited AQC operational range
- Peak PDP of 23% at 500 nm, 10% at 400 nm, and 3% at 800 nm.





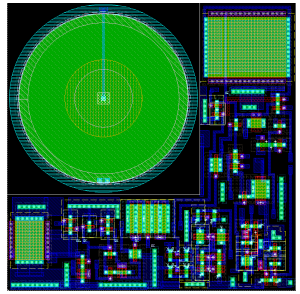
SPAD Visible Light Collection (Front-side Illumination)

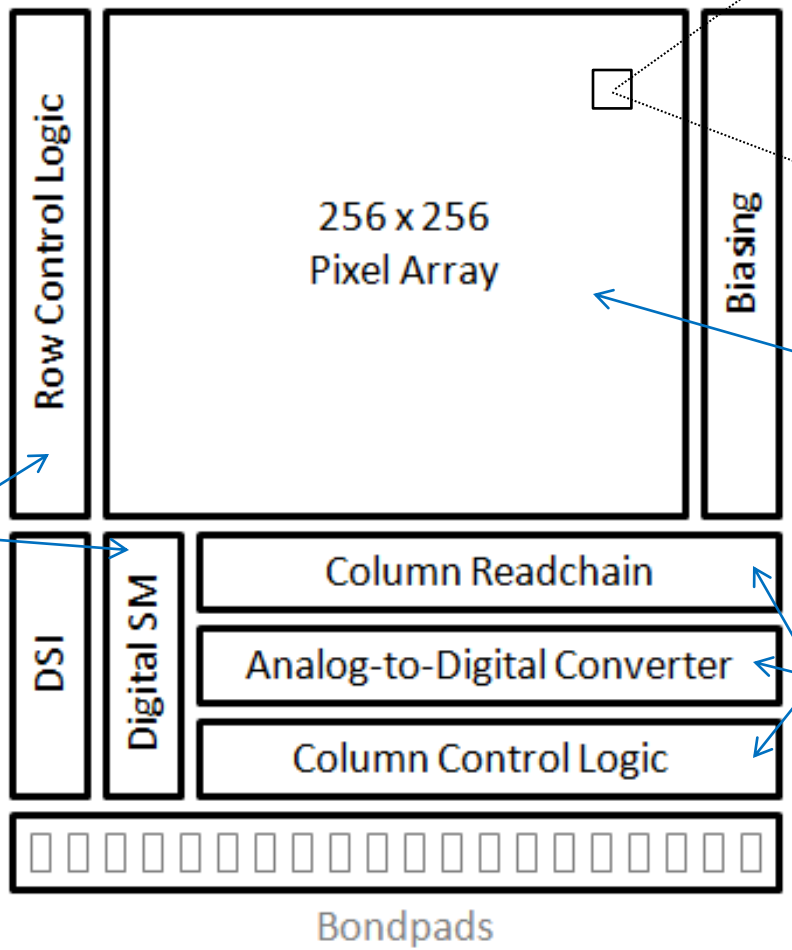
Comparison with Published Sensors

CMOS/CIS SPAD	Typical Specifications						
Parameter	1	2	3	4	5	6	7
Technology	180nm CMOS	180nm CIS	130nm CIS	130nm CIS	90nm CMOS	90nm CMOS	180nm CIS
Fab/Group	Charbon; U. Delft	TowerJazz Israel	Richardson; STMicro	Richardson; STMicro	Charbon; U. Delft	Richardson; STMicro	Voxtel
Year published	2012	2013	2009	2009	2010	2011	2016
Breakdown Voltage (V)	19.7	21.4	9.4, 12.8	14.4	10.4	14.9	23
Active Area (μm^2)	78.5	78.5	58	50.3	45.3	32.2	50.4
Dark Count Rate							
V_{ov}(V)	2	2.5	2	1.4	0.13	2.4	2.25
V_{ov} (%)	10.1	11.7	15.6	9.7	1.25	16.1	9.78
Value (kHz)	0.25-5.06	0.01	0.22	.025	8.1	.1-10	.016
Dark Count Rate per μm^2 (Hz)	637.00	0.13	3.79	0.50	178.81	310.56	0.22
PDP Peak (%)	36 (600nm)	46 (450nm)	36 (480nm)	28 (500nm)	12 (520nm)	44 (690nm)	23 (500nm)
Afterpulsing probab(%)	50	n.a.	< 1	0.02	32	0.375	< 0.01%
Deadtime (ns)	750	n.a.	180	100	1200	n.a.	37
FWHM Timing Jitter							
815nm laser (ps)	n.a.	n.a.	n.a.	200 (V_{ov}=1.4V)	n.a.	n.a.	
790nm laser (ps)	316 (V_{ov}=2V)	n.a.	n.a.	n.a.	n.a.	n.a.	
637nm laser (ps)	n.a.	n.a.	128 (V_{ov}=1V)	n.a.	398 (V_{ov}=0.13V)	n.a.	
470nm laser (ps)	n.a.	n.a.	n.a.	200 (V_{ov}=1.4V)	n.a.	84 (V_{ov}=2.36V)	
405nm laser (ps)	334 (V_{ov}=2V)	n.a.	n.a.	n.a.	435 (V_{ov}=0.13V)	n.a.	TBD

Voxtel's prototype SPAD devices demonstrated competitive performance and leading dark count rates with minimal device dead time.

DSPAD Sensor Architecture





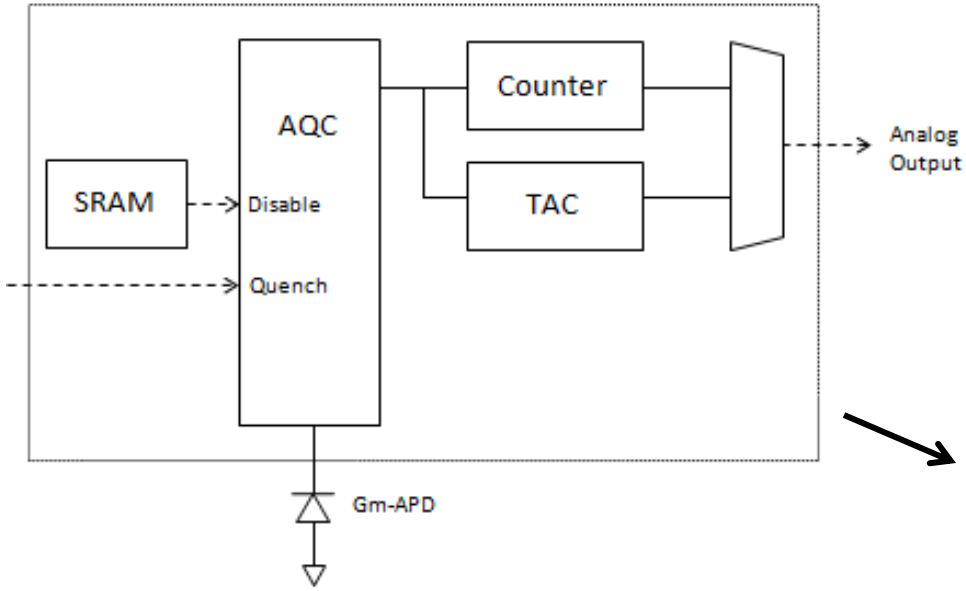
(1) Pixel produces and stores potential representative of integrated photons or time-of-arrival.

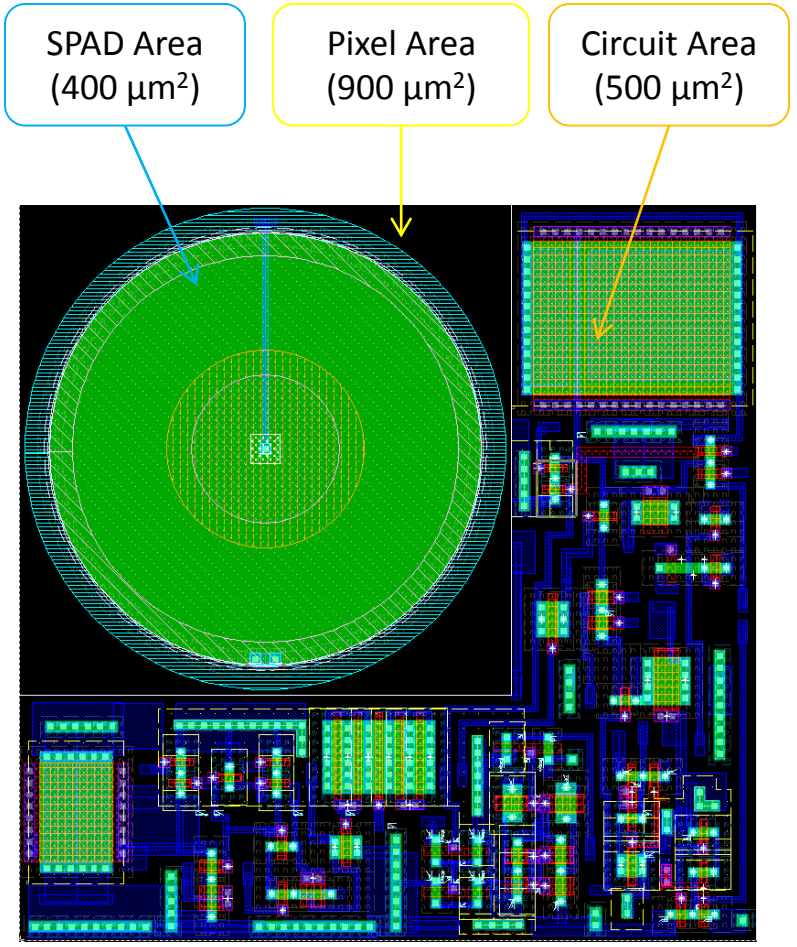
(2) Following active integration or gate time, digital state machine and row control logic scan rows of pixel pixel array sequentially, multiplexing pixel data into column readchain where it is sampled.

(3) Column readchain amplifies pixel data and column control logic multiplexes to ADC for digitization. LVDS drivers are used to drive output digital video.

DSPAD Pixel Development

DSPAD Pixel Block Diagram

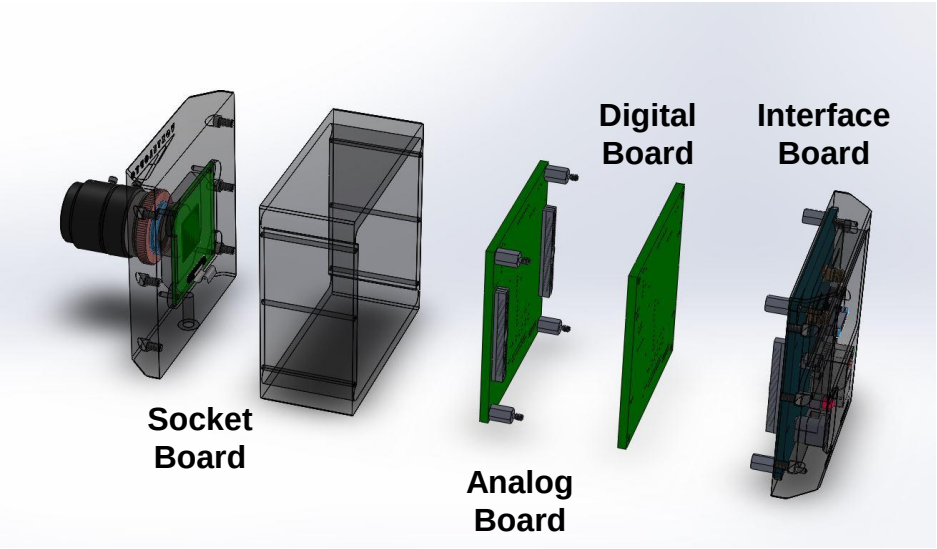


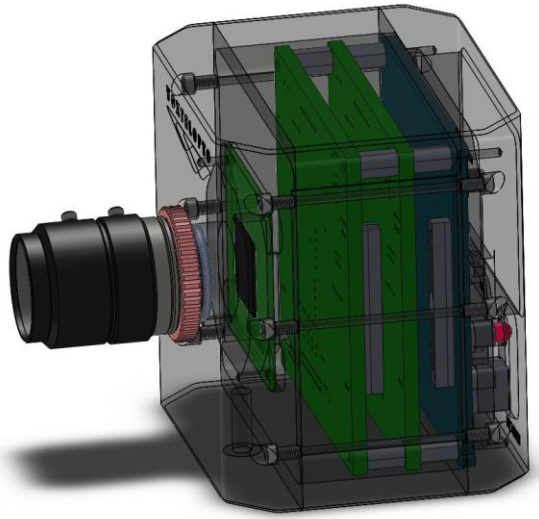


DSPAD Pixel Layout (30-µm pitch)

- AQC modulates bias and controls quench time of the Gm-APD. Generates digital pulse as a result of avalanche.
- Pixel output is either number of integrated photons or time-of-arrival.
- In-pixel SRAM to disable individual pixels, improving dark count rate and device yield.

DSPAD Camera Development





- DSPAD camera electronics is based on Voxtel VC-CAM platform. Camera electronics hardware consists of 1) analog, 2) digital, 3) interface, and 4) socket boards.
- The analog, digital, and interface boards are general purpose – only the socket board needs to be custom designed to integrate the DSPAD sensor.
- Bi-directional communication to/from the PC frame grabber occurs over base configuration Camera Link interface.

DSPAD Array Specification Summary

Specification	Goal	Notes
Pixel pitch, resolution	30 µm, 256 x 256	Baseline
Frame rate	230 Hz	1 ms integration time, snapshot, ITR
Sensitivity	Single photon	Gm-APD device
Dark count rate	< 10 counts/pixel/sec	Based on measured data
PDP	23% peak	At 500 nm, 2.25 V overbias
AQC quench time	10 – 1000 ns	Active, adjustable through DSI
Counter DR	10.5-bits	Integration mode
ToF gate time	15 – 100 ns	can be longer
SPAD jitter	~ 50 ps	Current estimate, measurement in progress
Timing precision	51 / 61 ps	In TOF mode, jitter + TDC (15/100 ns gate)
Timing DR	8.1 / 10.6-bits	In TOF mode (15/100 ns gate)
Output channels	1 (6-bits parallel)	Digital output, 12-bit ADC, DDR
SPAD device	Silicon, p-on-n	Monolithic
SPAD active area	20 x 20 µm	8-um diameter – 5.5% fill factor

Program Summary

Program Progress

- Technical risk related to the monolithic DSPAD design was greatly reduced through the development of several prototype arrays that were fabricated/characterized early in the program. These designs have served as optimization platform for the SPAD design.
- SPAD performance competitive with published CMOS based SPAD arrays has been demonstrated including DCR of 0.22 counts/μm^2 and peak PDPs of 23% (500 nm).
- The large format (256 x 256, 30-µm pixel pitch) monolithic DSPAD sensor (VX-827) is currently in the design stage with an expected completion date of September 2016. The VX-827 pixel design supports both photon counting and time-resolved modes of operation with over 10-bits of dynamic range and sub 100 ps timing resolution.

Program Summary

Future Program Plans

- Fabrication of the DSPAD sensor (VX-827) requires 3 month fabrication time and will be complete by January 2016.
- DSPAD evaluation camera based on VC-CAM platform will be developed in parallel with the DSPAD sensor fabrication.
- Further collaboration with Jefferson Lab will used to determine the radiation hardness of the SPAD devices, as well as the impact of disabling pixels that have received radiation damage.

Looking Forward…

- Long term goal is to develop back-side illuminated (BSI) sensor in attempt to optimize PDP in NIR and/or UV wavelengths.

Questions

Thanks for your time.

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