

# **High-Speed, Multi-Channel Detector Readout Electronics for Fast Radiation Detectors**

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# Outline

- Company background
- Readout electronics requirements
- Pixie-500
  - Prototype performance
- Pixie-500e
  - Architecture
  - Improvements
  - Development

# XIA LLC



DXP xMAP



DGF Pixie-4



Ultra-LO 1800



DXP Mercury



DGF Pixie-16



PhosWatch



$\mu$ DXP



DXP Saturn



DGF Polaris



DXP Mercury-4-OEM

# Detector signals

- Coaxial HPGe
  - Energy resolution  $\sim 0.14\%$  at 1333 keV
  - Rise-time  $\sim 50$  ns
- Inorganic scintillators + PMT
  - Energy resolution  $\sim 3\text{--}7\%$
  - Rise time  $\sim 10$  ns
- Organic scintillators + PMT
  - Fast risetime,  $< 10$  ns
  - Pulse-shape discrimination

# Digital Spectrometer Applications

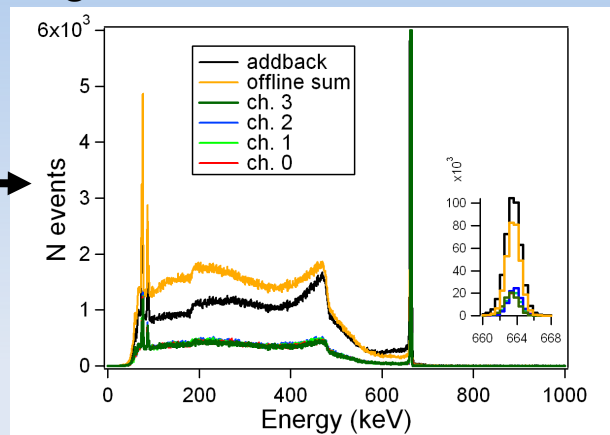
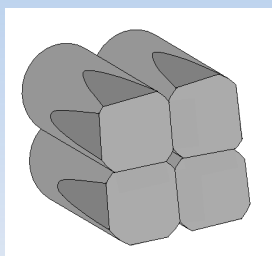
- HPGe
  - Energy resolution
  - Segmented, strip detectors
  - Multiple-site analysis
- Fast scintillators
  - High throughput
  - Low trigger threshold
  - Pulse-shape analysis
- Flexible coincidence schemes

# Digital Spectrometer Applications

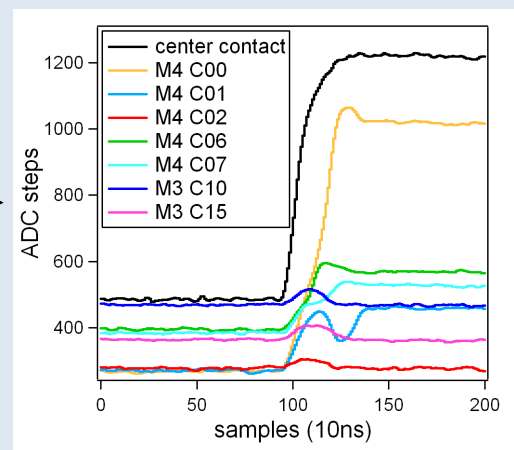
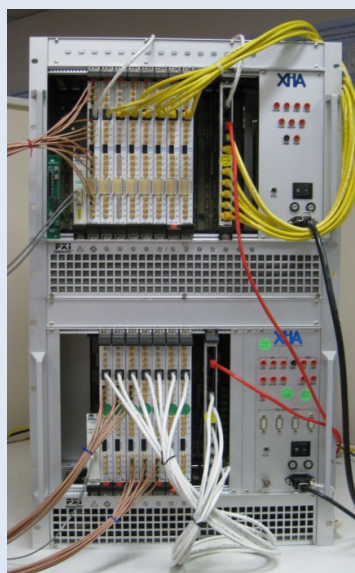
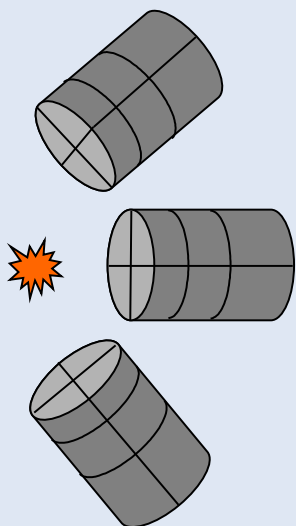
- Pulse-height analysis
  - Slow filter: spectroscopy
  - Pulse-shape analysis
- Timing measurements
  - Fast filter for trigger
  - Waveform capture
- Multiple channels
  - Event hit pattern
  - Trigger distribution
- Custom firmware

# Digital Spectrometer Applications

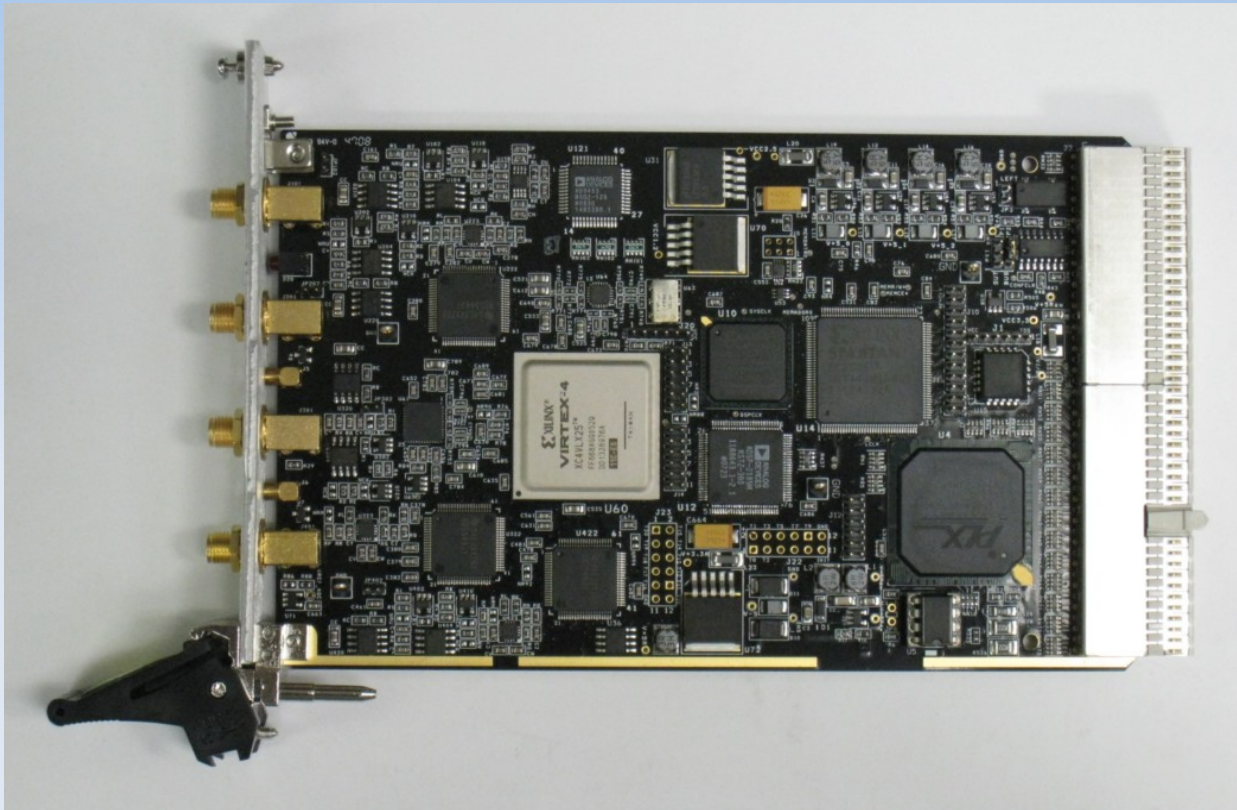
Compact clover readout system with single Pixie-4



HPGe detector array, gamma ray tracking with multiple Pixie-16



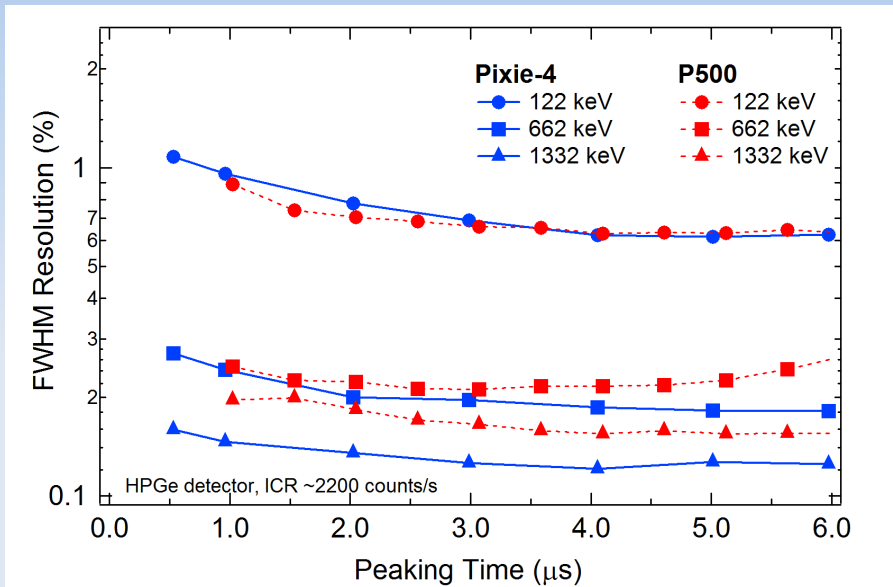
# P500 prototype



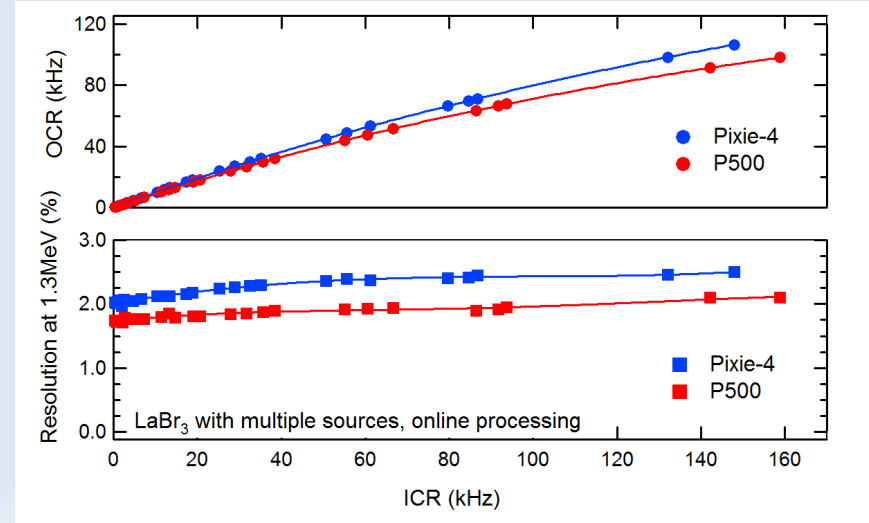
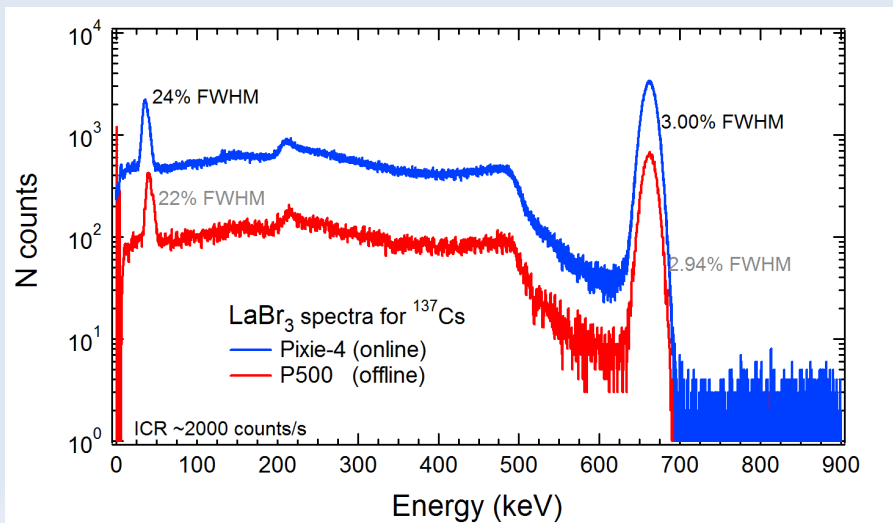
- Pixie-4 (75 MSPS, 14-bit ADC) → P500 (250 MSPS and 500 MSPS, 12-bit ADC)
- ADC to FPGA data flow
- Performance tests



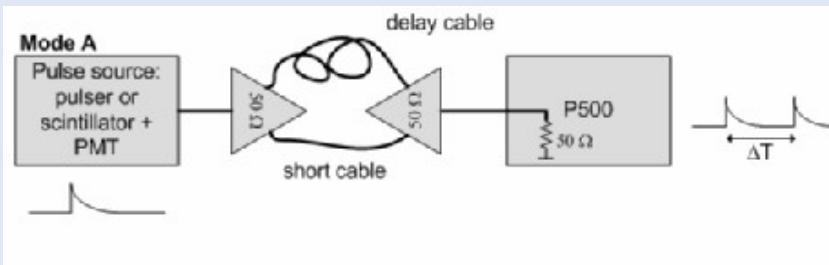
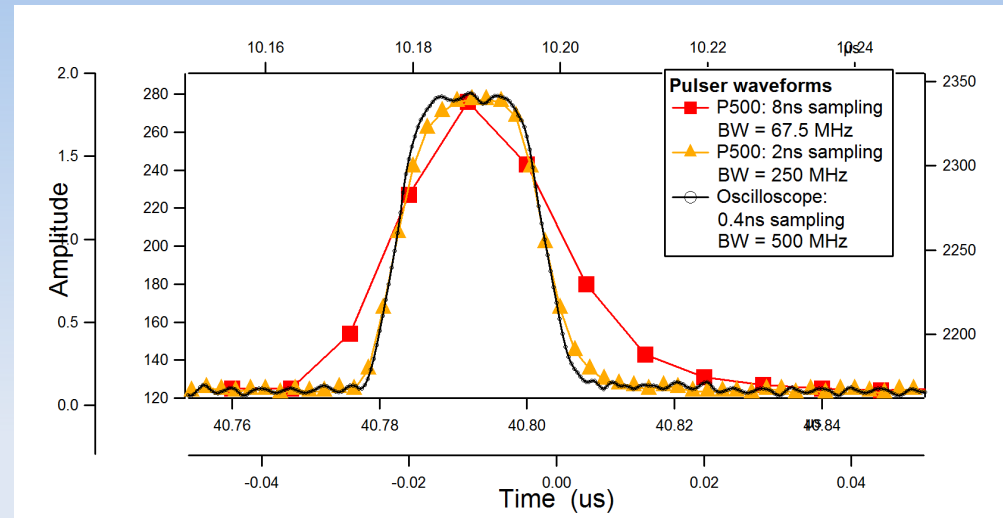
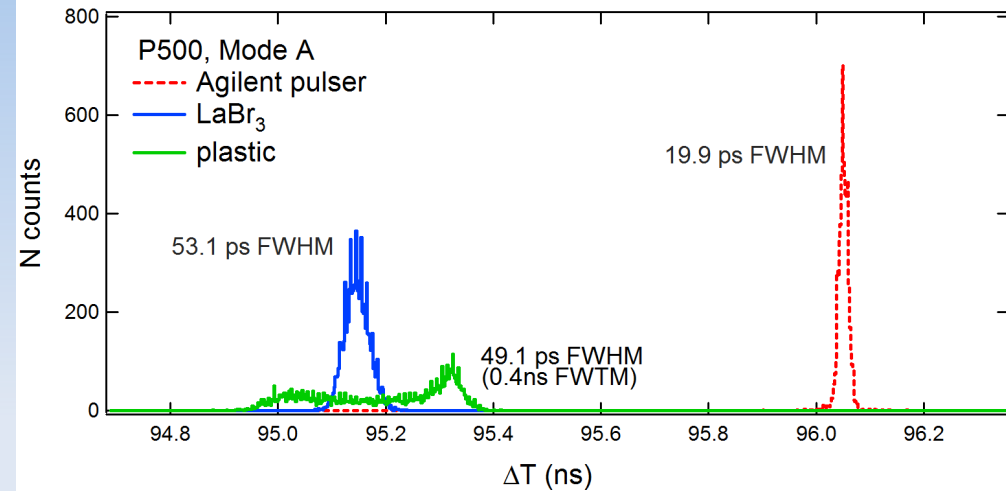
# Energy Resolution



- HPGe, comparable to Pixie-4 (~0.2% FWHM at 1.33 MeV)
- No penalty with scintillators



# Timing

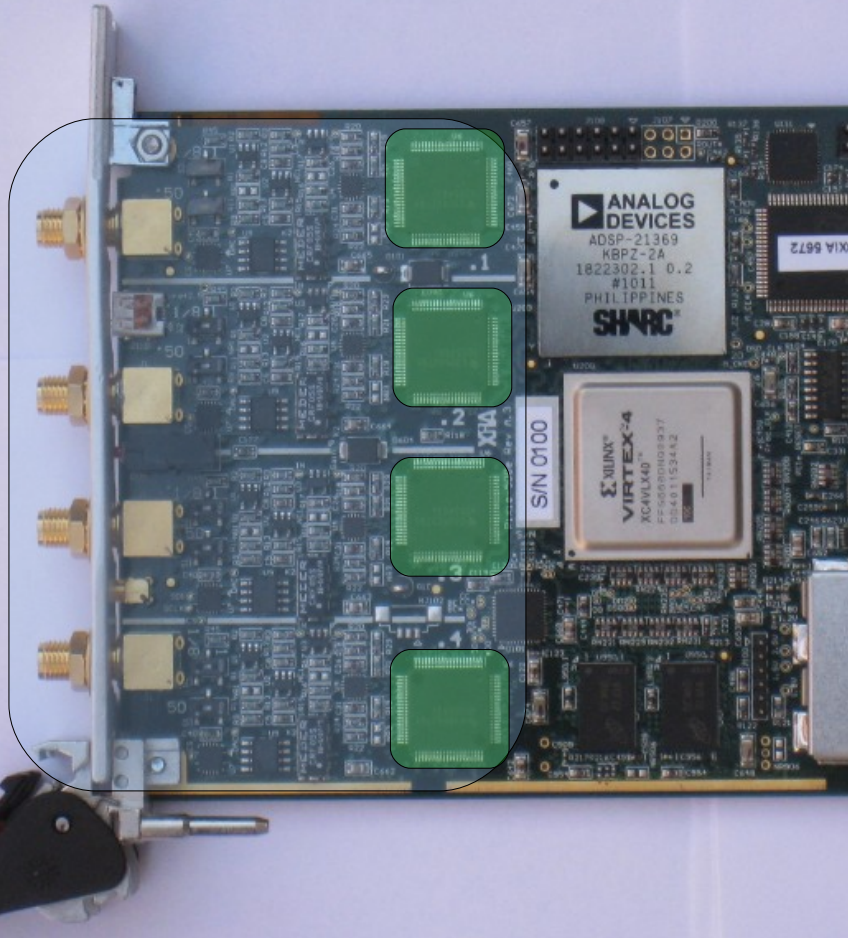


- 20–40 ps from pulser
- 23–100 ps from LaBr<sub>3</sub> detector

# Pixie-500 Express

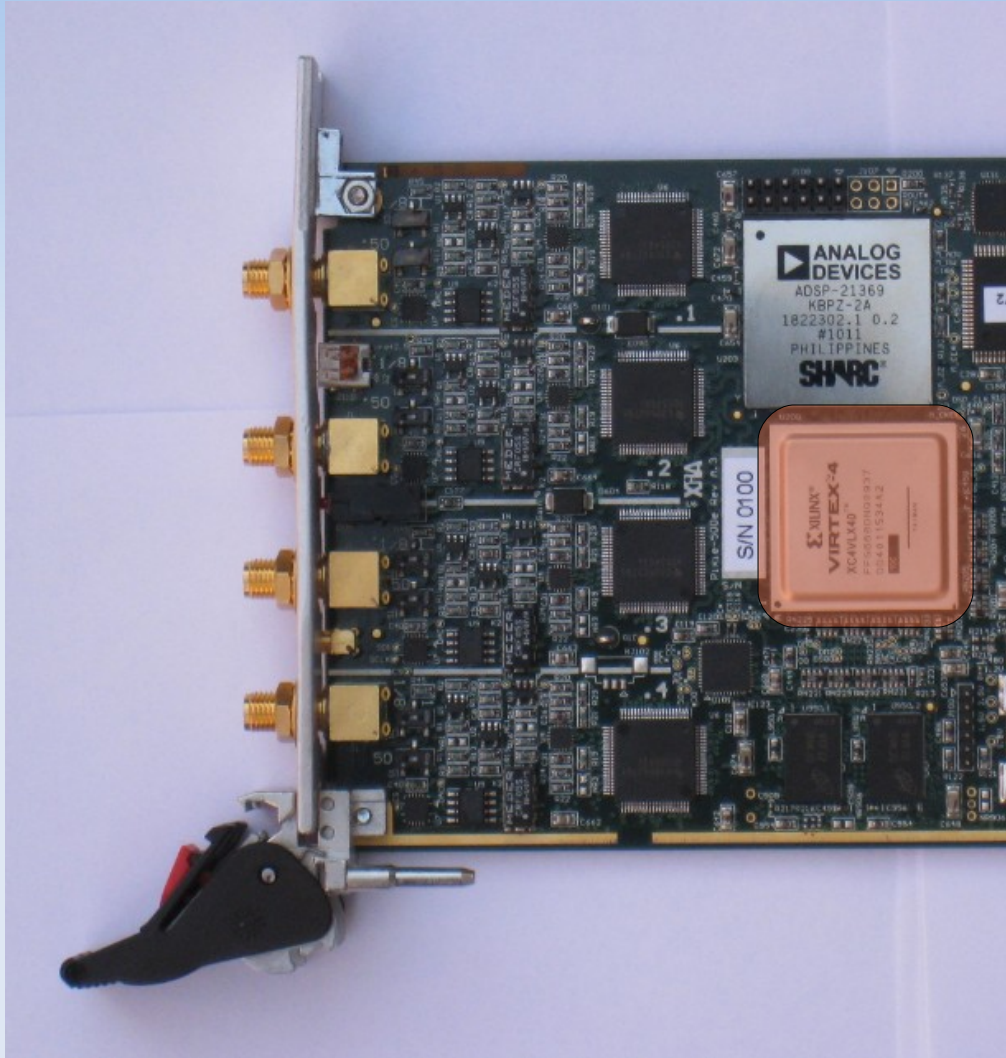
- Architecture changes
- Firmware development
- Host communication
- User code

# Pixie-500 Express



- Gain and Offset adjust
- ADC clock control
- 500 MSPS, 12-bit ADC
  - ADC: 12 LVDS lines at 500 MHz
  - FPGA: 125 MHz

# Pixie-500 Express



- Virtex-4
- De-serialize ADC stream
- Trigger filter
- Energy filter
- Pile-up inspector
- Hit pattern, coincidence

# Pixie-500 Express



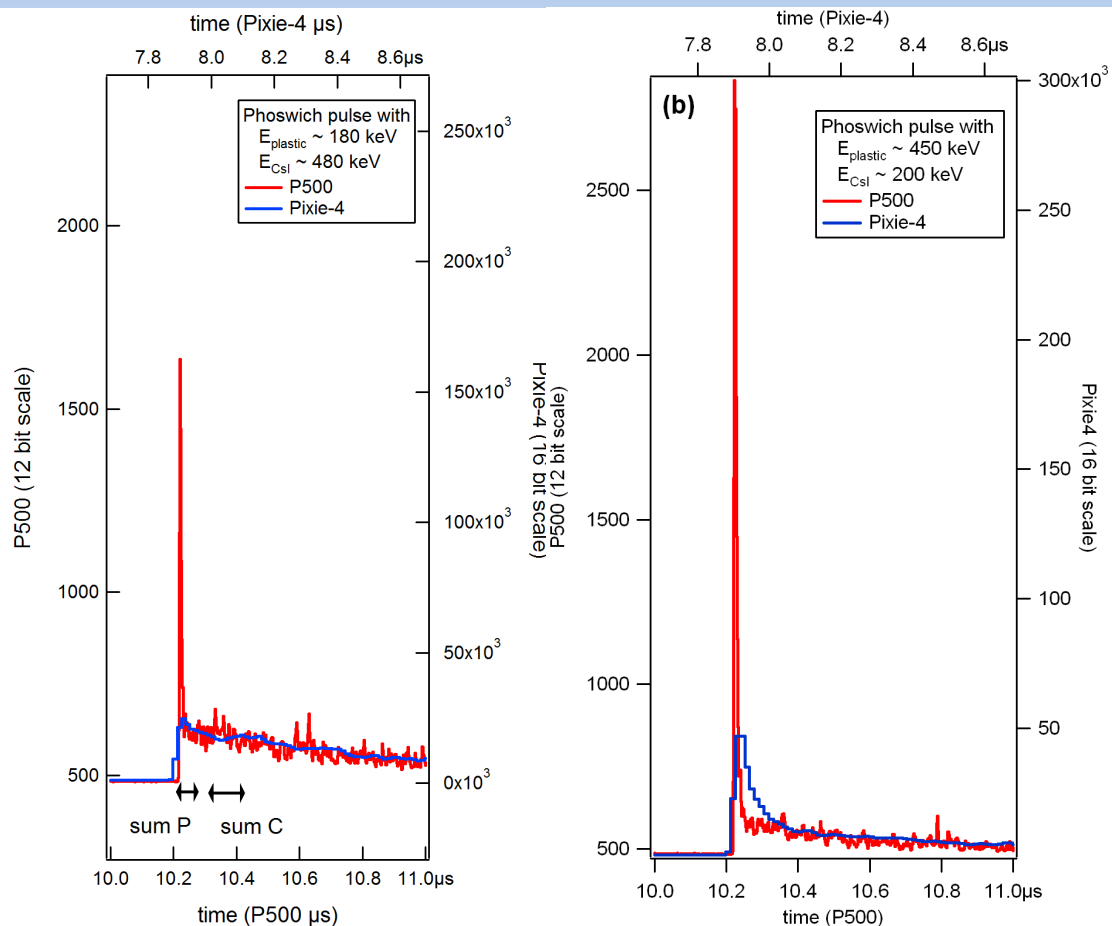
- From 75 MHz, 16-bit fixed point to 300 MHz, 32-bit floating point DSP
- Advanced pulse analysis algorithms
- User code from C, asm

# Pixie-500 Express

- PCI-Express, 4-lane bridge GN4124
- I/O:
  - From 132 MB/s  
(reality: 80 MB/s)
  - To 250 MB/s (1 lane)  
(measured 117 MB/s, 1 lane, at half clock rate)
- x4 with all lanes
- PCIe v.3: 1000 MB/s



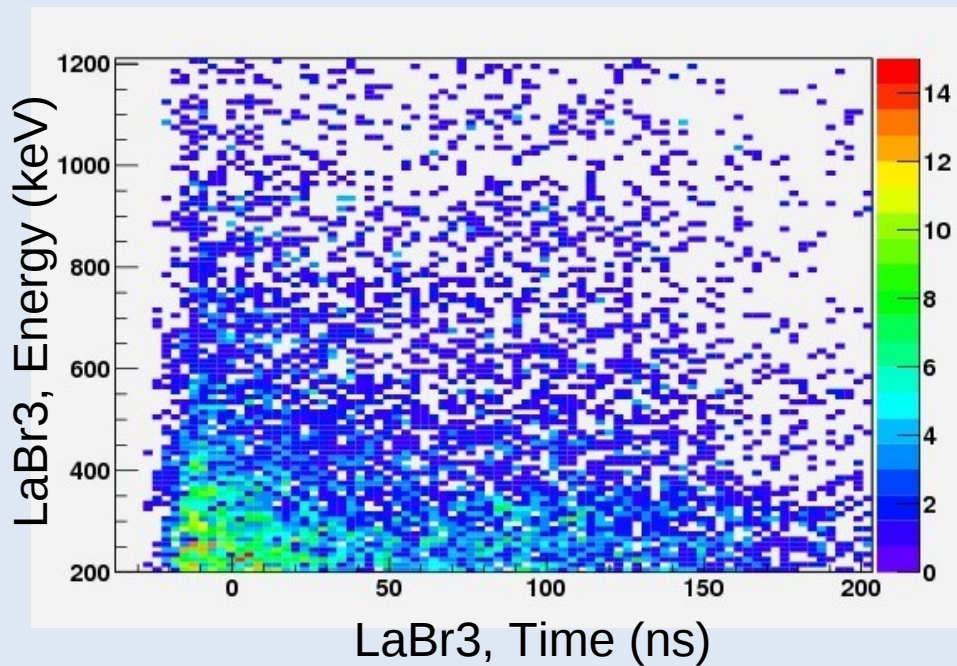
# Pulse Shape Analysis



- BC-404/CsI phoswich
- Combined events:
  - Electrons (plastic)
  - Gamma-rays (CsI)
- Better event discrimination
- Better detector sensitivity

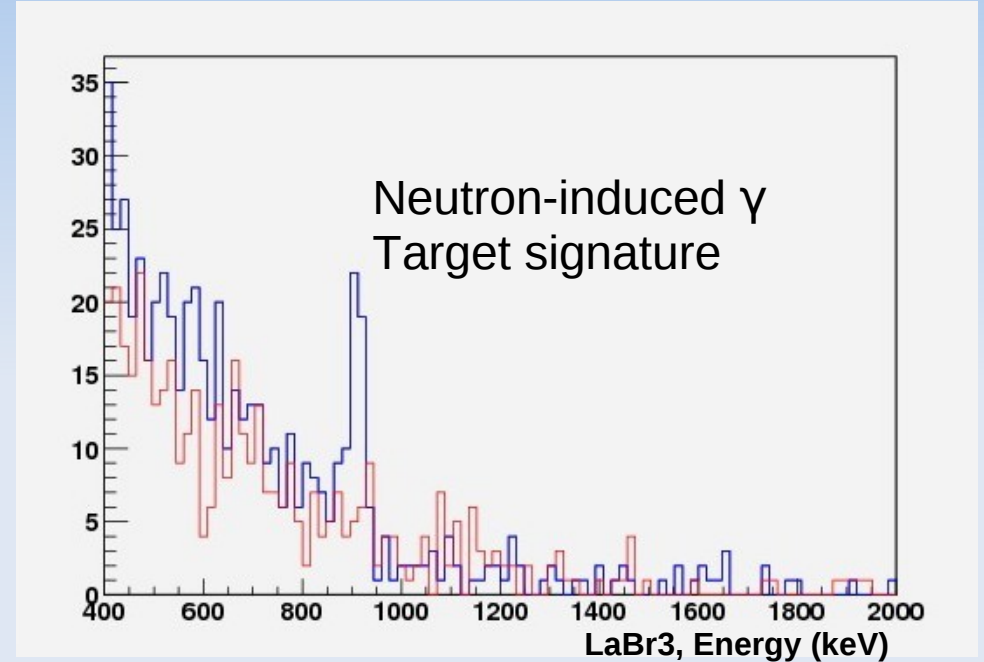
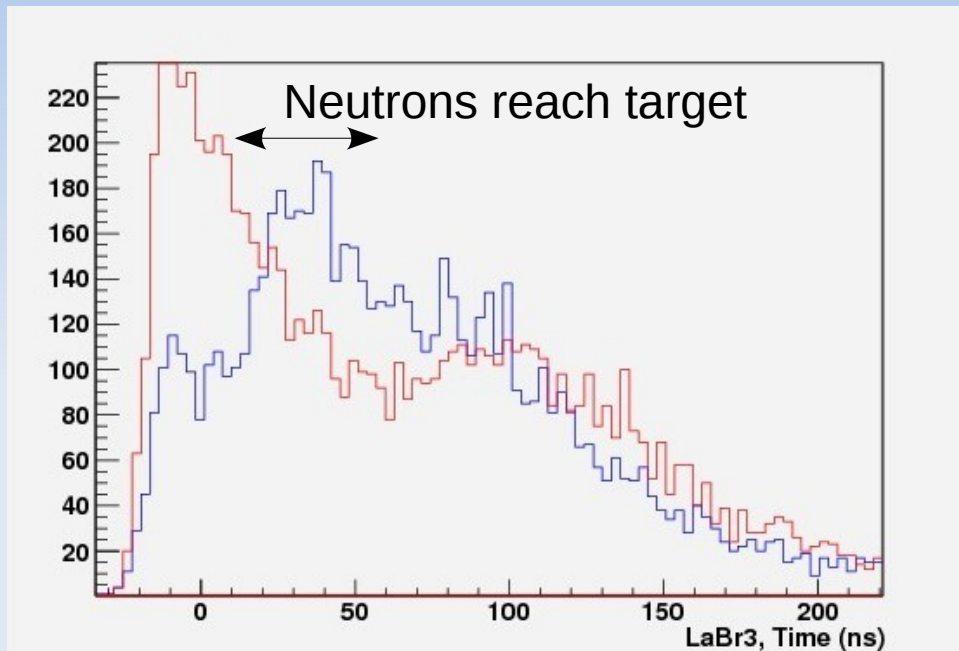


# LaBr<sub>3</sub>/nTOF



- Pulsed neutron source
- Coincidence with machine trigger
- Energy/Time-stamp for all events (+waveform)
- n-TOF with Stilbene

# LaBr<sub>3</sub>/nTOF

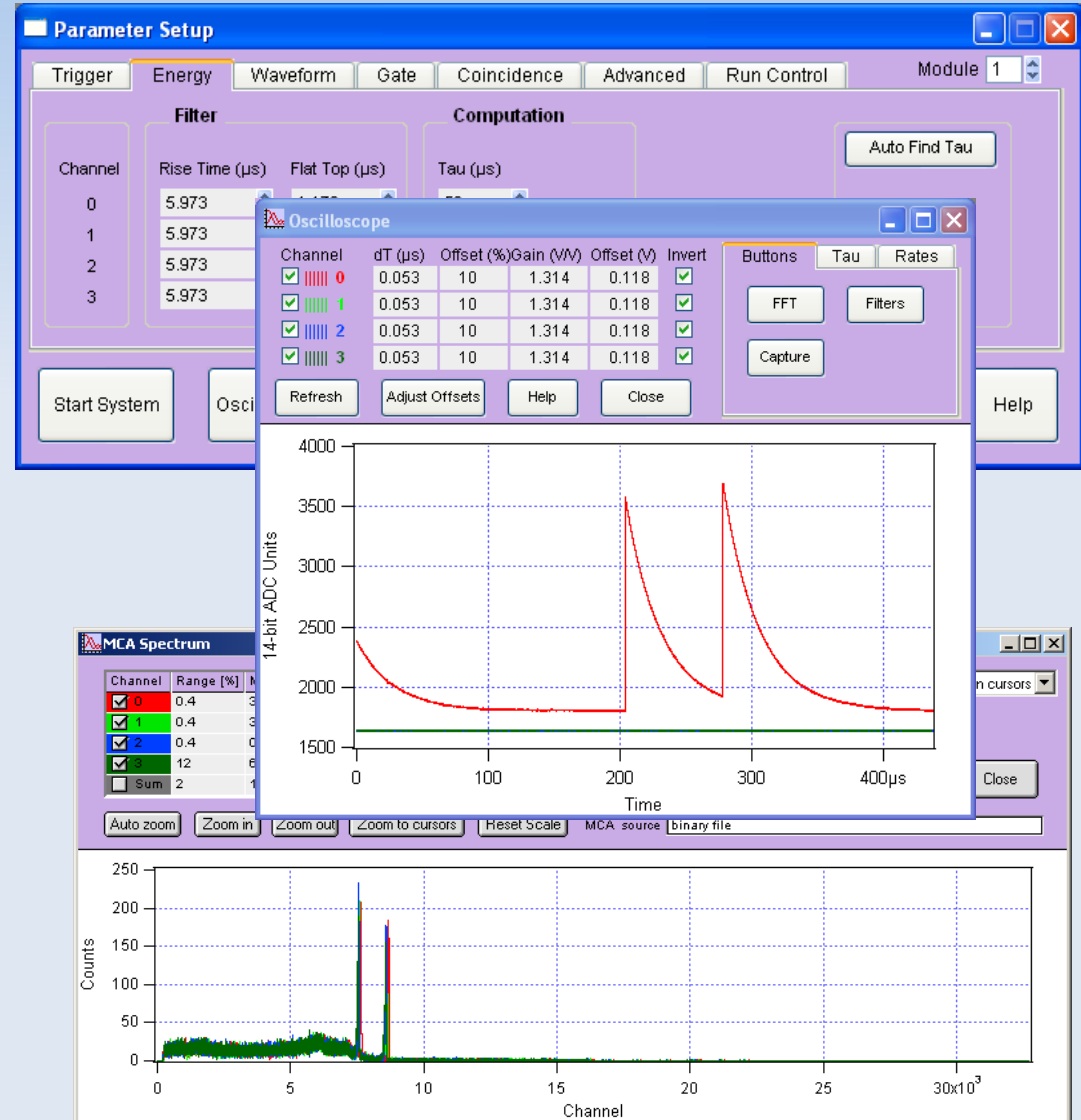
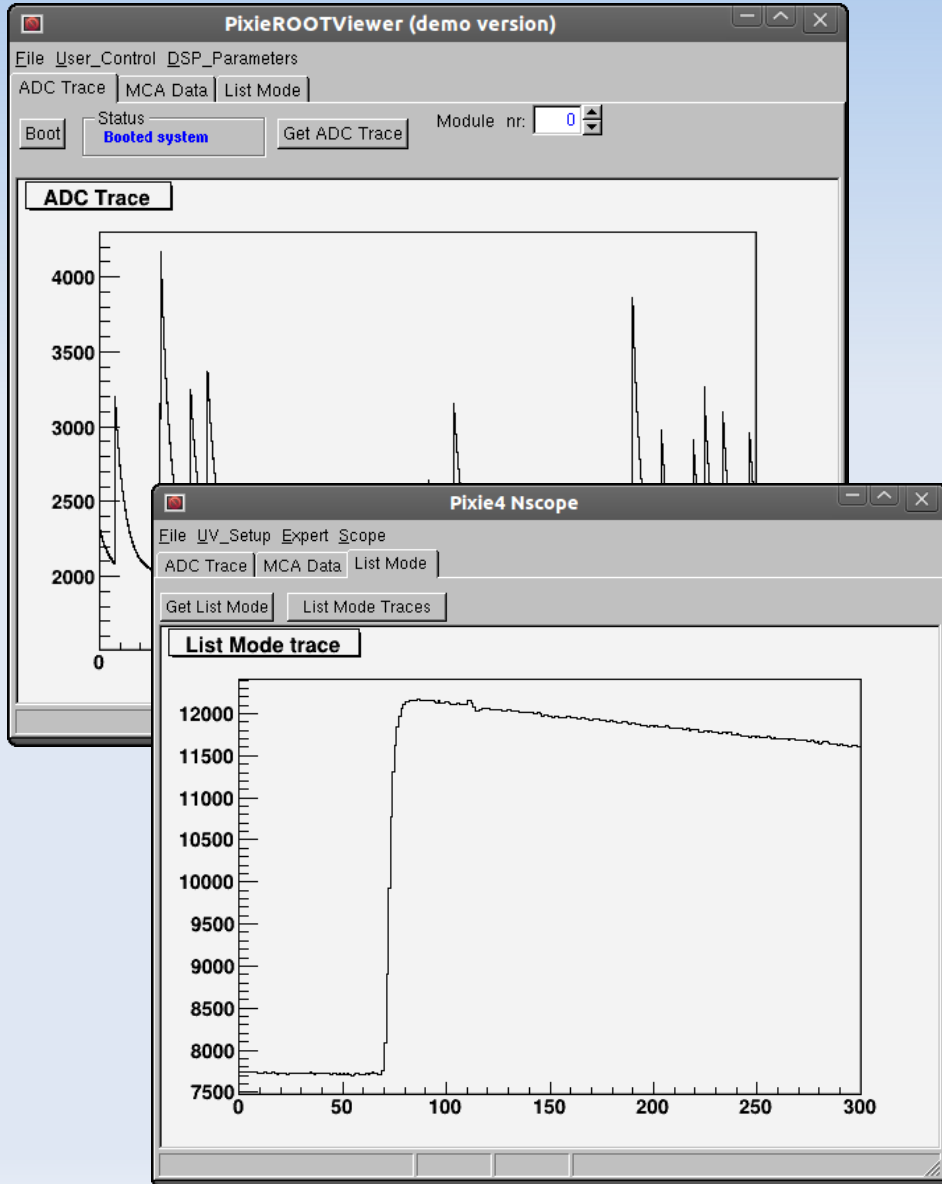


Timing and Energy signals from LaBr<sub>3</sub> with target and without target.

# User Interface

- UI
  - C-library API
    - Boot
    - Settings
    - Run control
    - Data readout
  - IgorPro
  - ROOT
- Custom FPGA firmware
- Custom DSP code (C, asm)

# User Interface



# Outlook

- Implemented high-speed ADC and FPGA communication
- ADC options
  - 12-bit 500 MSPS, 14-bit 400 MSPS...
- Work resulted in other products: Pixie-16 with 12, 14, 16-bit, 250–500 MSPS
- Advanced Firmware development